

This document addresses known errata and documentation issues for the Viterbi Compiler version 4.3.0. Errata are functional defects or errors, which may cause the Viterbi Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Viterbi Compiler v4.3.0 Issues

Altera has identified the following issues that affect the Viterbi Compiler:

- "Incorrect Behavior of numerr Signal" on page 1
- "Multiple Constraint Lengths May Cause Trellis Termination Errors When Using tr_init_state" on page 2
- "Editing Some Hybrid Parameters Can Cause the Maximum Constraint Length and ACS Units to Show Incorrect Values in IP Toolbench" on page 3
- "Changing Architecture In IP Toolbench Can Cause the Maximum Constraint Length to Show Incorrect Data." on page 3
- "The IP Toolbench Latency Calculator Returns Incorrect Values" on page 4
- "The Traceback Length Values that IP Toolbench Sets May Be Inadequate" on page 5
- "Decimal & Octal Can Be Selected Simultaneously" on page 5



For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

www.altera.com/literature/es/es_viterbi_430.pdf

Incorrect Behavior of numerr Signal

The `numerr` signal may provide incorrect data and keep counting up.

Affected Configurations

This issue affects parallel configurations.

Design Impact

You cannot use the `numerr` signal, but the output data is correct.

Workaround

To make the `numerr` signal behave correctly: after a reset, assert the `sink_val` signal for one clock cycle only during the cycle before the first `sink_sop`.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

Multiple Constraint Lengths May Cause Trellis Termination Errors When Using `tr_init_state`

When you specify the state at the end of a block with `tr_init_state`, you must use a number of bits equal to the maximum constraint length minus one irrespective of the constraint length of the code. In theory, you should set `tr_init_state` with a state composed only by constraint length minus one bits; where the constraint length for a code is less than the maximum constraint length. Currently, the Viterbi Compiler does not support the multiple constraint length features in this way.

Affected Configurations

This issue affects all configurations with multiple code definitions and multiple constraint lengths.

Design Impact

You may be unable to correctly terminate a block. Errors may be produced in the last bits of the block.

Workaround

This issue has no workaround. For a solution, contact Altera's mySupport website at www.altera.com/mysupport.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

Editing Some Hybrid Parameters Can Cause the Maximum Constraint Length and ACS Units to Show Incorrect Values in IP Toolbench

There is a synchronization issue between the IP Toolbench Code Sets tab and the Parameters tab. After generating a variation with a maximum constraint length of 8 or 9 and an ACS Units of 8 or 16, if you attempt to edit this variation; IP Toolbench shows incorrect values for the maximum constraint length and the ACS Units parameters. Maximum constraint length shows 7—the correct value is 8 or 9; ACS Units shows 1—the correct value is 8 or 16.

Affected Configurations

This issue affects only the hybrid Viterbi decoder.

Design Impact

If you ignore this issue, you will regenerate an incorrect variation.

Workaround

To resynchronize the IP Toolbench values, click the Code Set tab and change the value of L. When the maximum constraint length shows the correct value, the ACS Units menu shows the allowed values. You can then reselect the correct ACS Units parameter.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

Changing Architecture In IP Toolbench Can Cause the Maximum Constraint Length to Show Incorrect Data.

There is a synchronization issue in IP Toolbench, if you follow these steps:

1. Select **Parallel** architecture.
2. Enter $L = 3$ or $L = 4$ in the Code Sets tab.
3. Return to the Architecture tab and select **Hybrid** and change back to **Parallel**.

The Parameters tab now shows a maximum constraint length of 5—the correct value is 3.

Affected Configurations

This issue only affects the hybrid architecture.

Design Impact

There is no design impact. When you click **Finish** a MegaCore® function is generated with the correct maximum constraint length of 3 for the parallel architecture.

Workaround

To resynchronize the IP Toolbench values, go to the Code Set tab and change the value of L.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

The IP Toolbench Latency Calculator Returns Incorrect Values

The latency calculator on the Parameters tab fails to update the calculation when you change some parameters in IP Toolbench.

Affected Configurations

All configurations are affected.

Design Impact

Ignore the IP Toolbench latency readings.

Workaround

Use the latency formula in the *Viterbi Compiler User Guide* for your calculations.

Solution Status

This issue will be fixed in the next release of the Viterbi Compiler.

The Traceback Length Values that IP Toolbench Sets May Be Inadequate

IP Toolbench sets the traceback length (`tb_length`) values in the `block_period_stim.txt` file. The values to this input are set to either $6 \times L$ or V whichever is lower, where L is the constraint length of the code and V is the traceback length. However, IP Toolbench does not take into consideration punctured data, so `tb_length` may be inadequate for the test.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact, this issue only impacts the quality of the test data when you run the decoder with punctured data.

Workaround

Edit the file `block_period_stim.txt` to set an adequate value for `tb_length` for running punctured data.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

Decimal & Octal Can Be Selected Simultaneously

In IP Toolbench on the Code Sets tab, you can select both **Decimal** and **Octal** or turn them both off, on Linux 64-bit computers.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can lead to a misconfiguration of the Viterbi decoder, by entering erroneous polynomials.

Workaround

Select **Octal** and then select **Decimal** to leave only **Octal** selected.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history for Viterbi Compiler v4.3.0.

Version	Date	Errata Summary
1.3	February 2006	Added "Incorrect Behavior of numerr Signal" on page 1.
1.2	January 2006	Added the following issues: <ul style="list-style-type: none"> • "Multiple Constraint Lengths May Cause Trellis Termination Errors When Using tr_init_state" on page 2 • "Editing Some Hybrid Parameters Can Cause the Maximum Constraint Length and ACS Units to Show Incorrect Values in IP Toolbench" on page 3
1.1	November 2005	Added "Decimal & Octal Can Be Selected Simultaneously" on page 5.
1.0	October 2005	First release.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

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