

## Introduction

Arria™ GX devices support external memory interfaces, including DDR SDRAM, DDR2 SDRAM, and SDR SDRAM. Its dedicated phase-shift circuitry allows the Arria GX device to interface with an external memory at twice the system clock speed (up to 233 MHz/466 megabits per second (Mbps) with DDR2 SDRAM). In addition to external memory interfaces, you can also use the dedicated phase-shift circuitry for other applications that require a shifted input clock signal.

Most new memory architectures use a DDR I/O interface. Although Arria GX devices also support the mature and well established SDR external memory, this chapter focuses on DDR memory standards. These DDR memory standards cover a broad range of applications for embedded processor systems, image processing, storage, communications, and networking.

Arria GX devices offer external memory support in top and bottom I/O banks. [Figure 7-1](#) shows Arria GX device memory support.

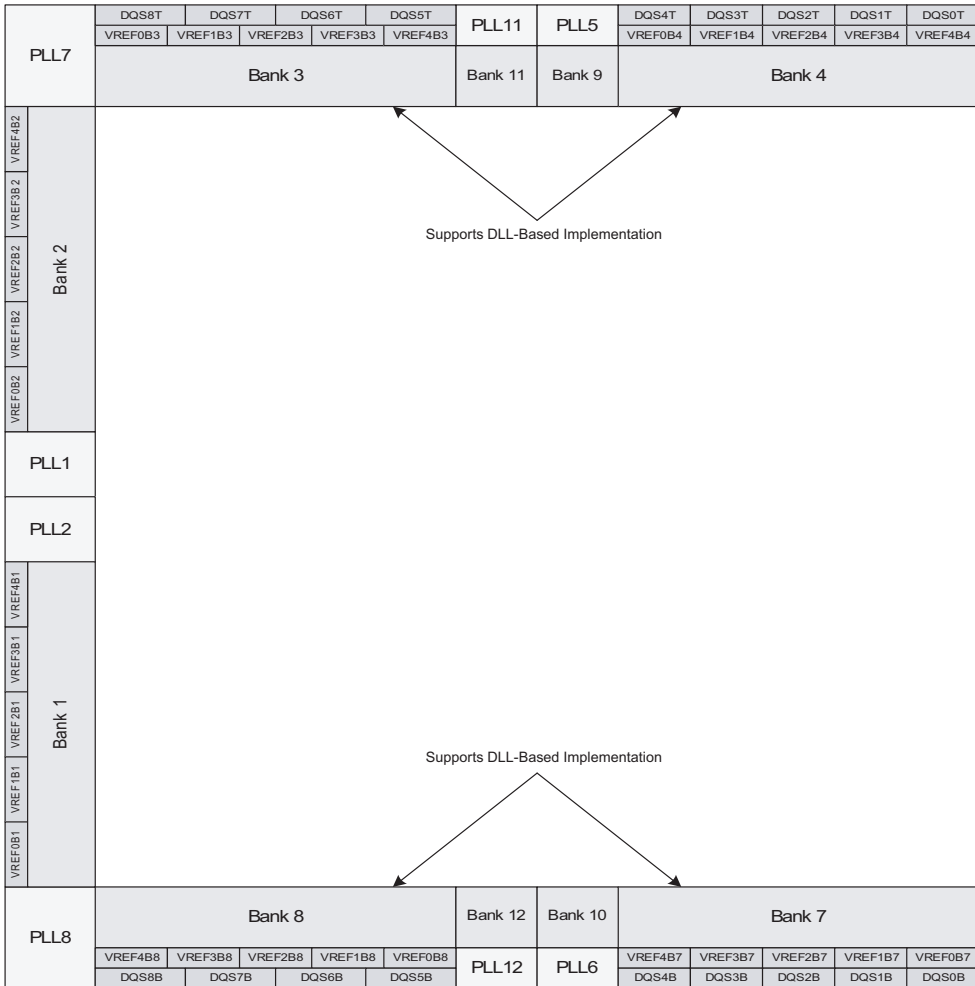


If your system requires memory interface support, you *must* use the ALTMEMPHY megafunction.

This chapter contains the following sections:

- [“External Memory Standards” on page 7-3](#)
- [“Arria GX DDR Memory Support Overview” on page 7-7](#)
- [“Conclusion” on page 7-26](#)

Figure 7–1. External Memory Support



Notes to Figure 7–1:

- (1) For more information about the ALTMEMPHY megafunction data path, refer to the *ALTMEMPHY Megafunction User Guide*.
- (2) EP1AGX20/35 and EP1AGX50/60 devices in the F484 package support external memory interfaces in the top I/O banks only.

Table 7–1 summarizes the maximum clock rate Arria GX devices support with external memory devices.

Memory Standards	–6 Speed Grade (MHz)
DDR2 SDRAM (3), (4)	233
DDR SDRAM (3), (4)	200

**Notes to Table 7–1:**

- (1) Memory interface timing specifications are dependent on the memory, board, physical interface, and core logic. Refer to each memory interface application note for more details about how each specification is generated.
- (2) Numbers are preliminary until characterization is final. The timing information featured in the Quartus® II software version 7.1 was used to define these clock rates.
- (3) This applies to interfaces with both modules and components.
- (4) These memory interfaces are supported using the ALTMEMPHY megafunction.

This chapter describes the hardware features in Arria GX devices that facilitate high-speed memory interfacing for each DDR memory standard.

## External Memory Standards

The following sections briefly describe external memory standards supported by Arria GX devices. Altera® offers a complete solution for these memories, including clear-text data path, memory controller, and timing analysis.

### DDR and DDR2 SDRAM

DDR SDRAM is a memory architecture that transmits and receives data at twice the clock speed. These devices transfer data on both the rising and falling edges of the clock signal. DDR2 SDRAM is a second-generation memory based on the DDR SDRAM architecture. It transfers data to Arria GX devices at up to 233 MHz/466 Mbps. Arria GX devices can support DDR SDRAM at up to 200 MHz/400 Mbps.

#### Interface Pins

DDR and DDR2 SDRAM devices use interface pins such as data (DQ), data strobe (DQS), clock, command, and address pins. Data is sent and captured at twice the system clock rate by transferring data on the clock's positive and negative edges. The commands and addresses still use only one active (positive) edge of a clock. DDR and DDR2 SDRAM use single-ended data strobes (DQS). DDR2 SDRAM can also use optional

differential data strobes (DQS and DQS#). However, Arria GX devices do not support the optional differential data strobes for DDR2 SDRAM interfaces. You can leave the DDR SDRAM memory DQS# pin unconnected. Only the shifted DQS signal from the DQS logic block is used to capture data.

DDR and DDR2 SDRAM  $\times 16$  devices use two DQS pins. Each DQS pin is associated with eight DQ pins. However, this is not the same as the  $\times 16/\times 18$  mode in Arria GX devices (see “[Data and Data Strobe Pins](#)” on [page 7–8](#)). To support a  $\times 16$  DDR2 SDRAM device, you need to configure Arria GX devices to use two sets of DQ pins in  $\times 8/\times 9$  mode. Similarly, if your  $\times 32$  memory device uses four DQS pins, where each DQS pin is associated with eight DQ pins, you need to configure the Arria GX devices to use four sets of DQS/DQ groups in  $\times 8/\times 9$  mode.

Connect the memory device’s DQ and DQS pins to Arria GX DQ and DQS pins, respectively, as listed in the Arria GX pin tables. DDR and DDR2 SDRAM also use active-high data mask, DM, and pins for writes. You can connect the memory’s DM pins to any of Arria GX I/O pins in the same bank as the DQ pins of the FPGA. There is one DM pin per DQS/DQ group in a DDR or DDR2 SDRAM device.

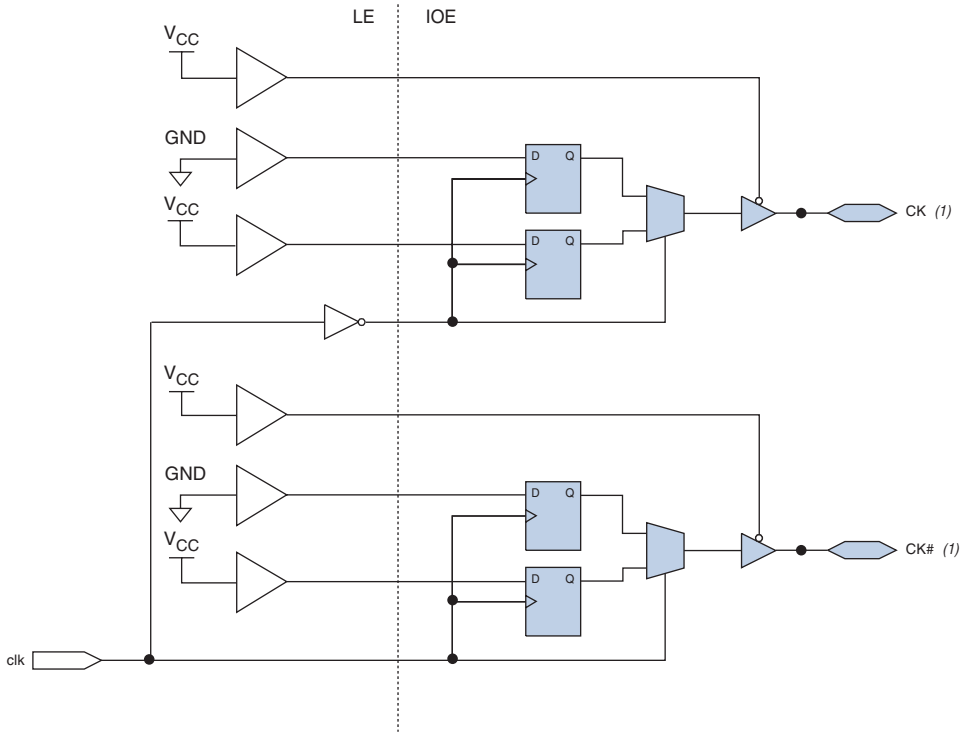


For more information about interfacing with DDR SDRAM, refer to [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#).

You can use any of the user I/O pins for commands and addresses to the DDR and DDR2 SDRAM. You may need to generate these signals from the system clock’s negative edge.

The clocks to the SDRAM device are called CK and CK# pins. Use any of the user I/O pins via the DDR registers to generate the CK and CK# signals to meet the DDR SDRAM or DDR2 SDRAM device’s  $t_{DQSS}$  requirement. The memory device’s  $t_{DQSS}$  specification requires that the write DQS signal’s positive edge must be within 25% of the positive edge of the DDR SDRAM or DDR2 SDRAM clock input. Using regular I/O pins for CK and CK# also ensures that any PVT variations on the DQS signals are tracked the same way by these CK and CK# pins. [Figure 7–2](#) shows a diagram that illustrates how to generate these clocks.

**Figure 7–2. Clock Generation for External Memory Interfaces in Arria GX Devices**



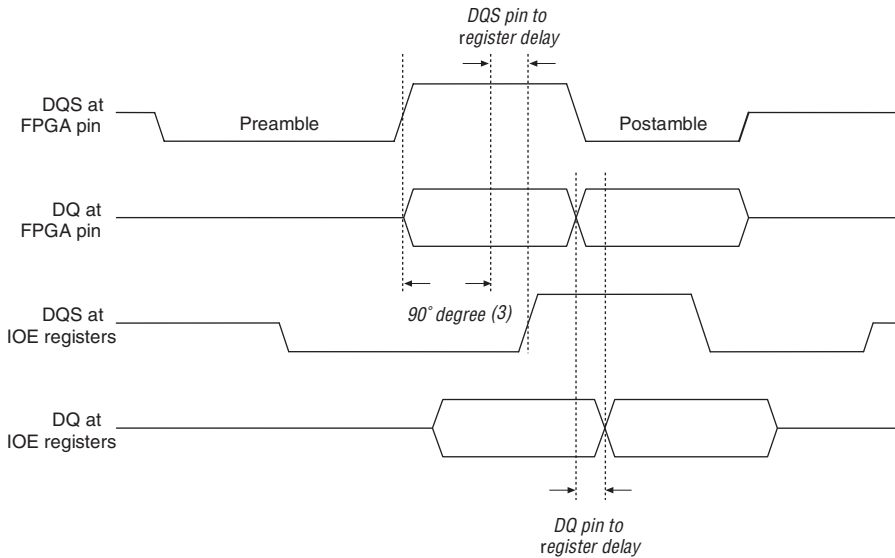
**Note to Figure 7–2:**

(1) CK and CK# are the clocks to the memory devices.

### Read and Write Operations

When reading from the memory, DDR and DDR2 SDRAM devices send the data edge-aligned with respect to the data strobe. To properly read the data in, the data strobe needs to be center-aligned with respect to the data inside the FPGA. Arria GX devices feature dedicated circuitry to shift this data strobe to the middle of the data window. Figure 7–3 shows an example of how the memory sends out the data and data strobe for a burst-of-two operation.

**Figure 7–3. Example of a 90° Shift on the DQS Signal** Notes (1), (2)

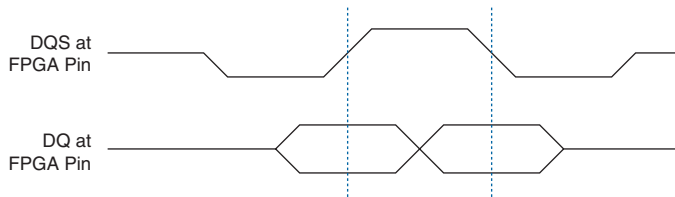


**Notes to Figure 7–3:**

- (1) DDR2 SDRAM does not support a burst length of two.
- (2) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA needs to send the data to the memory center-aligned with respect to the data strobe. Arria GX devices use a PLL to center-align the data by generating a 0° phase-shifted system clock for the write data strobes and a -90° phase-shifted write clock for the write data pins for DDR and DDR2 SDRAM. Figure 7–4 shows an example of the relationship between the data and data strobe during a burst-of-four write.

**Figure 7–4. DQ and DQS Relationship During a DDR and DDR2 SDRAM Write** Note (1)



**Note to Figure 7–4:**

- (1) This example shows a write for a burst length of two. DDR SDRAM devices do not support burst lengths of two.



For more information about DDR SDRAM and DDR2 SDRAM specifications, refer to the JEDEC standard publications JESD79C and JESD79-2, respectively, at [www.jedec.org](http://www.jedec.org).

## Arria GX DDR Memory Support Overview

This section describes Arria GX features that enable high-speed memory interfacing. It first describes Arria GX memory pins and then DQS phase-shift circuitry and DDR I/O registers. [Table 7-2](#) shows the I/O standard associated with the external memory interfaces.

<i>Table 7-2. External Memory Support in Arria GX Devices</i>	
Memory Standard	I/O Standard
DDR2 SDRAM	SSTL-18 Class II (1)
DDR SDRAM	SSTL-2 Class II

*Note to Table 7-2:*

- (1) Arria GX devices support 1.8-V HSTL/SSTL-18 Class I and II I/O standards in I/O banks 3, 4, 7, and 8.

Arria GX devices support data strobe or read clock signal (DQS) used in DDR SDRAM and DDR2 SDRAM devices with dedicated circuitry.



For more information about memory interfaces, see the appropriate Stratix II or Stratix II GX memory interfaces application note available at [www.altera.com](http://www.altera.com).

Arria GX devices contain dedicated circuitry to shift incoming DQS signals by 0°, 22.5°, 30°, 36°, 45°, 60°, 67.5°, 72°, 90°, 108°, 120°, or 144°, depending on the delay-locked loop (DLL) mode. There are four DLL modes. The DQS phase-shift circuitry uses a frequency reference to dynamically generate control signals for the delay chains in each of the DQS pins, allowing it to compensate for process, voltage, and temperature (PVT) variations. This phase-shift circuitry has been enhanced in Arria GX devices to support more phase-shift options with less jitter.

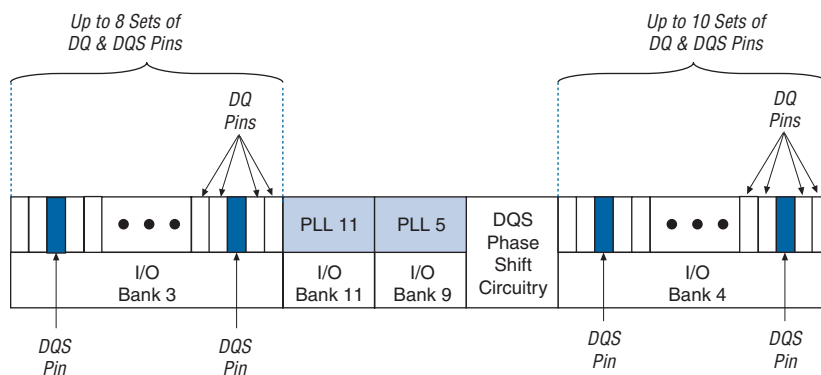
Besides DQS dedicated phase-shift circuitry, each DQS pin has its own DQS logic block that sets the delay for the signal input to the pin. Using DQS dedicated phase-shift circuitry with the DQS logic block allows for phase-shift fine-tuning. Additionally, every IOE in an Arria GX device contains six registers and one latch to achieve DDR operation.

## DDR Memory Interface Pins

Arria GX devices use data (DQ), data strobe (DQS), and clock pins to interface with external memory.

Figure 7–5 shows DQ and DQS pins in the Arria GX I/O banks on the top of the device. A similar arrangement is repeated at the bottom of the device.

**Figure 7–5. DQ and DQS Pins Per I/O Bank**



### Data and Data Strobe Pins

Arria GX data pins for DDR memory interfaces are called DQ pins. Arria GX devices can use either bidirectional data strobes or unidirectional read clocks. Depending on the external memory interface, either the memory device's read data strobes or read clocks feed the Arria GX DQS pins.

Arria GX DQS pins connect to the DQS pins in DDR and DDR2 SDRAM interfaces. In every Arria GX device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR memory up to 233 MHz/466 Mbps (with DDR2). These I/O banks support DQS signals with DQ bus modes of  $\times 4$ ,  $\times 8/\times 9$ ,  $\times 16/\times 18$ , or  $\times 32/\times 36$ .

In  $\times 4$  mode, each DQS pin drives up to four DQ pins within that group. In  $\times 8/\times 9$  mode, each DQS pin drives up to nine DQ pins within that group to support one parity bit and eight data bits. If the parity bit is not used, you can use the extra DQ pins as regular user I/O pins. Similarly, with  $\times 16/\times 18$  and  $\times 32/\times 36$  modes, each DQS pin drives up to 18 and 36 DQ pins, respectively. There are two parity bits in the

×16/×18 mode and four parity bits in the ×32/×36 mode. Table 7-3 shows the number of DQS/DQ groups supported in each Arria GX package for DLL-based implementations.

**Table 7-3. Arria GX DQS and DQ Bus Mode Support Note (1)**

Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
484-pin FineLine BGA	2	0	0	0
780-pin FineLine BGA	18	8	4	0
1,152-pin FineLine BGA	36	18	8	4

**Note to Table 7-3:**

- (1) Check the pin table for each DQS/DQ group in the different modes.

The DQS pins are listed in the Arria GX pin tables as DQS [17 . . 0] T or DQS [17 . . 0] B. The T denotes pins on the top of the device; the B denotes pins on the bottom of the device. Corresponding DQ pins are marked as DQ [17 . . 0]. The numbering scheme starts from right to left on the package bottom view. When not used as DQ or DQS pins, these pins are available as regular I/O pins. Figure 7-6 shows the DQS pins in Arria GX I/O banks.

**Figure 7-6. DQS Pins in Arria GX I/O Banks Note (1), (2)**

**Top I/O Banks**

DQS17T	DQS16T	DQS15T	• • •	DQS10T	PLL 11	PLL 5	DQS Phase Shift Circuitry	DQS9T	DQS8T	• • •	DQS0T
I/O Bank 3				I/O Bank 11	I/O Bank 9	I/O Bank 4					

**Bottom I/O Banks**

I/O Bank 8				I/O Bank 12	I/O Bank 10	DQS Phase Shift Circuitry	I/O Bank 7			
DQS17B	DQS16B	DQS15B	• • •	DQS10B	PLL 12		PLL 6	DQS9B	DQS8B	• • •

**Notes to Figure 7-6:**

- (1) There are up to 18 pairs of DQS pins on both the top and bottom of the device.
- (2) See Table 7-3 for DQS bus mode support based on the package.

The DQ pin numbering is based on  $\times 4$  mode. There are up to eight DQS/DQ groups in  $\times 4$  mode in I/O banks 3 and 8 and up to 10 DQS/DQ groups in  $\times 4$  mode in I/O banks 4 and 7. In  $\times 8/\times 9$  mode, two adjacent  $\times 4$  DQS/DQ groups plus one parity pin are combined; one DQS pin from the combined groups can drive all the DQ and parity pins. Since there is an even number of DQS/DQ groups in an I/O bank, combining groups is efficient. Similarly, in  $\times 16/\times 18$  mode, four adjacent  $\times 4$  DQS/DQ groups plus two parity pins are combined and one DQS pin from the combined groups can drive all the DQ and parity pins. In  $\times 32/\times 36$  mode, eight adjacent DQS/DQ groups are combined and one DQS pin can drive all the DQ and parity pins in the combined groups.



On the top and bottom side of the device, the DQ and DQS pins must be configured as bidirectional DDR pins to enable the DQS phase-shift circuitry. You must use the `ALTMEMPHY` megafunction to configure the DQ and DQS paths, respectively.

### *Clock Pins*

You can use any of the DDR I/O registers to generate clocks to the memory device. For better performance, use the same I/O bank as the data and address and command pins.

### *Address and Command Pins*

You can use any of the user I/O pins in the top or bottom bank of the device for addresses and commands. For better performance, use the same I/O bank as the data pins.

### *Other Pins (Parity, DM Pins)*

You can use any of the DQ pins for parity pins in Arria GX devices. The Arria GX device family has support for parity in  $\times 8/\times 9$ ,  $\times 16/\times 18$ , and  $\times 32/\times 36$  mode. There is one parity bit available per eight bits of data pins.

The data mask and DM pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pins indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. You can use any I/O pins in the same bank as the DQ pins for DM signals. Each group of DQS and DQ signals in DDR and DDR2 SDRAM devices requires a DM pin. The DDR I/O output registers, clocked by the  $-90^\circ$  shifted clock, creates the DM signals, similar to DQ output signals.

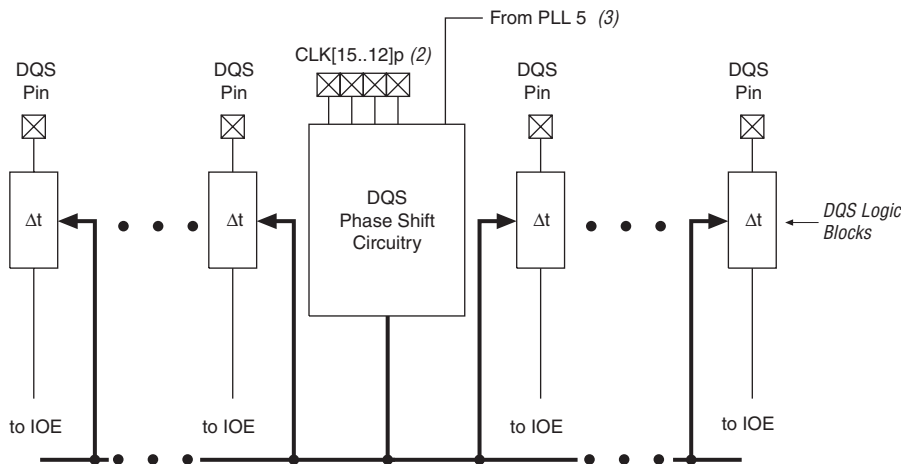


Perform timing analysis to calculate write clock phase shift.

## DQS Phase-Shift Circuitry

Arria GX phase-shift circuitry and DQS logic block controls the DQS pins. Each Arria GX device contains two phase-shifting circuits. There is one circuit for I/O banks 3 and 4 and another circuit for I/O banks 7 and 8. The phase-shifting circuit on the top of the device can control all the DQS pins in the top I/O banks; the phase-shifting circuit on the bottom of the device can control all the DQS pins in the bottom I/O banks. Figure 7-7 shows DQS pin connections to the DQS logic block and DQS phase-shift circuitry.

Figure 7-7. DQS Pins and DQS Phase-Shift Circuitry Note (1)

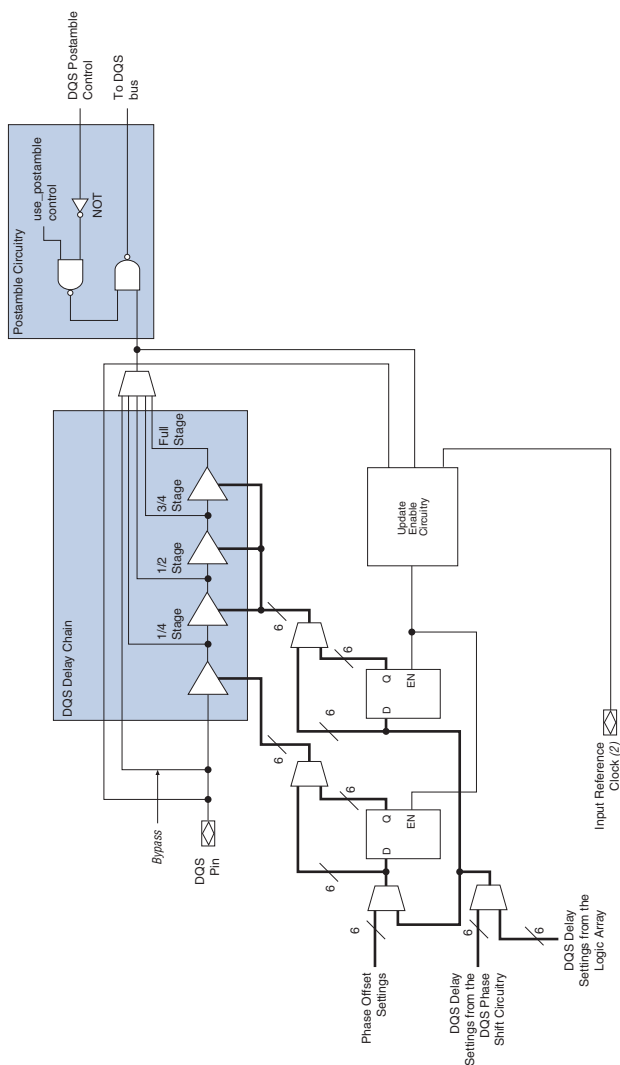


### Notes to Figure 7-7:

- (1) There are up to 18 pairs of DQS pins available on the top or bottom of the Arria GX device, up to eight on the left side of the DQS phase-shift circuitry (I/O banks 3 and 8) and up to ten on the right side (I/O banks 4 and 7).
- (2) Clock pins CLK [15 . . 12] p feed the phase-shift circuitry on the top of the device; clock pins CLK [7 . . 4] p feed the phase-shift circuitry on the bottom of the device. You can also use a phase-locked loop (PLL) clock output as a reference clock to the phase-shift circuitry. You can also use the reference clock in the logic array.
- (3) You can only use PLL 5 to feed DQS phase-shift circuitry on the top of the device and PLL 6 to feed DQS phase-shift circuitry on the bottom of the device.

Figure 7-8 shows the connections between the DQS phase-shift circuitry and the DQS logic block.

Figure 7–8. DQS Phase-Shift Circuitry and DQS Logic Block Connections *Note (1)*



**Notes to Figure 7–8:**

- (1) All features of the DQS phase-shift circuitry and DQS logic block are controlled from the ALTMEMPHY megafunction in the Quartus II software.
- (2) DQS logic block is available on every DQS pin.
- (3) There is one DQS phase-shift circuit on the top and bottom side of the device.
- (4) The input reference clock can come from CLK [15 . . 12] p or PLL 5 for the DQS phase-shift circuitry on the top side of the device or from CLK [7 . . 4] p or PLL 6 for the DQS phase-shift circuitry on the bottom side of the device.
- (5) Each individual DQS pin can have individual DQS delay settings to and from the logic array.
- (6) This register is one of the DQS IOE input registers.

Phase-shift circuitry is only used during read transactions where the DQS pins are acting as input clocks or strobes. Phase-shift circuitry can shift the incoming DQS signal by 0°, 22.5°, 30°, 36°, 45°, 60°, 67.5°, 72°, 90°, 108°, 120°, or 144°. The shifted DQS signal is then used as clocks at the DQ IOE input registers.

Figure 7-3 on page 7-6 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the DQS phase-shift circuitry and the DQS logic block and some routing delay from the DQS pin to the DQ IOE registers. DQ signals only goes through routing delay from the DQ pin to the DQ IOE registers and maintains the 90° relationship between the DQS and DQ signals at the DQ IOE registers since the software automatically sets delay chains to match the routing delay between the pins and the IOE registers for the DQ and DQS input paths.

All 18 DQS pins on either the top or bottom of the device can have their input signal phase shifted by a different degree amount but all must be referenced at one particular frequency. For example, you can have a 90° phase shift on DQS0T and have a 60° phase shift on DQS1T, both referenced from a 200-MHz clock. Not all phase-shift combinations are supported, however. The phase shifts on the same side of the device must all be a multiple of 22.5° (up to 90°), a multiple of 30° (up to 120°), or a multiple of 36° (up to 144°).

In order to generate the correct phase shift with the DLL used, you must provide a clock signal of the same frequency as the DQS signal to the DQS phase-shift circuitry. Any of the CLK[15..12]p clock pins can feed the phase circuitry on the top of the device (I/O banks 3 and 4) or any of the CLK[7..4]p clock pins can feed the phase circuitry on the bottom of the device (I/O banks 7 and 8). Arria GX devices can also use PLLs 5 or 6 as the reference clock to the DQS phase-shift circuitry on the top or bottom of the device, respectively. PLL 5 is connected to the DQS phase-shift circuitry on the top side of the device; PLL 6 is connected to the DQS phase-shift circuitry on the bottom side of the device. Both the top and bottom phase-shift circuits need unique clock pins or PLL clock outputs for the reference clock.



When you have a PLL dedicated only to generate the DLL input reference clock, you must set the PLL mode to **No Compensation** or the Quartus II software will change the setting automatically. Because there are no other PLL outputs used, the PLL does not need to compensate for any clock paths.

## DLL

DQS phase-shift circuitry uses a delay-locked loop (DLL) to dynamically measure the clock period needed by the DQS pin (see [Figure 7-8](#)). DQS phase-shift circuitry then uses the clock period to generate the correct phase shift. The DLL in the Arria GX DQS phase-shift circuitry can operate between 100 and 233 MHz. Phase-shift circuitry needs a maximum of 256 clock cycles to calculate the correct input clock period. Data sent during these clock cycles may not be properly captured.



Although the DLL can run up to 233 MHz, other factors may prevent you from interfacing with a 233-MHz external memory device.



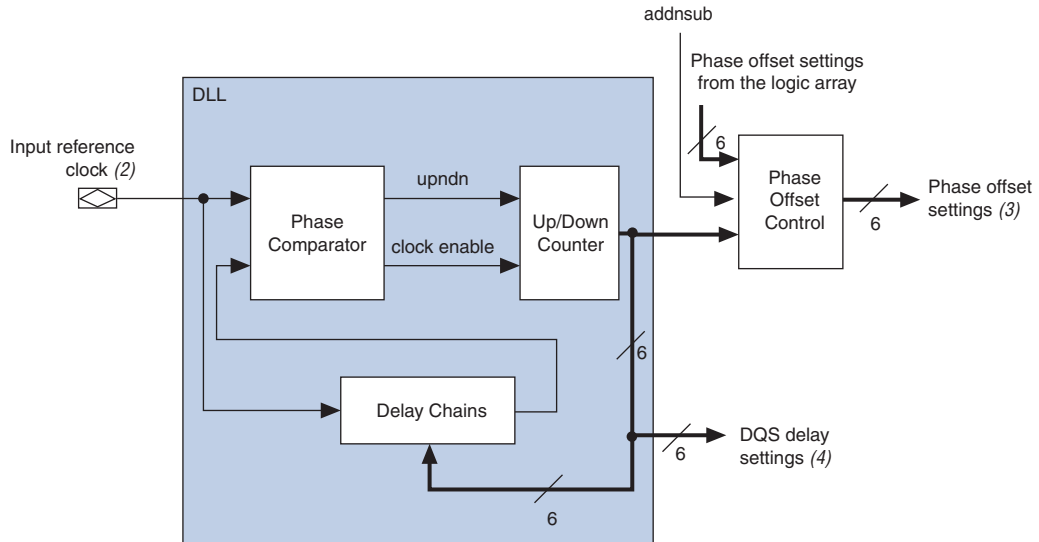
You can still use DQS phase-shift circuitry for any memory interfaces that are less than 100 MHz. The DQS signal is shifted by 2.5 ns. You can add more shift by using the phase offset module. Even if the DQS signal is not shifted exactly to the middle of the DQ valid window, the IOE is still able to capture the data in this low frequency application.

There are three different frequency modes for the Arria GX DLL. Each frequency mode provides different phase shift, as shown in [Table 7-4](#).

Frequency Mode	Frequency Range (MHz)	Available Phase Shift	Number of Delay Chains
0	100–175	30, 60, 90, 120	12
1	150–230	22.5, 45, 67.5, 90	16
2	200–310	30, 60, 90, 120	12

In frequency mode 0, Arria GX devices use a 6-bit setting to implement phase-shift delay. In frequency modes 1 and 2, Arria GX devices only use a 5-bit setting to implement phase-shift delay.

You can reset the DLL from either the logic array or a user I/O pin. This signal is not shown in [Figure 7-9](#). Each time the DLL is reset, you must wait for 256 clock cycles before you can capture the data properly. Additionally, if the DLL reference clock is stopped and restarted thereafter, such as during SDRAM refresh cycles, a minimum of 16 clock cycles is needed before capturing data properly.

**Figure 7–9. Simplified Diagram of the DQS Phase-Shift Circuitry** *Note (1)***Notes to Figure 7–9:**

- (1) All features of the DQS phase-shift circuitry are accessible from the ALTMEMPHY megafunction in the Quartus II software.
- (2) The input reference clock for DQS phase-shift circuitry on the top side of the device can come from CLK [15 . . 12] p or PLL 5. The input reference clock for DQS phase-shift circuitry on the bottom side of the device can come from CLK [7 . . 4] p or PLL 6.
- (3) Phase offset settings can only go to DQS logic blocks.
- (4) DQS delay settings can go to the logic array and/or the DQS logic block.

The input reference clock goes into the DLL to a chain of up to 16 delay elements. The phase comparator compares the signal coming out of the end of the delay element chain to the input reference clock. The phase comparator then issues the up/ndn signal to the up/down counter. This signal increments or decrements a 6-bit delay setting (DQS delay settings) that increases or decreases the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

DQS delay settings contain control bits to shift the signal on the input DQS pin by the amount set in the ALTMEMPHY megafunction. For 0 shift, both the DLL and DQS logic blocks are bypassed. Since Arria GX DQS and DQ pins are designed such that the pin-to-IOE delays are matched, the skew between the DQ and DQS pins at the DQ IOE registers is negligible when you implement 0 shift. You can feed the DQS delay settings to the DQS logic block and logic array.

### *Phase Offset Control*

DQS phase-shift circuitry also contains a phase offset control module that can add or subtract a phase offset amount from the DQS delay setting (phase offset settings from the logic array in [Figure 7-10](#)). You should use the phase offset control module for making small shifts to the input signal and use the DQS phase-shift circuitry for larger signal shifts.

You can either use a static phase offset or a dynamic phase offset to implement the additional phase shift. The available additional phase shift is implemented in 2s-complement between settings -64 to +63 for frequency mode 0 and between settings -32 to +31 for frequency modes 1, 2, and 3.



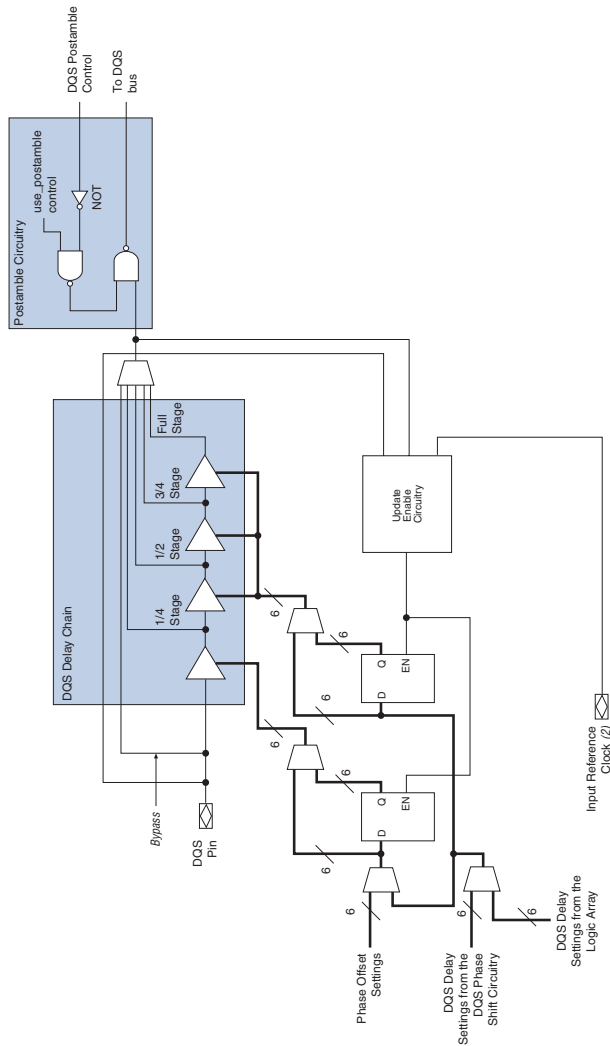
For more information about the value for each step, refer to the [DC & Switching Characteristics](#) chapter in volume 1 of the *Arria GX Device Handbook*. If you need one additional degree phase shift, you must convert the delay amount to degrees in the operating frequency.

When using the static phase offset, you can specify the phase offset amount in the ALTMEMPHY megafunction as a positive number for addition or a negative number for subtraction. You can also have a dynamic phase offset that is always added to, subtracted from, or both added to and subtracted from the DLL phase shift. When you always add or subtract, you can dynamically input the phase offset amount into the `dll_offset [5..0]` port. When you want to both add and subtract dynamically, you control the `addnsub` signal in addition to the `dll_offset [5..0]` signals.

### **DQS Logic Block**

Each DQS pin is connected to a separate DQS logic block (see [Figure 7-10](#)). The logic block contains DQS delay chains and postamble circuitry.

Figure 7-10. Simplified Diagram of the DQS Logic Block Note (1)



## Notes to Figure 7-10:

- (1) All features of the DQS logic block are controllable from the ALTMEMPHY megafunction in the Quartus II software.
- (2) The input reference clock for DQS phase-shift circuitry on the top side of the device can come from CLK [15 . . 12] p or PLL 5. The input reference clock for DQS phase-shift circuitry on the top side of the device can come from CLK [7 . . 4] p or PLL 6.
- (3) This register is one of the DQS IOE input registers.

### DQS Delay Chains

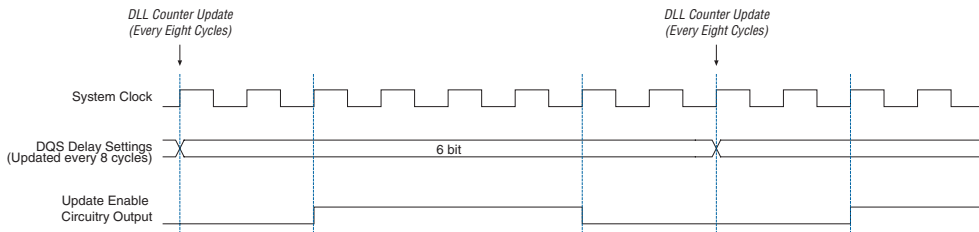
DQS delay chains consist of a set of variable delay elements to allow the input DQS signals to be shifted by the amount given by the DQS phase-shift circuitry or the logic array. There are four delay elements in the DQS delay chain; the first delay chain closest to the DQS pin can either be shifted by the DQS delay settings or by the sum of the DQS delay setting and the phase-offset setting. The number of delay chains used is transparent to the users because the ALTMEMPHY megafunction automatically sets it. DQS delay settings can come from DQS phase-shift circuitry on the same side of the device as the target DQS logic block or from the logic array. When you apply a 0° shift in the ALTMEMPHY megafunction, DQS delay chains are bypassed.

The delay elements in the DQS logic block mimic the delay elements in the DLL. The amount of delay is equal to the sum of the delay element's intrinsic delay and the product of the number of delay steps and the value of the delay steps.

Both the DQS delay settings and the phase-offset settings pass through a latch before going into the DQS delay chains. The latches are controlled by the update enable circuitry to allow enough time for any changes in the DQS delay setting bits to arrive to all the delay elements. This allows them to be adjusted at the same time. The update enable circuitry enables the latch to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry to all the DQS logic blocks before the next change. It uses the input reference clock to generate the update enable output. The ALTMEMPHY megafunction uses this circuit by default. See [Figure 7-11](#) for an example waveform of the update enable circuitry output.

The shifted DQS signal then goes to the DQS bus to clock the IOE input registers of the DQ pins. It can also go into the logic array for resynchronization purposes.

**Figure 7-11. DQS Update Enable Waveform**



### *DQS Postamble Circuitry*

For external memory interfaces that use a bidirectional read strobe like DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from a high-impedance state. See [Figure 7-3 on page 7-6](#). The state where DQS is low, just after a high-impedance state, is called the preamble; the state where DQS is low, just before it returns to a high-impedance state, is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. DQS postamble circuitry ensures data is not lost when there is noise on the DQS line at the end of a read postamble time. It is to be used with one of the DQS IOE input registers such that the DQS postamble control signal can ground the shifted DQS signal used to clock the DQ input registers at the end of a read operation. This ensures that any glitches on the DQS input signals at the end of the read postamble time do not affect the DQ IOE registers.

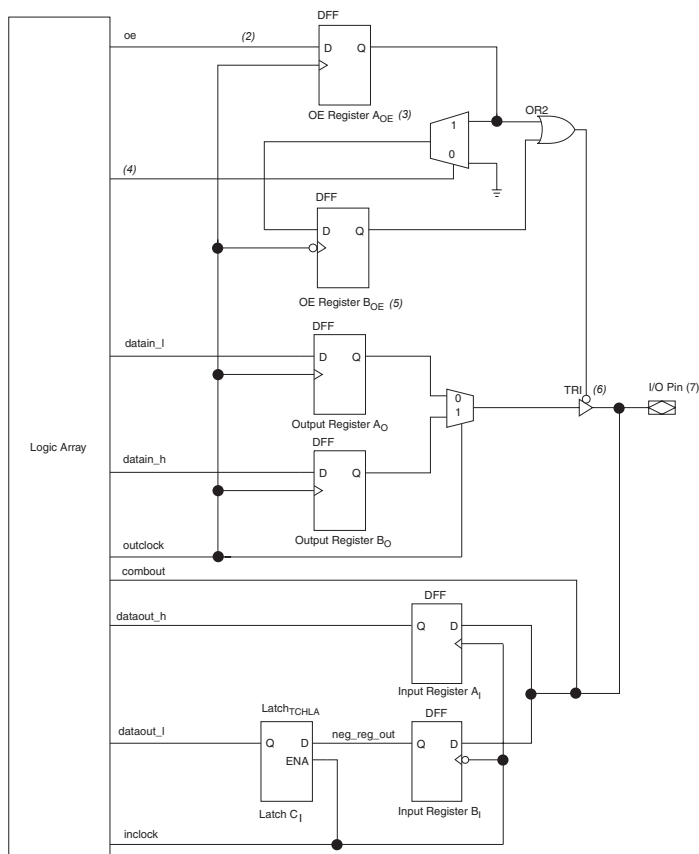


For more information about DDR SDRAM and DDR2 SDRAM, refer to [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#).

### **DDR Registers**

Each IOE in an Arria GX device contains six registers and one latch. Two registers and a latch are used for input, two registers are used for output, and two registers are used for output enable control. The second output enable register provides the write preamble for the DQS strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by a half clock cycle to provide the external memory's DQS write preamble time specification. [Figure 7-12](#) shows the six registers and the latch in the Arria GX IOE. [Figure 7-13](#) shows how the second OE register extends the DQS high-impedance state by half a clock cycle during a write operation.

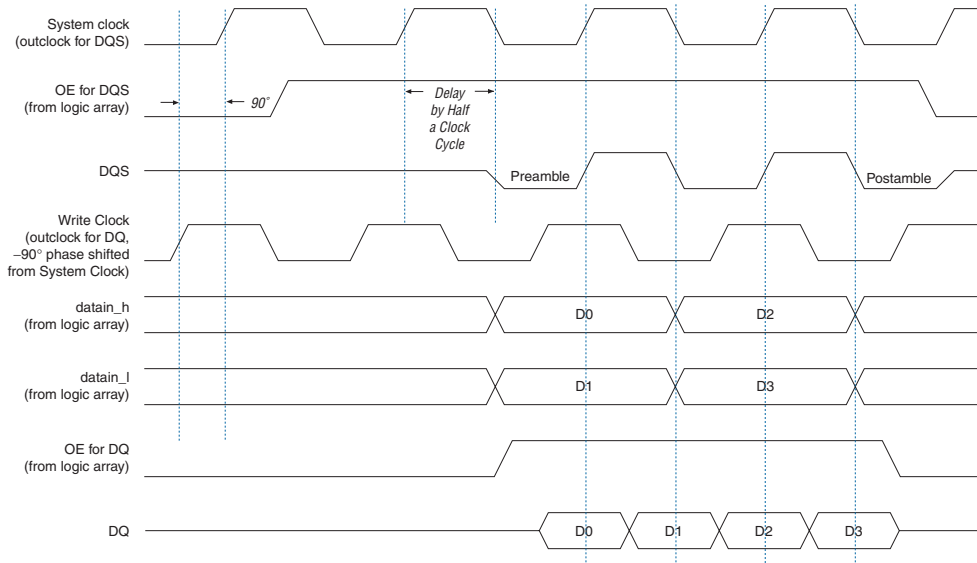
Figure 7–12. Bidirectional DDR I/O Path in Arria GX Devices *Note (1)*



Notes to Figure 7–12:

- (1) All control signals can be inverted at the IOE. The signal names used here match the Quartus II software naming convention.
- (2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before input to the A<sub>OE</sub> register during compilation.
- (3) The A<sub>OE</sub> register generates the enable signal for general-purpose DDR I/O applications.
- (4) This select line is to choose whether the OE signal should be delayed by half-a-clock cycle.
- (5) The B<sub>OE</sub> register generates the delayed enable signal for the write strobes or write clocks for memory interfaces.
- (6) The tri-state enable is active low by default. However, you can design it to be active high. The combinational control path for the tri-state is not shown in this diagram.
- (7) You can also have combinational output to the I/O pin; this path is not shown in the diagram.
- (8) On the top and bottom I/O banks, the clock to this register can be an inverted register A's clock or a separate clock (inverted or non-inverted).

**Figure 7–13. Extending the OE Disable by Half-a-Clock Cycle for a Write Transaction *Note (1)***

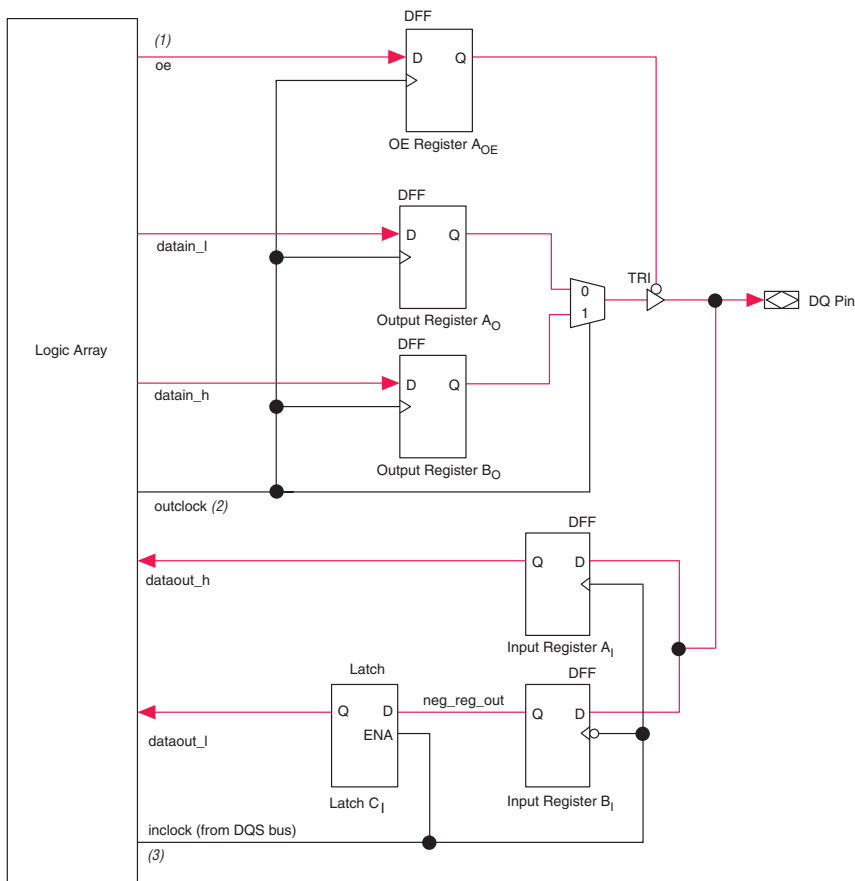


**Note to Figure 7–13:**

- (1) This waveform reflects the software simulation result. The OE signal is active low on the device. However, the Quartus II software implements this signal as active high and automatically adds an inverter before the A<sub>OE</sub> register D input.

Figures 7-14 and 7-15 summarize the IOE registers used for the DQ and DQS signals.

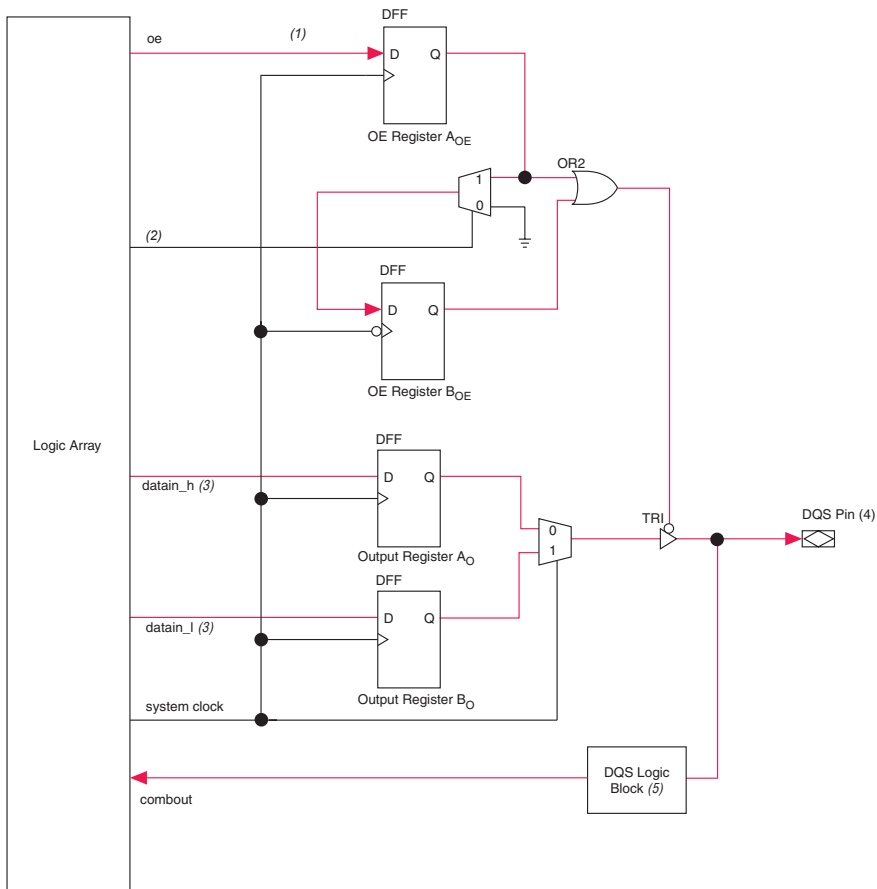
Figure 7-14. DQ Configuration in Arria GX IOE Note (1)



Notes to Figure 7-14:

- (1) You should use the ALTMEMPHY megafunction to generate the data path for your memory interface.
- (2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before the OE register A<sub>OE</sub> during compilation.
- (3) The outclock signal for DDR and DDR2 SDRAM interfaces has a 90° phase-shift relationship with the system clock. The shifted DQS signal can clock this register.
- (4) The shifted DQS signal must be inverted before going to the DQ IOE. The inversion is automatic if you use the ALTMEMPHY megafunction to generate the DQ signals.
- (5) On the top and bottom I/O banks, the clock to this register can be an inverted register A's clock or a separate clock (inverted or non-inverted).

Figure 7–15. DQS Configuration in Arria GX IOE Note (1)



## Notes to Figure 7–15:

- (1) Use the ALTMEMPHY megafunction to generate the data path for your memory interface.
- (2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before OE register A<sub>OE</sub> during compilation.
- (3) The select line can be chosen in the ALTMEMPHY megafunction.
- (4) The datain\_l and datain\_h pins are usually connected to ground and V<sub>CC</sub>, respectively.
- (5) DQS postamble circuitry and handling is not shown in this diagram. For more information, refer to [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#).
- (6) DQS logic blocks are only available with DQS pins.
- (7) You must invert this signal before it reaches the DQ IOE. This signal is automatically inverted if you use the ALTMEMPHY megafunction to generate the DQ signals.

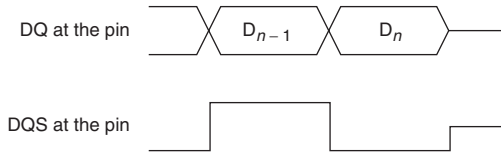
For interfaces to DDR SDRAM and DDR2 SDRAM, the Arria GX DDR IOE structure requires you to invert the incoming DQS signal to ensure proper data transfer. By default, the ALTMEMPHY megafunction adds the inverter to the `inclock` port when it generates DQ blocks. As shown in [Figure 7–12 on page 7–20](#), the `inclock` signal's rising edge clocks the  $A_1$  register, `inclock` signal's falling edge clocks the  $B_1$  register, and latch  $C_1$  is opened when `inclock` is 1. In a DDR memory read operation, the last data coincides with DQS being low. If you do not invert the DQS pin, you will not get this last data as the latch does not open until the next rising edge of the DQS signal.

[Figure 7–16](#) shows waveforms of the circuit shown in [Figure 7–14 on page 7–22](#).

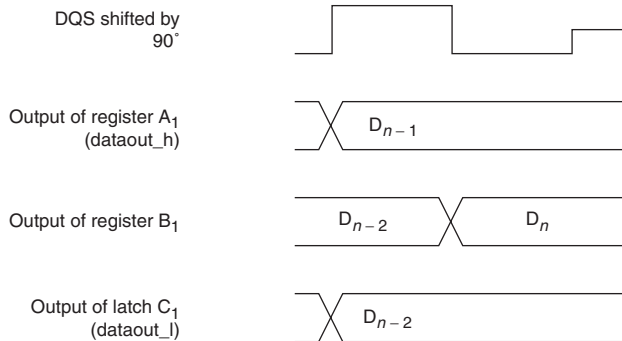
The first set of waveforms in [Figure 7–16](#) shows the edge-aligned relationship between the DQ and DQS signals at the Arria GX device pins. The second set of waveforms in [Figure 7–16](#) shows what happens if the shifted DQS signal is not inverted; the last data,  $D_n$ , does not get latched into the logic array as DQS goes to tri-state after the read postamble time. The third set of waveforms in [Figure 7–16](#) shows a proper read operation with the DQS signal inverted after the 90° shift; the last data,  $D_n$ , does get latched. In this case the outputs of register  $A_1$  and latch  $C_1$ , which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register  $A_1$ , register  $B_1$ , and latch  $C_1$  refer to the nomenclature in [Figure 7–14 on page 7–22](#).

**Figure 7-16. DQ Captures with Non-Inverted and Inverted Shifted DQS**

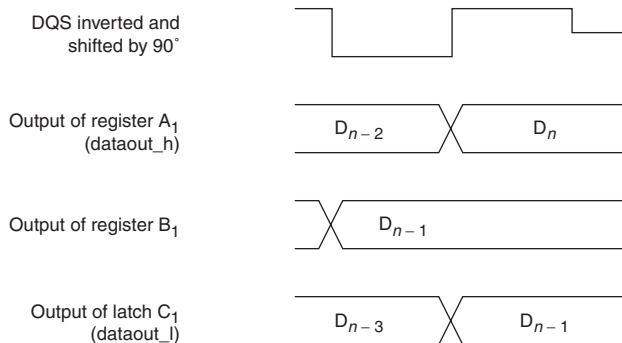
**DQ & DQS Signals**



**Shifted DQS Signal is Not Inverted**



**Shifted DQS Signal is Inverted**



## PLL

When using the Arria GX top and bottom I/O banks (I/O banks 3, 4, 7, or 8) to interface with a DDR memory, at least one PLL with two outputs is needed to generate the system clock and write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock is either shifted by  $-90^\circ$  or  $90^\circ$  from the system clock and is used to generate the DQ signals during writes.

For DDR and DDR2 SDRAM interfaces above 200 MHz, Altera also recommends a second read PLL to help ease resynchronization.

## Conclusion

Arria GX devices support SDR SDRAM, DDR SDRAM, and DDR2 SDRAM external memories. Arria GX devices feature high-speed interfaces that transfer data between external memory devices at up to 233 MHz/466 Mbps. DQS phase-shift circuitry and DQS logic blocks within Arria GX devices allow you to fine-tune the phase shifts for the input clocks or strobes to properly align clock edges as needed to capture data.

## Referenced Documents

This chapter references the following documents:

- [ALTMEMPHY Megafunction User Guide](#)
- [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#)
- [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#)
- [DC & Switching Characteristics](#) chapter in volume 1 of the *Arria GX Device Handbook*

## Document Revision History

Table 7–5 shows the revision history for this chapter.

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2008 v1.2	Updated the “DLL” section.	—
	Minor text edits.	—
August 2007 v1.1	Added the “Referenced Documents” section.	—
May 2007 v1.0	Initial Release	—