

This chapter describes the boundary-scan test (BST) features that are supported in Arria® II GX devices. The features are similar to Arria GX devices, unless stated in this document.

This chapter includes the following sections:

- “IEEE Std. 1149.6 Boundary-Scan Register” on page 11–2
- “BST Operation Control” on page 11–3
- “I/O Voltage Support in a JTAG Chain” on page 11–5
- “Boundary-Scan Description Language Support” on page 11–6

Arria II GX devices support IEEE Std. 1149.1 and IEEE Std. 1149.6. The IEEE Std. 1149.6 is only supported on the high-speed serial interface (HSSI) transceivers in Arria II GX devices. The IEEE Std. 1149.6 enables board-level connectivity checking between transmitters and receivers that are AC coupled (connected with a capacitor in series between the source and destination).

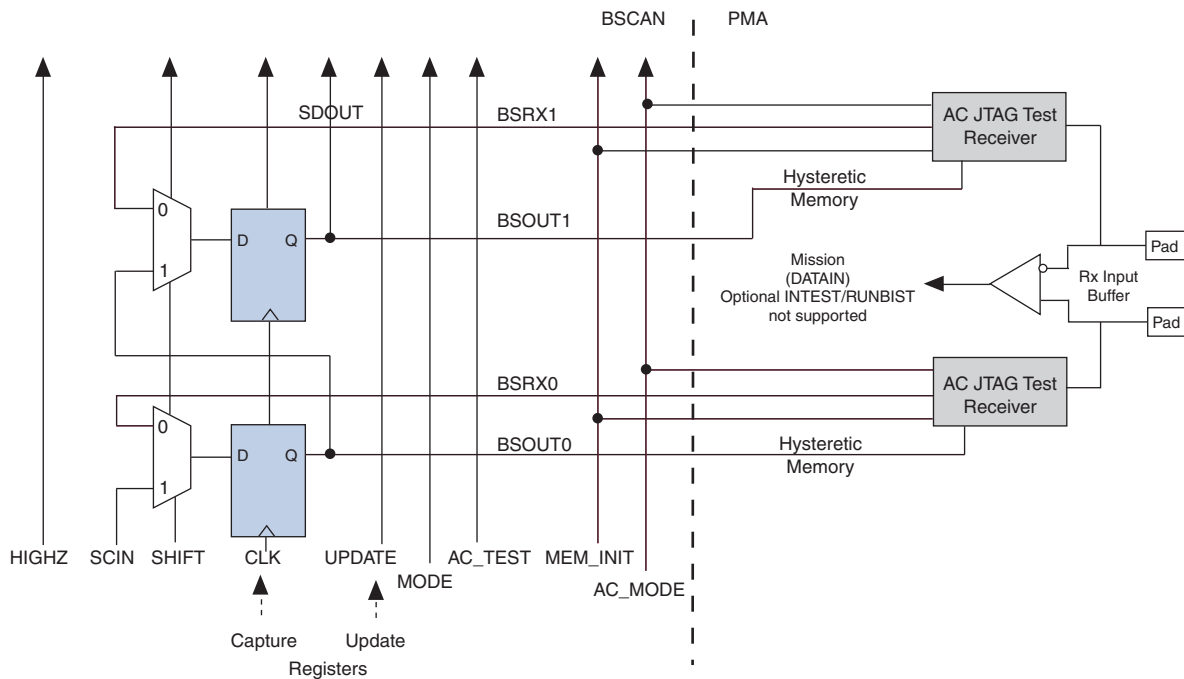


For information about the following topics, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Arria GX Devices* chapter:

- IEEE Std. 1149.1 BST architecture and circuitry
- TAP controller state-machine
- IEEE Std. 1149.1 JTAG instructions
- JTAG instructions code with descriptions
- IEEE Std. 1149.1 BST guidelines

Figure 11-2 shows the Arria II GX HSSI receiver/input clock buffer BSC.

Figure 11-2. Arria II GX HSSI Receiver/Input Clock Buffer BSC with IEEE Std. 1149.6 BST Circuitry



For information about Arria II GX user I/O boundary-scan cells, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Arria GX Devices* chapter.

BST Operation Control

Table 11-1 lists the boundary-scan register length for Arria II GX devices.

Table 11-1. Arria II GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2AGX45	1227
EP2AGX65	1227
EP2AGX95	1467
EP2AGX125	1467
EP2AGX190	1971
EP2AGX260	1971

Table 11-2 lists the IDCODE information for Arria II GX devices.

Table 11-2. 32-Bit Arria II GX Device IDCODE

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
EP2AGX45	0000	0010010100010010	000 0110 1110	1
EP2AGX65	0000	0010010100000010	000 0110 1110	1
EP2AGX95	0000	0010010100010011	000 0110 1110	1
EP2AGX125	0000	0010010100000011	000 0110 1110	1
EP2AGX190	0000	0010010100010100	000 0110 1110	1
EP2AGX260	0000	0010010100000100	000 0110 1110	1

Notes to Table 11-2:

- (1) The MSB is on the left.
 (2) The IDCODE LSB is always 1.



To read IDCODE correctly, issue the IDCODE instruction after initialization, which is signaled by nSTATUS going high.

IEEE Std.1149.6 mandates the addition of two new instructions: EXTEST_PULSE and EXTEST_TRAIN. These two instructions enable edge-detecting behavior on the signal path containing the AC pins.

EXTEST_PULSE

The instruction code for EXTEST_PULSE is 0010001111. The EXTEST_PULSE instruction generates three output transitions:

- Driver drives data on the falling edge of TCK in UPDATE_IR/DR.
- Driver drives inverted data on the falling edge of TCK after entering the RUN_TEST/IDLE state.
- Driver drives data on the falling edge of TCK after leaving the RUN_TEST/IDLE state.

EXTEST_TRAIN

The instruction code for EXTEST_TRAIN is 0001001111. The EXTEST_TRAIN instruction behaves the same as the EXTEST_PULSE instruction with one exception. The output continues to toggle on the TCK falling edge as long as the TAP controller is in the RUN_TEST/IDLE state.

I/O Voltage Support in a JTAG Chain

An Arria II GX device operating in BST mode uses four required pins: TDI, TDO, TMS, and TCK. The TDO output pin and all JTAG input pins are powered by the V_{CCIO} power supply of I/O Bank 8C.

The JTAG chain supports several devices. However, use caution if the chain contains devices that have different V_{CCIO} levels.


Table 11-3 shows board design recommendations to ensure proper JTAG chain operation.

Table 11-3. Supported TDO/TDI Voltage Combinations

Device	TDI Input Buffer Power	Arria II GX TDO V_{CCIO} Voltage Level in I/O Bank 8C				
		$V_{CCIO} = 3.3\text{ V}$	$V_{CCIO} = 3.0\text{ V}$	$V_{CCIO} = 2.5\text{ V}$	$V_{CCIO} = 1.8\text{ V}$	$V_{CCIO} = 1.5\text{ V}$
Arria II GX	$V_{CCIO} = 3.3\text{ V}$	✓ (1)	✓ (1)	✓ (2)	✓ (3)	Level shifter required
	$V_{CCIO} = 3.0\text{ V}$	✓ (1)	✓ (1)	✓ (2)	✓ (3)	Level shifter required
	$V_{CCIO} = 2.5\text{ V}$	✓ (1)	✓ (1)	✓ (2)	✓ (3)	Level shifter required
	$V_{CCIO} = 1.8\text{ V}$	✓ (1)	✓ (1)	✓ (2)	✓ (3)	Level shifter required
	$V_{CCIO} = 1.5\text{ V}$	✓ (1)	✓ (1)	✓ (2)	✓ (3)	✓
Non-Arria II GX	$V_{CC} = 3.3\text{ V}$	✓ (1)	✓ (1)	✓ (2)	✓ (3)	Level shifter required
	$V_{CC} = 2.5\text{ V}$	✓ (1), (4)	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required
	$V_{CC} = 1.8\text{ V}$	✓ (1), (4)	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required
	$V_{CC} = 1.5\text{ V}$	✓ (1), (4)	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓



Notes to Table 11-3:

- (1) The TDO output buffer meets $V_{OH}(\text{Min.}) = 2.4\text{ V}$.
- (2) The TDO output buffer meets $V_{OH}(\text{Min.}) = 2.0\text{ V}$.
- (3) An external 250- Ω pull-up resistor is not required; however, they are recommended if signal levels on the board are not optimal.
- (4) The input buffer must be 3.0-V tolerant.
- (5) The input buffer must be 2.5-V tolerant.
- (6) The input buffer must be 1.8-V tolerant.

 For more information about I/O voltage support in the JTAG chain, refer to the [IEEE 1149.1 \(JTAG\) Boundary-Scan Testing for Arria GX Devices](#).

Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.6 BST-capable device that can be tested. You can test software development systems then use the BSDL files for test generation, analysis, and failure diagnostics.

-  For more information about BSDL files for IEEE Std. 1149.6-compliant Arria II GX devices, refer to the [IEEE 1149.6 BSDL Files](#) page on the Altera website.
-  You can also generate BSDL files (pre-configuration and post-configuration) for IEEE Std. 1149.6-compliant Arria II GX devices with the Quartus® II software version 9.1 and later. For the procedure to generate BSDL files using the Quartus II software, refer to the [BSDL Files Generation in QII](#).

Revision History

[Table 11-4](#) lists the revision history for this chapter.

Table 11-4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009, v2.0	<ul style="list-style-type: none"> ■ Updated Table 11-1 and Table 11-2. ■ Updated “I/O Voltage Support in a JTAG Chain” section. ■ Minor text edits. 	Updated for Arria II GX v9.1 release.
February 2009, v 1.0	Initial release.	—