

This section discusses configuring configuration chains that contain a mixture of Altera® device families, combining different configuration schemes on your board and using a CPLD and flash memory to configure your Altera FPGA. It is recommended that you read the chapters in Volume I for your target device family before reading this section.

This section includes the following chapters:

- [Chapter 7, Combining Different Configuration Schemes](#)

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

This chapter describes how to configure Altera® FPGAs using multiple configuration schemes on the same board. Combining JTAG configuration with passive serial (PS) or active serial (AS) configuration on your board is useful in the prototyping environment because it allows multiple methods to configure your FPGA. For example, if your production environment calls for PS configuration using a configuration device, you must reprogram your configuration device every time you wanted to test a design change in your FPGA. If you include the FPGA in the same JTAG chain as the configuration device, the FPGA can be reconfigured via JTAG without having to reprogram the configuration device.

In this chapter, the generic term “download cable” includes the Altera USB Blaster universal serial bus (USB) port download cable, MasterBlaster™ serial/USB communications cable, EthernetBlaster, ByteBlaster™ II parallel port download cable, and the ByteBlasterMV™ parallel port download cable. In this section, the generic term “FPGA” includes ACEX® 1K, APEX™ 20K, APEX II, Arria® series, Cyclone® series, FLEX® 10K, Mercury™, and Stratix® series devices.



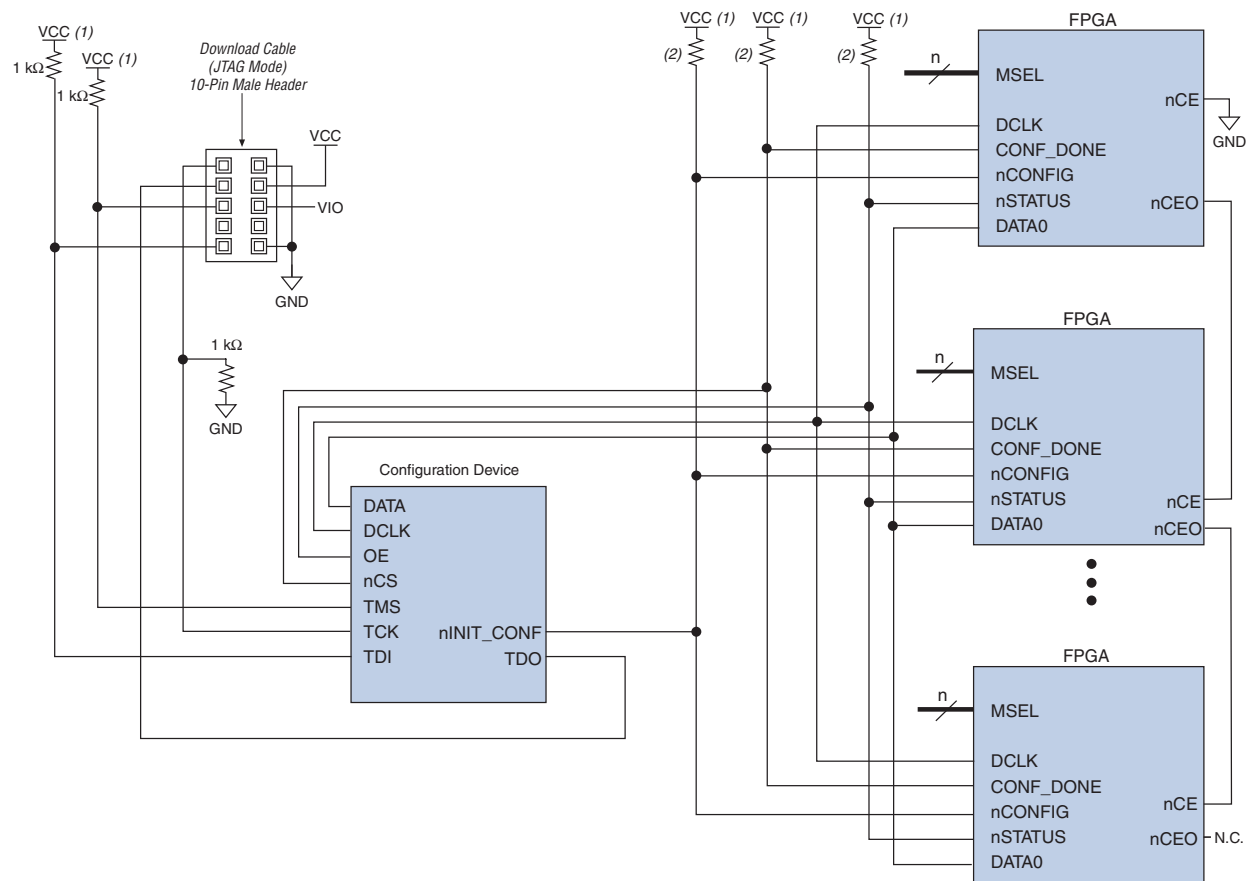
The figures in this chapter will only show the configuration interface connections.



For detailed information about pull-up resistor values or other pins on the specific FPGA or configuration device, refer to appropriate chapter in the *Configuration Handbook*.

Passive Serial and JTAG

[Figure 7-1](#) shows the configuration interface connections when you are using a download cable to JTAG program a configuration device and the configuration device is used to configure the FPGAs. In [Figure 7-1](#), multiple FPGAs are daisy-chained together and the MSEL pins should be set to select PS as the configuration mode.

Figure 7-1. JTAG Programming of Configuration Device with PS Configuration of FPGA Using a Configuration Device**Notes to Figure 7-1:**

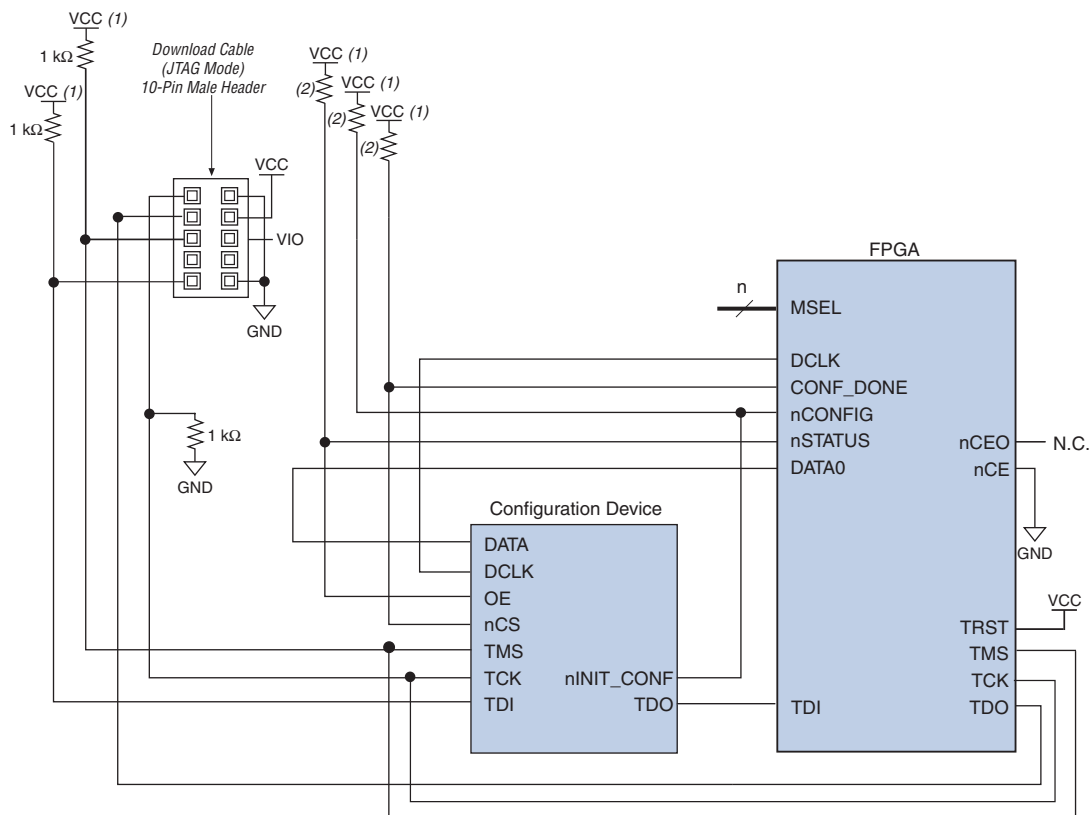
- (1) V_{CC} should be connected to the same supply voltage as the configuration device. For APEX 20KE devices, $nCONFIG$ should be pulled up to V_{CCINT} .
- (2) If the internal pull-up resistors of the configuration device are used, external pull-up resistors should not be used on these pins.

Figure 7-2 shows the configuration interface connections when the configuration device and the FPGA are in the same JTAG chain. Make sure the TDO signal drives out a high enough voltage to meet the next device's TDI minimum high-level input voltage (V_{IH}). The TDO output will drive out the voltage of the I/O bank's V_{CCIO} where it resides. For example, if the TDO pin resides in an I/O bank whose V_{CCIO} is set to 3.3 V, the TDO pin will drive out 3.3 V. The download cable is used to JTAG program the configuration device and the FPGA. The configuration device is used to configure the FPGA. The MSEL pins should be set to select PS as the configuration mode.



If there is a configuration device on board, upon power-up you should allow the FPGA to finish configuration before attempting JTAG configuration.

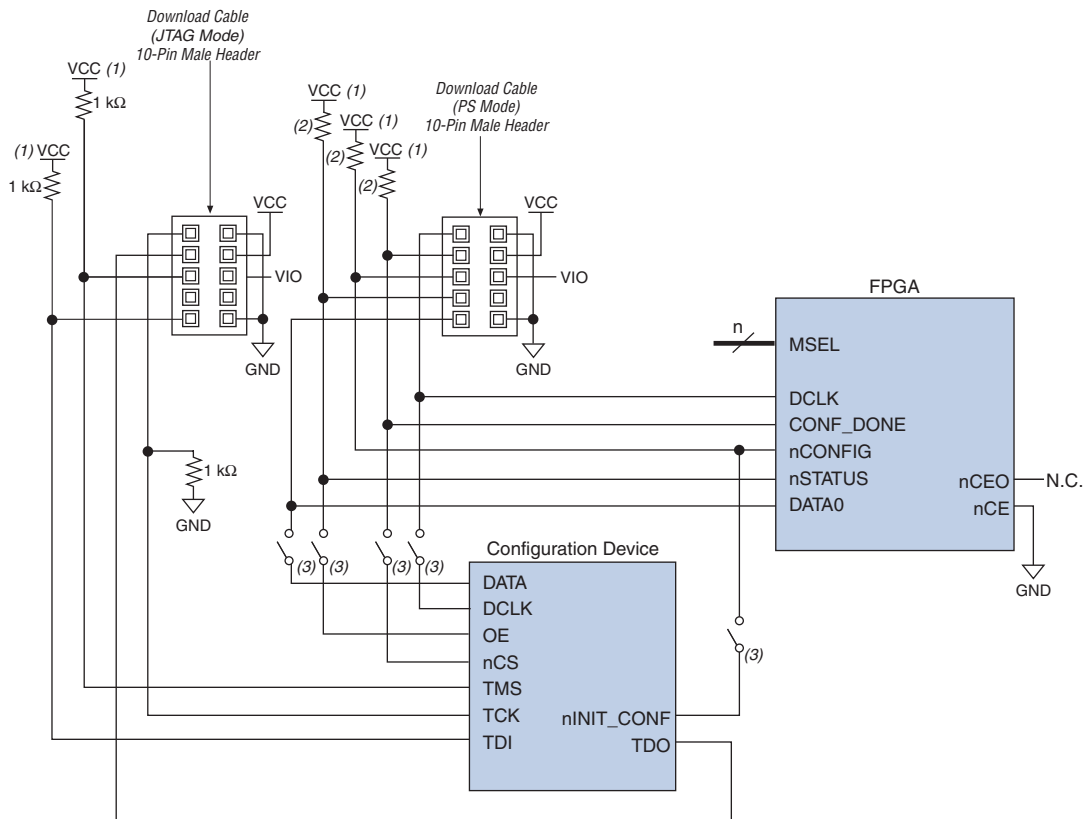
Figure 7-2. JTAG Programming of Configuration Device and FPGA with PS Configuration of FPGA Using a Configuration Device



Notes to Figure 7-2:

- (1) V_{CC} should be connected to the same supply voltage as the configuration device. For APEX 20KE devices, $nCONFIG$ should be pulled up to V_{CCINT} .
- (2) If the internal pull-up resistors of the configuration device are used, external pull-up resistors should not be used on these pins.

The download cables can be used in different modes (e.g., JTAG mode or PS mode) and in each mode, the header of the download cable connects to different pins on the FPGA. Therefore, two separate 10-pin headers are required on your board in order to support two different modes of the download cable. Figure 7-3 shows a schematic with two download cables. One download cable is used in JTAG mode to JTAG program the configuration device. The second download cable is used in PS mode to configure the FPGA using PS configuration. The MSEL pins should be set to select PS as the configuration mode.

Figure 7-3. JTAG Programming of Configuration Device with PS Configuration of FPGA Using a Configuration Device and Download Cable**Notes to Figure 7-3:**

- (1) V_{CC} should be connected to the same supply voltage as the configuration device. For APEX 20KE devices, $nCONFIG$ should be pulled up to V_{CCINT} .
- (2) If the internal pull-up resistors of the configuration device are used, external pull-up resistors should not be used on these pins.
- (3) To configure the FPGA with a download cable, you should either remove the configuration device from its socket or place a switch on the five common signals between the download cable and the configuration device.



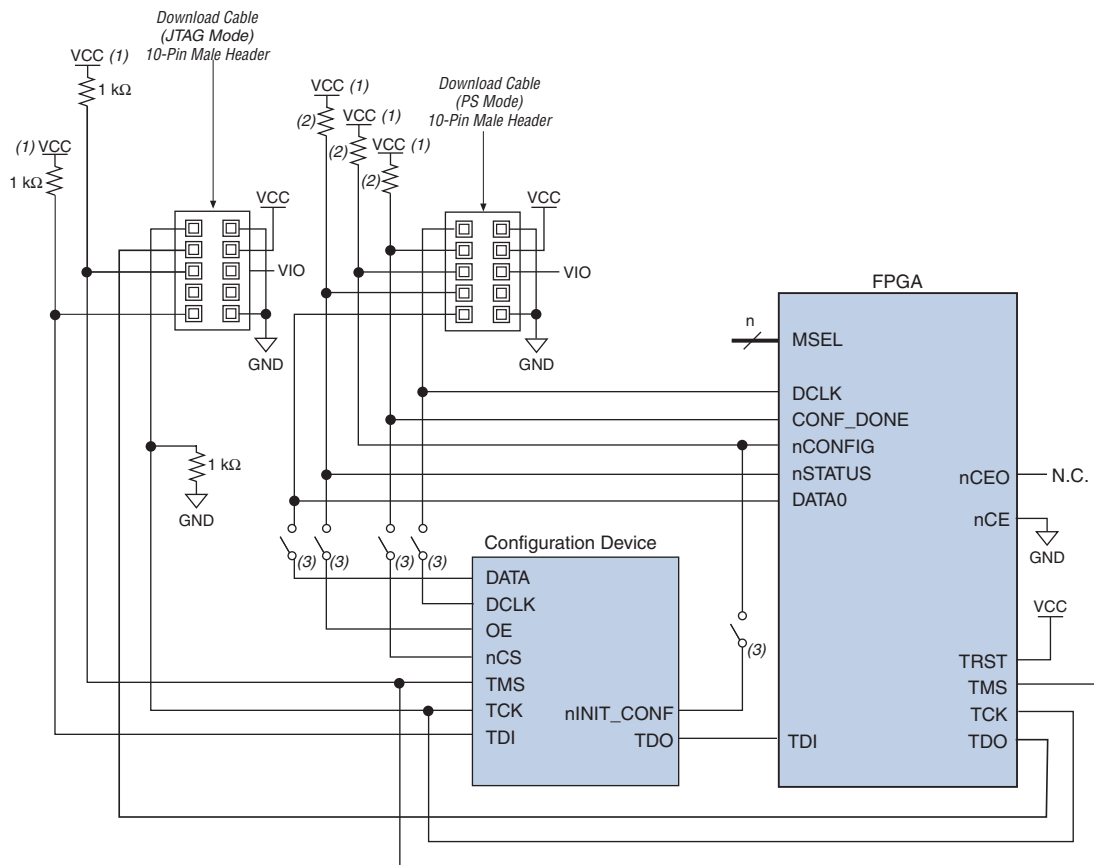
You should not attempt PS configuration with a download cable while a configuration device is connected to an FPGA.

If you try to configure the FPGA using the download cable while the configuration device is connected to the FPGA, the low signals driven on the $nSTATUS$ and $CONF_DONE$ pins will pull the OE and nCS pins of the configuration device low. This will reset the configuration device and cause it to try to configure the FPGA. To perform PS configuration with the download cable, you should either remove the configuration device from its socket when using the download cable, or place a switch on the five common signals between the download cable and the configuration device.

Figure 7-4 shows a schematic that allows configuration of the FPGA with either a PS mode download cable or JTAG mode download cable. Additionally, the FPGA can be configured using the configuration device. One download cable is used in JTAG mode to JTAG program the configuration device and FPGA. In Figure 7-4 the configuration device and FPGA are in the same JTAG chain. Make sure the TDO signal drives out a

high enough voltage to meet the next device's TDI minimum high-level input voltage (V_{IH}). The TDO output will drive out the voltage of the I/O bank's V_{CCIO} where it resides. For example, if the TDO pin resides in an I/O bank whose V_{CCIO} is set to 3.3 V, the TDO pin will drive out 3.3 V. The second download cable is used in PS mode to configure the FPGA using PS configuration. The MSEL pins should be set to select PS as the configuration mode.

Figure 7-4. Combining JTAG Programming of Configuration Device and FPGA with PS Configuration of FPGA Using a Configuration Device and Download Cable



Notes to Figure 7-4:

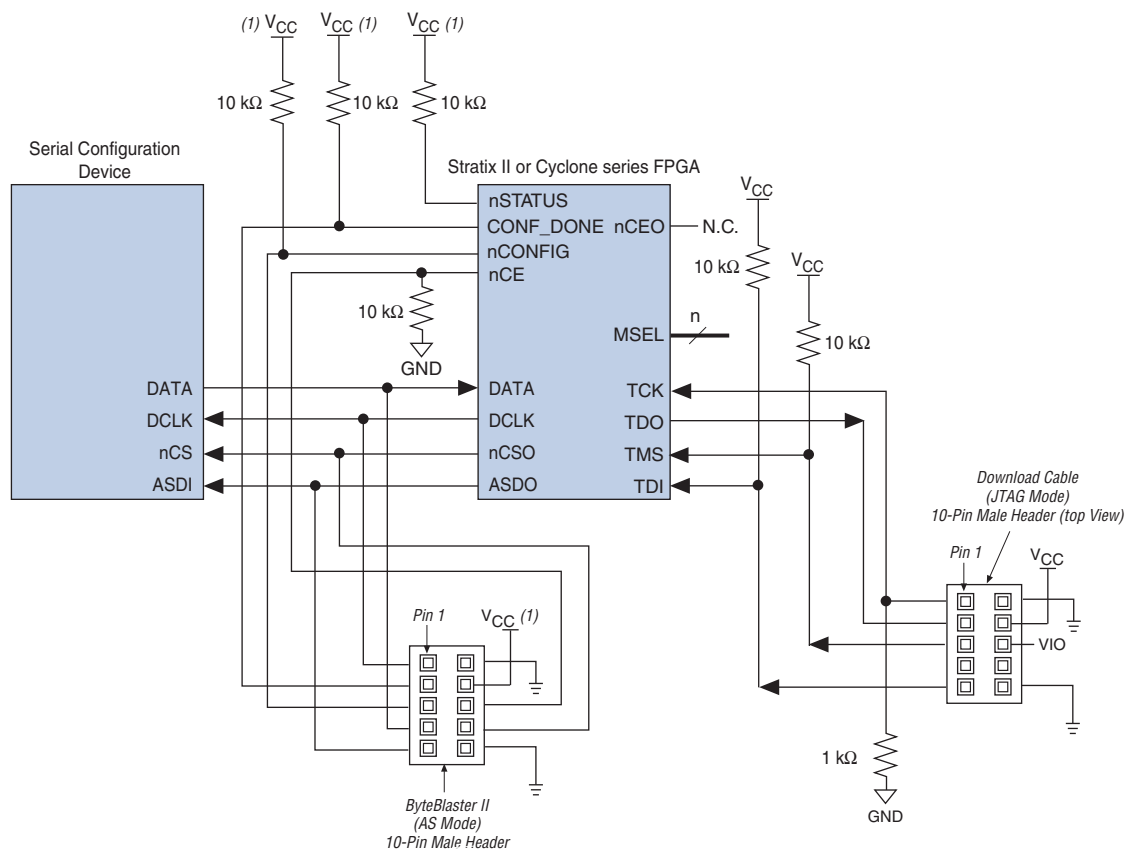
- (1) V_{CC} should be connected to the same supply voltage as the configuration device. For APEX 20KE devices, $nCONFIG$ should be pulled up to V_{CCINT} .
- (2) If the internal pull-up resistors of the configuration device are used, external pull-up resistors should not be used on these pins.
- (3) To configure the FPGA with a download cable, you should either remove the configuration device from its socket or place a switch on the five common signals between the download cable and the configuration device.

Figure 7-1 on page 7-2 and Figure 7-4 also apply for fast passive parallel (FPP) mode, except DATA [7 . . 0] is connected from the enhanced configuration device to the FPGAs that support FPP configuration. The MSEL pins must be set accordingly.

Active Serial and JTAG

For devices that support AS configuration (e.g. Stratix series, Cyclone series, or Arria series devices), you can combine the AS configuration scheme with JTAG-based configuration (refer to [Figure 7-5](#)). This setup uses two 10-pin download cable headers on the board. One download cable is used in JTAG mode to configure the Stratix II or Cyclone series FPGA directly via the JTAG interface. The other download cable is used in AS mode to program the serial configuration device in-system via the AS programming interface. The MSEL pins should be set to select the AS configuration mode. If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration will be terminated.

Figure 7-5. Combining JTAG Programming of Configuration Device and FPGA with AS Configuration of FPGA Using a Configuration Device and Download Cable



Note to Figure 7-5:

(1) V_{CC} should be connected to 3.3 V.

Chapter Revision History

Table 7-1 lists the revision history for this chapter.

Table 7-1. Chapter Revision History

Date	Version	Changes Made
December 2009	2.5	<ul style="list-style-type: none">■ Updated Table 7-1.■ Removed “Referenced Documents” section.
October 2008	2.4	<ul style="list-style-type: none">■ Updated “Introduction” and “Active Serial and JTAG” sections.■ Added “Referenced Documents” section.■ Updated new document format.
January 2008	2.3	<ul style="list-style-type: none">■ Corrected figure title in Figure 9-5.
April 2007	2.2	<ul style="list-style-type: none">■ Added document revision history.
August 2005	2.1	<ul style="list-style-type: none">■ Removed active cross references referring to document outside Chapter 9.
July 2004	2.0	<ul style="list-style-type: none">■ Added Stratix II and Cyclone II device information throughout chapter.
September 2003	1.0	<ul style="list-style-type: none">■ Initial Release.

