
This section provides documentation on design considerations when utilizing Cyclone devices. In addition to these design considerations, refer to the Intellectual Property section of the Altera web site for a complete offering of IP cores for Cyclone devices.

This section contains the following chapters:

- [Chapter 10, Implementing Double Data Rate I/O Signaling in Cyclone Devices](#)
- [Chapter 11. Using Cyclone Devices in Multiple-Voltage Systems](#)
- [Chapter 12. Designing with 1.5-V Devices](#)

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Introduction

Double data rate (DDR) transmission is used in many applications where fast data transmission is needed, such as memory access and first-in first-out (FIFO) memory structures. DDR uses both edges of a clock to transmit data, which facilitates data transmission at twice the rate of a single data rate (SDR) architecture using the same clock speed. This method also reduces the number of I/O pins required to transmit data.

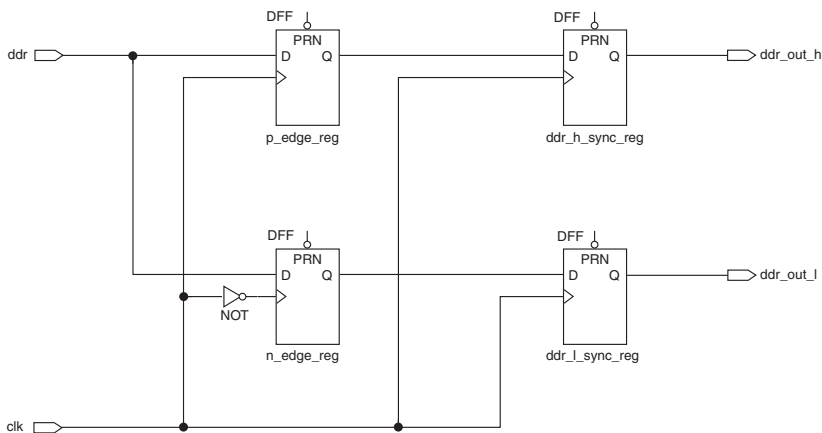
This chapter shows implementations of a double data rate I/O interface using Cyclone® devices. Cyclone devices support DDR input, DDR output, and bidirectional DDR signaling.

For more information on using Cyclone devices in applications with DDR SDRAM and FCRAM memory devices, refer to “[DDR Memory Support](#)” on page 10–4.

Double Data Rate Input

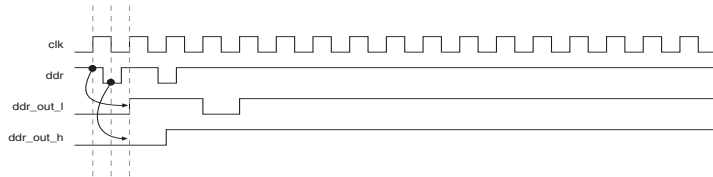
The DDR input implementation shown in [Figure 10–1](#) uses four internal logic element (LE) registers located in the logic array block (LAB) adjacent to the DDR input pin. The DDR data is fed to the first two of four registers. One register captures the DDR data present during the rising edge of the clock. The second register captures the DDR data present during the falling edge of the clock.

Figure 10–1. Double Data Rate Input Implementation



The third and fourth registers synchronize the two data streams to the rising edge of the clock. [Figure 10-2](#) shows examples of functional waveforms from a double data rate input implementation.

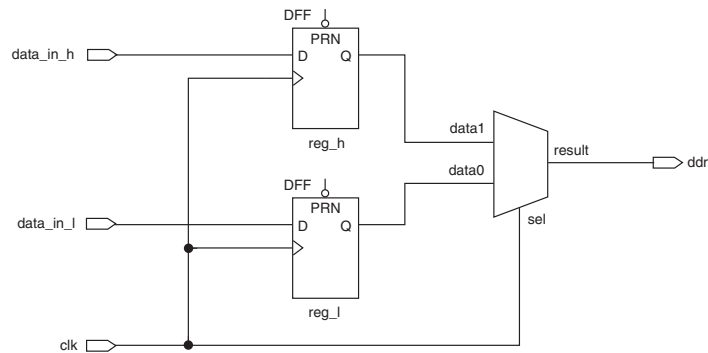
Figure 10-2. Double Data Rate Input Functional Waveforms



Double Data Rate Output

[Figure 10-3](#) shows a schematic representation of double data rate output implemented in a Cyclone device. The DDR output logic is implemented using LEs in the LAB adjacent to the output pin. Two registers are used to synchronize two serial data streams. The registered outputs are then multiplexed by the common clock to drive the DDR output pin at two times the data rate.

Figure 10-3. Double Data Rate Output Implementation

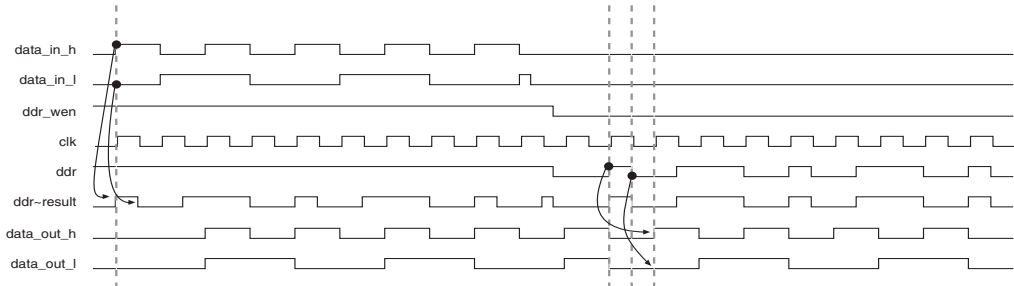


While the clock signal is logic-high, the output from `reg_h` is driven onto the DDR output pin. While the clock signal is logic-low, the output from `reg_l` is driven onto the DDR output pin. The DDR output pin can be any available user I/O pin.

[Figure 10-4](#) shows examples of functional waveforms from a double data rate output implementation.

Figure 10–6 shows example waveforms from a bidirectional double data rate implementation.

Figure 10–6. Double Data Rate Bidirectional Waveforms



DDR Memory Support

The Cyclone device family supports both DDR SDRAM and FCRAM memory interfaces up to 133 MHz.



For more information about extended DDR memory support in Cyclone devices, refer to the *Cyclone FPGA Family Data Sheet* section of the *Cyclone Device Handbook*.

Conclusion

Utilizing both the rising and falling edges of a clock signal, double data rate transmission is a popular strategy for increasing the speed of data transmission while reducing the required number of I/O pins. Cyclone devices can be used to implement this strategy for use in applications such as FIFO structures, SDRAM/FCRAM interfaces, as well as other time-sensitive memory access and data-transmission situations.

Referenced Documents

This chapter references the following document:

- *Cyclone FPGA Family Data Sheet* section of the *Cyclone Device Handbook*

Document Revision History

Table 10–1 shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.2	Minor textual and style changes. Added “Referenced Documents” section.	—
January 2007 v1.1	Added document revision history.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Introduction

To meet the demand for higher system speed in data communications, semiconductor vendors use increasingly advanced processing technologies requiring lower operating voltages. As a result, printed circuit boards (PCBs) often incorporate devices conforming to one of several voltage level I/O standards, such as 3.3-V, 2.5-V, 1.8-V and 1.5-V. A mixture of components with various voltage level I/O standards on a single PCB is inevitable.

In order to accommodate this mixture of devices on a single PCB, a device that can act as a bridge or interface between these devices is needed. The Cyclone[®] device family's MultiVolt[™] I/O operation capability meets the increasing demand for compatibility with devices of different voltages. MultiVolt I/O operation separates the power supply voltage from the output voltage, enabling Cyclone devices to interoperate with other devices using different voltage levels on the same PCB.

In addition to MultiVolt I/O operation, this chapter discusses several other features that allow you to use Cyclone devices in multiple-voltage systems without damaging the device or the system, including:

- Hot-Socketing—add and remove Cyclone devices to and from a powered-up system without affecting the device or system operation
- Power-Up Sequence flexibility—Cyclone devices can accommodate any possible power-up sequence
- Power-On Reset—Cyclone devices maintain a reset state until voltage is within operating range

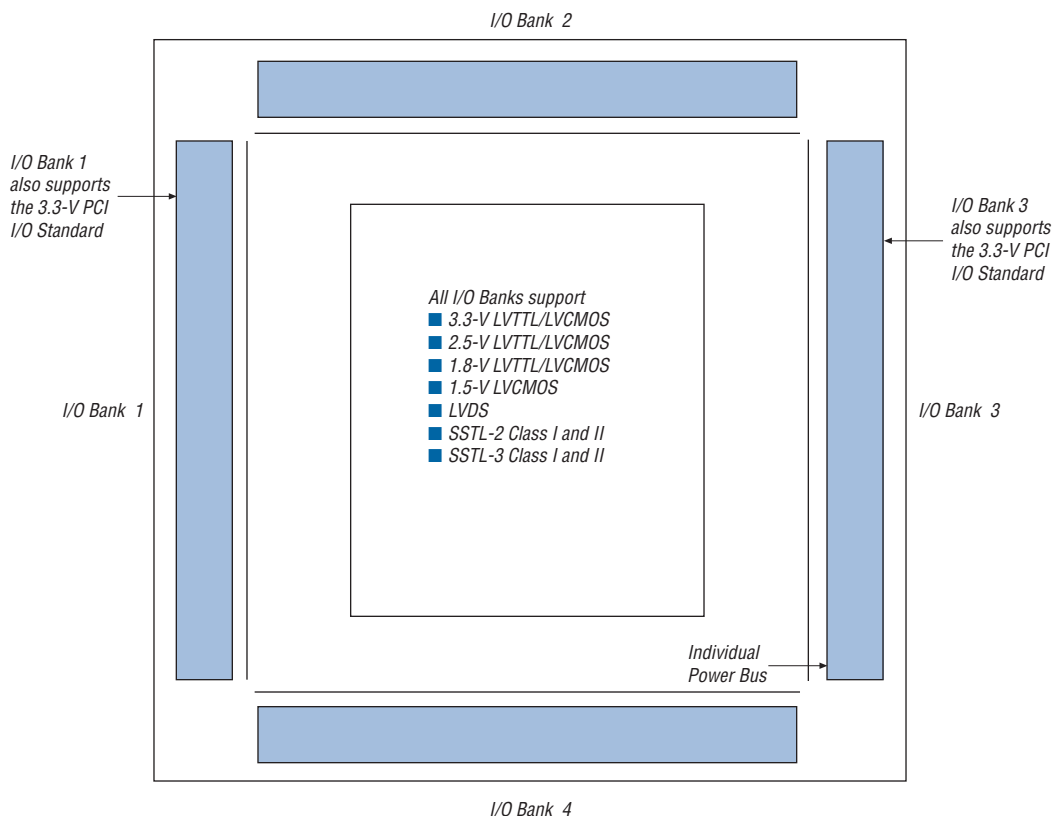
I/O Standards

The I/O buffer of a Cyclone device is programmable and supports a wide range of I/O voltage standards. Each I/O bank in a Cyclone device can be programmed to comply with a different I/O standard. All I/O banks can be configured with the following I/O standards:

- 3.3-V LVTTTL/LVCMOS
- 2.5-V LVTTTL/LVCMOS
- 1.8-V LVTTTL/LVCMOS
- 1.5-V LVCMOS
- LVDS
- SSTL-2 Class I and II
- SSTL-3 Class I and II

I/O banks 1 and 3 also include 3.3-V PCI I/O standard interface capability. See Figure 11–1.

Figure 11–1. I/O Standards Supported by Cyclone Devices Notes (1), (2), (3)



Notes to Figure 11–1

- (1) Figure 1 is a top view of the silicon die.
- (2) Figure 1 is a graphical representation only. Refer to the pin list and the Quartus® II software for exact pin locations.
- (3) The EP1C3 device in the 100-pin thin quad flat pack (TQFP) package does not have support for a PLL LVDS input or an external clock output.

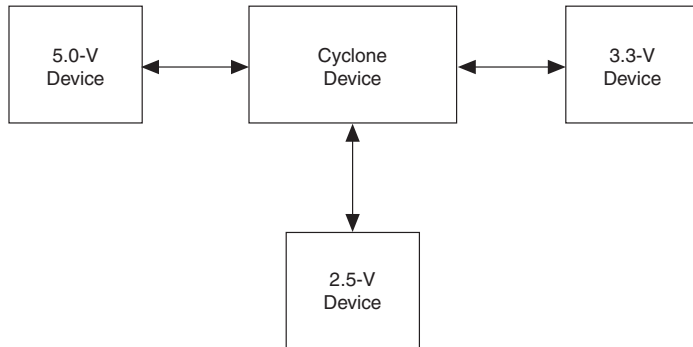
MultiVolt I/O Operation

Cyclone devices include MultiVolt I/O operation capability, allowing the core and I/O blocks of the device to be powered-up with separate supply voltages. The VCCINT pins supply power to the device core and the VCCIO pins supply power the device's I/O buffers.



Supply all device V_{CCIO} pins that have MultiVolt I/O capability at the same voltage level (e.g., 3.3-V, 2.5-V, 1.8-V, or 1.5-V). See [Figure 11-2](#).

Figure 11-2. Implementing a Multiple-Voltage System with a Cyclone Device

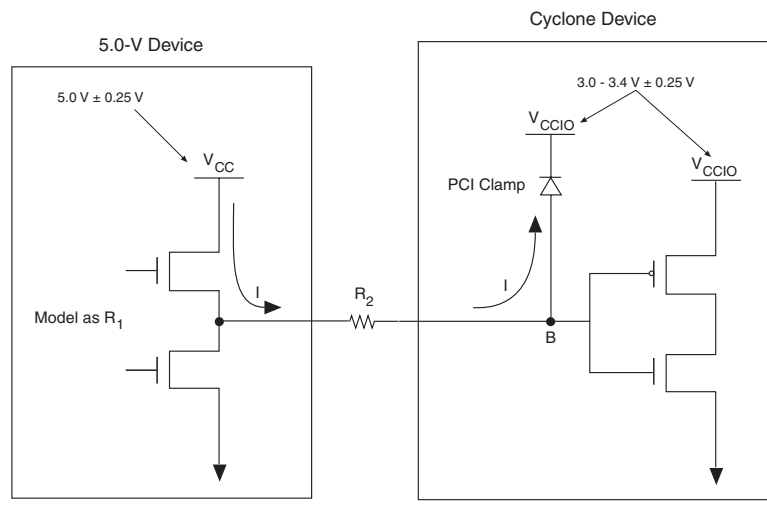


5.0-V Device Compatibility

A Cyclone device may not correctly interoperate with a 5.0-V device if the output of the Cyclone device is connected directly to the input of the 5.0-V device. If V_{OUT} of the Cyclone device is greater than V_{CCIO} , the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0-V.

A Cyclone device can drive a 5.0-V LVTTTL device by connecting the V_{CCIO} pins of the Cyclone device to 3.3 V. This is because the output high voltage (V_{OH}) of a 3.3-V interface meets the minimum high-level voltage of 2.4-V of a 5.0-V LVTTTL device. (A Cyclone device cannot drive a 5.0-V LVCMOS device.)

Because the Cyclone devices are 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliant the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.1-V. To drive a Cyclone device with a 5.0-V device, you must connect a resistor (R_2) between the Cyclone device and the 5.0-V device. See [Figure 11-3](#).

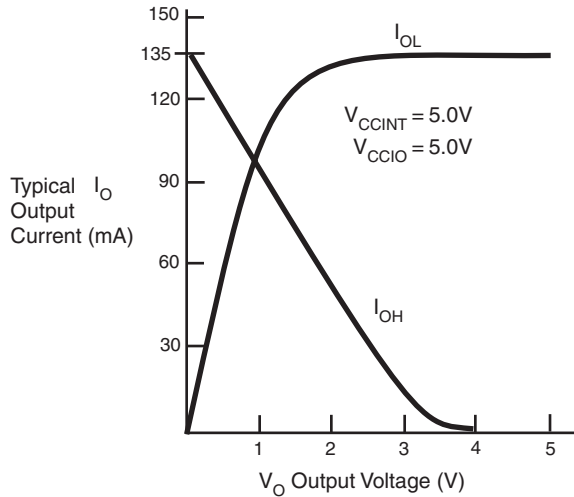
Figure 11–3. Driving a Cyclone Device with a 5.0-Volt Device

If V_{CCIO} is between 3.0-V and 3.6-V and the PCI clamping diode (not available on EP1C3 devices) is enabled, the voltage at point B in [Figure 11–3](#) is 4.3-V or less. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace. The PCI clamping diode in the Cyclone device can support 25mA of current.

To compute the required value of R_2 , first calculate the model of the pull-up transistors on the 5.0-V device. This output resistor (R_1) can be modeled by dividing the 5.0-V device supply voltage (V_{CC}) by the I_{OH} :

$$R_1 = V_{CC}/I_{OH}$$

[Figure 11–4](#) shows an example of typical output drive characteristics of a 5.0-V device.

Figure 11–4. Output Drive Characteristics of a 5.0-V Device

As shown above, $R_1 = 5.0\text{-V} / 135\text{ mA}$.



The values usually shown in data sheets reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction applied to the above example gives R_1 a value of $30\ \Omega$

R_2 should be selected to not violate the driving device's IOH specification. For example, if the above device has a maximum IOH of 8 mA, given the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{-V} = 3.7\text{-V}$. Given that the maximum supply load of a 5.0-V device (V_{CC}) will be 5.25-V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.25\text{V} - 3.7\text{V}) - (8\text{ mA} \times 30\ \Omega)}{8\text{ mA}} = 164\ \Omega$$

This analysis assumes worst-case conditions. If your system will not see a wide variation in voltage-supply levels, you can adjust these calculations accordingly.



Because 5.0-V device tolerance in Cyclone devices requires use of the PCI clamp (not available on EP1C3 devices), and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured.

Hot-Socketing

Hot-socketing, also known as hot-swapping, refers to inserting or removing a board or device into or out of a system board while system power is on. For a system to support hot-socketing, plug-in or removal of the subsystem or device must not damage the system or interrupt system operation.

All devices in the Cyclone family are designed to support hot-socketing without special design requirements. The following features have been implemented in Cyclone devices to facilitate hot-socketing:

- Devices can be driven before power-up with no damage to the device.
- I/O pins remain tri-stated during power-up.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies.



Because 5.0-V tolerance in Cyclone devices require the use of the PCI clamping diode, and the clamping diode is only available after configuration has finished, be careful not to connect 5.0-V signals to the device.

Devices Can Be Driven before Power-Up

The device I/O pins, dedicated input pins, and dedicated clock pins of Cyclone devices can be driven before or during power-up without damaging the devices.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. For Cyclone devices, I/O pins are tri-stated before and during power-up and configuration, and will not drive out.

Signal Pins Do Not Drive the V_{CCIO} or V_{CCINT} Power Supplies

A device that does not support hot-socketing will short power supplies together when powered-up through its signal pins. This irregular power-up can damage both the driving and driven devices and can disrupt card power-up.

In Cyclone devices, there is no current path from I/O pins, dedicated input pins, or dedicated clock pins to the V_{CCIO} or V_{CCINT} pins before or during power-up. A Cyclone device may be inserted into (or removed from) a powered-up system board without damaging or interfering with system-board operation. When hot-socketing, Cyclone devices have a minimal effect on the signal integrity of the backplane.



The maximum DC current when hot-socketing Cyclone devices is less than 300 μA , whereas the maximum AC current during hot-socketing is less than 8 mA for a period of 10ns or less.

During hot-socketing, the signal pins of a device may be connected and driven by the active system before the power supply can provide current to the device V_{CC} and ground planes. Known as latch-up, this condition can cause parasitic diodes to turn on within the device, causing the device to consume a large amount of current, and possibly causing electrical damage. This operation can also cause parasitic diodes to turn on inside of the driven device. Cyclone devices are immune to latch-up when hot-socketing.

Power-Up Sequence

Because Cyclone devices can be used in a multi-voltage environment, they are designed to tolerate any possible power-up sequence. Either V_{CCINT} or V_{CCIO} can initially supply power to the device, and 3.3-V, 2.5-V, 1.8-V, or 1.5-V input signals can drive the devices without special precautions before V_{CCINT} or V_{CCIO} is applied. Cyclone devices can operate with a V_{CCIO} voltage level that is higher than the V_{CCINT} level. You can also change the V_{CCIO} supply voltage while the board is powered-up. However, you must ensure that the V_{CCINT} and V_{CCIO} power supplies stay within the correct device operating conditions.

When V_{CCIO} and V_{CCINT} are supplied from different power sources to a Cyclone device, a delay between V_{CCIO} and V_{CCINT} may occur. Normal operation does not occur until both power supplies are in their recommended operating range. When V_{CCINT} is powered-up, the IEEE Std. 1149.1 Joint Test Action Group (JTAG) circuitry is active. If TMS and TCK are connected to V_{CCIO} and V_{CCIO} is not powered-up, the JTAG signals are left floating. Thus, any transition on TCK can cause the state machine to transition to an unknown JTAG state, leading to incorrect operation when V_{CCIO} is finally powered-up. To disable the JTAG state during the power-up sequence, TCK should be pulled low to ensure that an inadvertent rising edge does not occur on TCK.

Power-On Reset

When designing a circuit, it is important to consider system state at power-up. Cyclone devices maintain a reset state during power-up. When power is applied to a Cyclone device, a power-on-reset event occurs if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). A POR event does not occur if these conditions are not met because slower rise times can cause incorrect device initialization and functional failure. The V_{CCIO} level of the I/O banks that contains configuration pins must also reach an acceptable level to trigger POR event.



If V_{CCINT} does not remain in the specified operating range, operation is not assured until V_{CCINT} re-enters the range.

Conclusion

PCBs often contain a mix of 5.0-V, 3.3-V, 2.5-V, 1.8-V, and 1.5-V devices. The Cyclone device family's MultiVolt I/O operation capability allows you to incorporate newer-generation devices with devices of varying voltage levels. This capability also enables the device core to run at its core voltage, V_{CCINT} , while maintaining I/O pin compatibility with other logic levels. Altera has taken further steps to make system design easier by designing devices that allow V_{CCINT} and V_{CCIO} to power-up in any sequence and by incorporating support for hot-socketing.

Document Revision History

Table 11-1 shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.3	Minor textual and style changes.	—
January 2007 v1.2	Updated "Power-On Reset" section.	—
October 2003 v1.1	Added 64-bit PCI support information.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

Introduction

The Cyclone® FPGA family provides the best solution for high-volume, cost-sensitive applications. A Cyclone device is fabricated on a leading-edge 1.5-V, 0.13- μ m, all-layer copper SRAM process.

Using a 1.5-V operating voltage provides the following advantages:

- Lower power consumption compared to 2.5-V or 3.3-V devices.
- Lower operating temperature.
- Less need for fans and other temperature-control elements.

Since many existing designs are based on 5.0-V, 3.3-V and 2.5-V power supplies, a voltage regulator may be required to lower the voltage supply level to 1.5-V. This document provides guidelines for designing with Cyclone devices in mixed-voltage and single-voltage systems and provides examples using voltage regulators. This document also includes information about:

- [“Power Sequencing and Hot Socketing” on page 12-1](#)
- [“Using MultiVolt I/O Pins” on page 12-2](#)
- [“Voltage Regulators” on page 12-3](#)
- [“1.5-V Regulator Application Examples” on page 12-19](#)
- [“Board Layout” on page 12-21](#)
- [“Power Sequencing and Hot Socketing” on page 12-1](#)

Power Sequencing and Hot Socketing

Because 1.5-V Cyclone FPGAs can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

You can drive signals into Cyclone FPGAs before and during power up without damaging the device. In addition, Cyclone FPGAs do not drive out during power up since they are tri-stated during power up. Once the device reaches operating conditions and is configured, Cyclone FPGAs operate as specified by the user.



For more information, refer to the [Cyclone FPGA Family Data Sheet](#) section of the *Cyclone Device Handbook*.

Using MultiVolt I/O Pins

Cyclone FPGAs require a 1.5-V V_{CCINT} and a 3.3-V, 2.5-V, 1.8-V, or 1.5-V I/O supply voltage level (V_{CCIO}). All pins, including dedicated inputs, clock, I/O, and JTAG pins, are 3.3-V tolerant before and after V_{CCINT} and V_{CCIO} are powered.

When V_{CCIO} is connected to 1.5-V, the output is compatible with 1.5-V logic levels. The output pins can be made 1.8-V, 2.5-V, or 3.3-V compatible by using open-drain outputs pulled up with external resistors. You can use external resistors to pull open-drain outputs up with a 1.8-V, 2.5-V, or 3.3-V V_{CCIO} . Table 12-1 summarizes Cyclone MultiVolt I/O support.

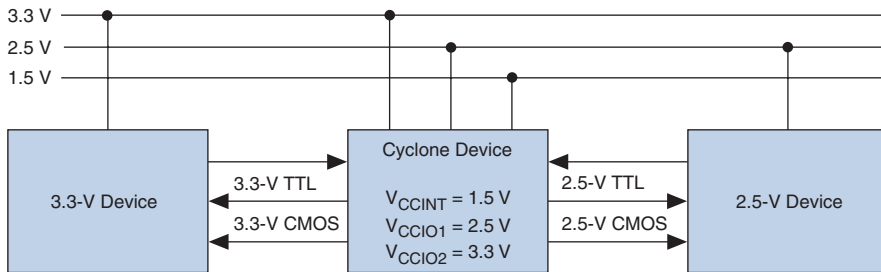
Table 12-1. Cyclone MultiVolt I/O Support Note (1)

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5-V	1.8-V	2.5-V	3.3-V	5.0-V	1.5-V	1.8-V	2.5-V	3.3-V	5.0-V
1.5-V	✓	✓	✓ (2)	✓ (2)	—	✓	—	—	—	—
1.8-V	✓	✓	✓	✓	—	✓ (3)	✓	—	—	—
2.5-V	—	—	✓	✓	—	✓ (5)	✓ (5)	✓	—	—
3.3-V	—	—	✓ (4)	✓	✓ (6)	✓ (7)	✓ (7)	✓ (7)	✓	✓ (8)

Notes to Table 12-1:

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO} .
- (2) When $V_{CCIO} = 1.5\text{-V}$ and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected.
- (3) When $V_{CCIO} = 1.8\text{-V}$, a Cyclone device can drive a 1.5-V device with 1.8-V tolerant inputs.
- (4) When $V_{CCIO} = 3.3\text{-V}$ and a 2.5-V input signal feeds an input pin, or when $V_{CCIO} = 1.8\text{-V}$ and a 1.5-V input signal feeds an input pin, the V_{CCIO} supply current is slightly larger than expected. The reason for this increase is that the input signal level does not drive to the V_{CCIO} rail, which causes the input buffer to not completely shut off.
- (5) When $V_{CCIO} = 2.5\text{-V}$, a Cyclone device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
- (6) Cyclone devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.
- (7) When $V_{CCIO} = 3.3\text{-V}$, a Cyclone device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
- (8) When $V_{CCIO} = 3.3\text{-V}$, a Cyclone device can drive a device with 5.0-V LVTTTL inputs but not 5.0-V LVCMOS inputs.

Figure 12-1 shows how Cyclone FPGAs interface with 3.3-V and 2.5-V devices while operating with a 1.5-V V_{CCINT} to increase performance and save power.

Figure 12–1. Cyclone FPGAs Interface with 3.3-V and 2.5-V Devices

Voltage Regulators

This section explains how to generate a 1.5-V supply from another system supply. Supplying power to the 1.5-V logic array and/or I/O pins requires a 5.0-V- or 3.3-V-to-1.5-V voltage regulator. A linear regulator is ideal for low-power applications because it minimizes device count and has acceptable efficiency for most applications. A switching voltage regulator provides optimal efficiency. Switching regulators are ideal for high-power applications because of their high efficiency.

This section will help you decide which regulator to use in your system, and how to implement the regulator in your design. There are several companies that provide voltage regulators for low-voltage devices, such as Linear Technology Corporation, Maxim Integrated Products, Intersil Corporation (Elantec), and National Semiconductor Corporation.

Table 12–2 shows the terminology and specifications commonly encountered with voltage regulators. Symbols are shown in parentheses. If the symbols are different for linear and switching regulators, the linear regulator symbol is listed first.

Table 12–2. Voltage Regulator Specifications and Terminology (Part 1 of 2)

Specification/Terminology	Description
Input voltage range (V_{IN}, V_{CC})	Minimum and maximum input voltages define the input voltage range, which is determined by the regulator process voltage capabilities.
Line regulation (line regulation, V_{OUT})	Line regulation is the variation of the output voltage (V_{OUT}) with changes in the input voltage (V_{IN}). Error amplifier gain, pass transistor gain, and output impedance all influence line regulation. Higher gain results in better regulation. Board layout and regulator pin-outs are also important because stray resistance can introduce errors.

Table 12–2. Voltage Regulator Specifications and Terminology (Part 2 of 2)

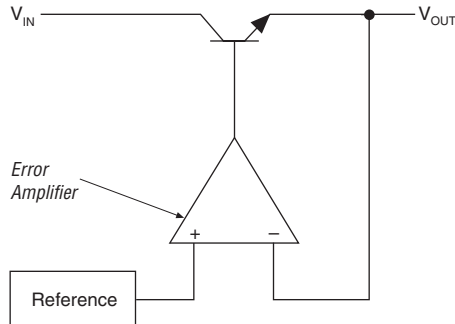
Specification/Terminology	Description
Load regulation (load regulation, V_{OUT})	Load regulation is a variation in the output voltage caused by changes in the input supply current. Linear Technology regulators are designed to minimize load regulation, which is affected by error amplifier gain, pass transistor gain, and output impedance.
Output voltage selection	Output voltage selection is adjustable by resistor voltage divider networks, connected to the error amplifier input, that control the output voltage. There are multiple output regulators that create 5.0-, 3.3-, 2.5-, 1.8- and 1.5-V supplies.
Quiescent current	Quiescent current is the supply current during no-load or quiescent state. This current is sometimes used as a general term for a supply current used by the regulator.
Dropout voltage	Dropout voltage is the difference between the input and output voltages when the input is low enough to cause the output to drop out of regulation. The dropout voltage should be as low as possible for better efficiency.
Current limiting	Voltage regulators are designed to limit the amount of output current in the event of a failing load. A short in the load causes the output current and voltage to decrease. This event cuts power dissipation in the regulator during a short circuit.
Thermal overload protection	This feature limits power dissipation if the regulator overheats. When a specified temperature is reached, the regulator turns off the output drive transistors, allowing the regulator to cool. Normal operation resumes once the regulator reaches a normal operating temperature.
Reverse current protection	If the input power supply fails, large output capacitors can cause a substantial reverse current to flow backward through the regulator, potentially causing damage. To prevent damage, protection diodes in the regulator create a path for the current to flow from V_{OUT} to V_{IN} .
Stability	The dominant pole placed by the output capacitor influences stability. Voltage regulator vendors can assist you in output capacitor selection for regulator designs that differ from what is offered.
Minimum load requirements	A minimum load from the voltage divider network is required for good regulation, which also serves as the ground for the regulator's current path.
Efficiency	Efficiency is the division of the output power by the input power. Each regulator model has a specific efficiency value. The higher the efficiency value, the better the regulator.

Linear Voltage Regulators

Linear voltage regulators generate a regulated output from a larger input voltage using current pass elements in a linear mode. There are two types of linear regulators available: one using a series pass element and another using a shunt element (e.g., a zener diode). Altera recommends using series linear regulators because shunt regulators are less efficient.

Series linear regulators use a series pass element (i.e., a bipolar transistor or MOSFET) controlled by a feedback error amplifier (see [Figure 12-2](#)) to regulate the output voltage by comparing the output to a reference voltage. The error amplifier drives the transistor further on or off continuously to control the flow of current needed to sustain a steady voltage level across the load.

Figure 12-2. Series Linear Regulator



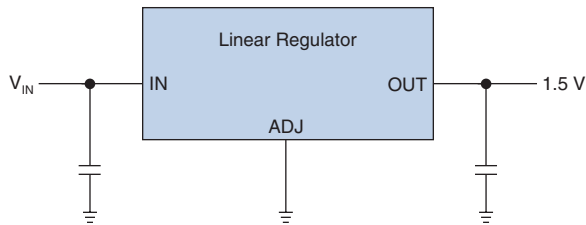
[Table 12-3](#) shows the advantages and disadvantages of linear regulators compared to switching regulators.

Advantages	Disadvantages
<ul style="list-style-type: none"> Requires few supporting components Low cost Requires less board space Quick transient response Better noise and drift characteristics No electromagnetic interference (EMI) radiation from the switching components Tighter regulation 	<ul style="list-style-type: none"> Less efficient (typically 60%) Higher power dissipation Larger heat sink requirements

You can minimize the difference between the input and output voltages to improve the efficiency of linear regulators. The dropout voltage is the minimum allowable difference between the regulator's input and output voltage.

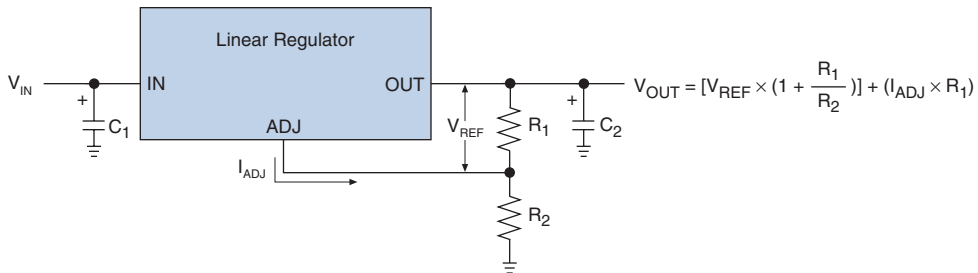
Linear regulators are available with fixed, variable, single, or multiple outputs. Multiple-output regulators can generate multiple outputs (e.g., 1.5- and 3.3-V outputs). If the board only has a 5.0-V power voltage supply, you should use multiple-output regulators. The logic array requires a 1.5-V power supply, and a 3.3-V power supply is required to interface with 3.3- and 5.0-V devices. However, fixed-output regulators have fewer supporting components, reducing board space and cost. [Figure 12-3](#) shows an example of a three-terminal, fixed-output linear regulator.

Figure 12-3. Three-Terminal, Fixed-Output Linear Regulator



Adjustable-output regulators contain a voltage divider network that controls the regulator's output. [Figure 12-4](#) shows how you can also use a three-terminal linear regulator in an adjustable-output configuration.

Figure 12-4. Adjustable-Output Linear Regulator



Switching Voltage Regulators

Step-down switching regulators can provide 3.3-V-to-1.5-V conversion with up to 95% efficiencies. This high efficiency comes from minimizing quiescent current, using a low-resistance power MOSFET switch, and, in higher-current applications, using a synchronous switch to reduce diode losses.

Switching regulators supply power by pulsing the output voltage and current to the load. Table 12-4 shows the advantages and disadvantages of switching regulators compared to linear regulators.

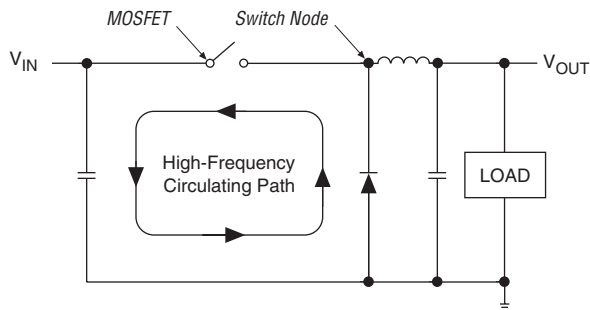


For more information about switching regulators, refer to Linear Technology's application note, *AN35: Step Down Switching Regulators*, at www.linear.com/designtools/app_notes.jsp.

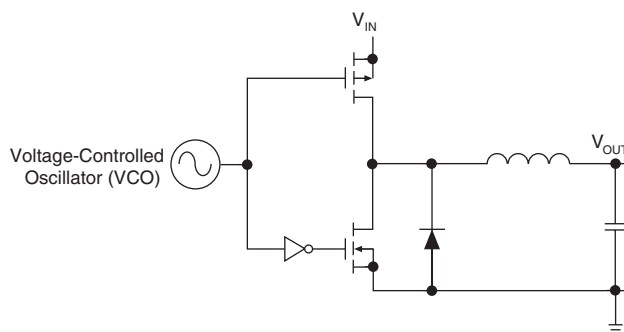
Advantages	Disadvantages
Highly efficient (typically >80%) Reduced power dissipation Smaller heat sink requirements Wider input voltage range High power density	Generates EMI Complex to design Requires 15 or more supporting components Higher cost Requires more board space

There are two types of switching regulators, asynchronous and synchronous. Asynchronous switching regulators have one field effect transistor (FET) and a diode to provide the current path while the FET is off (see Figure 12-5).

Figure 12-5. Asynchronous Switching Regulator



Synchronous switching regulators have a voltage- or current-controlled oscillator that controls the on and off time of the two MOSFET devices that supply the current to the circuit (see Figure 12-6).

Figure 12–6. Voltage-Controlled Synchronous Switching Regulator

Maximum Output Current

Select an external MOSFET switching transistor (optional) based on the maximum output current that it can supply. Use a MOSFET with a low on-resistance and a voltage rating high enough to avoid avalanche breakdown. For gate-drive voltages less than 9-V, use a logic-level MOSFET. A logic-level MOSFET is only required for topologies with a controller IC and an external MOSFET.

Selecting Voltage Regulators

Your design requirements determine which voltage regulator you need. The key to selecting a voltage regulator is understanding the regulator parameters and how they relate to the design.

The following checklist can help you select the proper regulator for your design:

- Do you require a 3.3-V, 2.5-V, and 1.5-V output (V_{OUT})?
- What precision is required on the regulated 1.5-V supplies (line and load regulation)?
- What supply voltages (V_{IN} or V_{CC}) are available on the board?
- What voltage variance (input voltage range) is expected on V_{IN} or V_{CC} ?
- What is the maximum I_{CC} (I_{OUT}) required by your Altera® device?
- What is the maximum current surge ($I_{OUT(MAX)}$) that the regulator will need to supply instantaneously?

Choose a Regulator Type

If required, select either a linear, asynchronous switching, or synchronous switching regulator based on your output current, regulator efficiency, cost, and board-space requirements. DC-to-DC converters have output current capabilities from 1 to 8 A. You can use a controller with an external MOSFET rated for higher current for higher-output-current applications.

Calculate the Maximum Input Current

Use the following equation to estimate the maximum input current based on the output power requirements at the maximum input voltage:

$$I_{IN,DC(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN(MAX)}}$$

Where η is nominal efficiency: typically 90% for switching regulators, 60% for linear 2.5-V-to-1.5-V conversion, 45% for linear 3.3-V-to-1.5-V conversion, and 30% for linear 5.0-V-to-1.5-V conversion.

Once you identify the design requirements, select the voltage regulator that is best for your design. Tables 12-5 and 12-6 list a few Linear Technology and Elantec regulators available at the time this document was published. There may be more regulators to choose from depending on your design specification. Contact a regulator manufacturer for availability.

Table 12-5. Linear Technology 1.5-V Output Voltage Regulators

Voltage Regulator	Regulator Type	Total Number of Components	V _{IN} (V)	I _{OUT} (A)	Special Features
LT1573	Linear	10	2.5 or 3.3 (1)	6	—
LT1083	Linear	5	5.0	7.5	—
LT1084	Linear	5	5.0	5	—
LT1085	Linear	5	5.0	3	Inexpensive solution
LTC1649	Switching	22	3.3	15	Selectable output
LTC1775	Switching	17	5.0	5	—

Note to Table 12-5:

- (1) A 3.3-V V_{IN} requires a 3.3-V supply to the regulator's input and 2.5-V supply to bias the transistors.

Table 12–6. Elantec 1.5-V Output Voltage Regulators

Voltage Regulator	Regulator Type	Total Number of Components	V _{IN} (V)	I _{OUT} (A)	Special Features
EL7551C	Switching	11	5.0	1	—
EL7564CM	Switching	13	5.0	4	—
EL7556BC	Switching	21	5.0	6	—
EL7562CM	Switching	17	3.3 or 5.5	2	—
EL7563CM	Switching	19	3.3	4	—

Voltage Divider Network

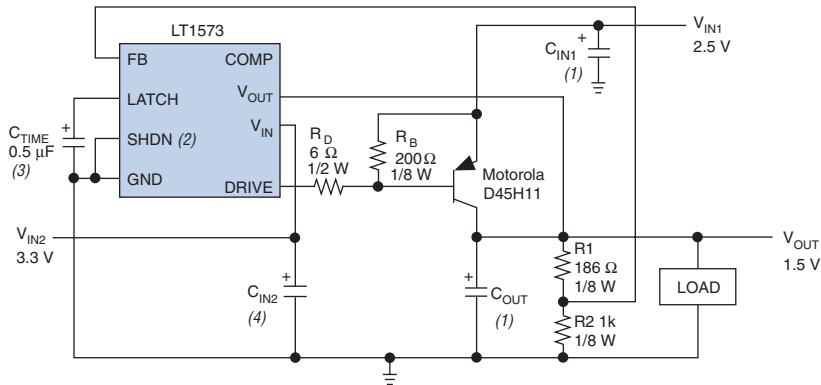
Design a voltage divider network if you are using an adjustable output regulator. Follow the controller or converter IC's instructions to adjust the output voltage.

1.5-V Regulator Circuits

This section contains the circuit diagrams for the voltage regulators discussed in this chapter. You can use the voltage regulators in this section to generate a 1.5-V power supply. Refer to the voltage regulator data sheet to find detailed specifications. If you require further information that is not shown in the data sheet, contact the regulator's vendor.

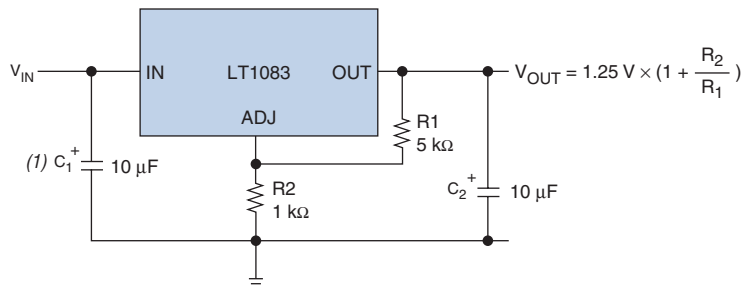
Figures 12–7 through 12–12 show the circuit diagrams of Linear Technology voltage regulators listed in Table 12–5.

The LT1573 linear voltage regulator converts 2.5-V to 1.5-V with an output current of 6A (see Figure 12–7).

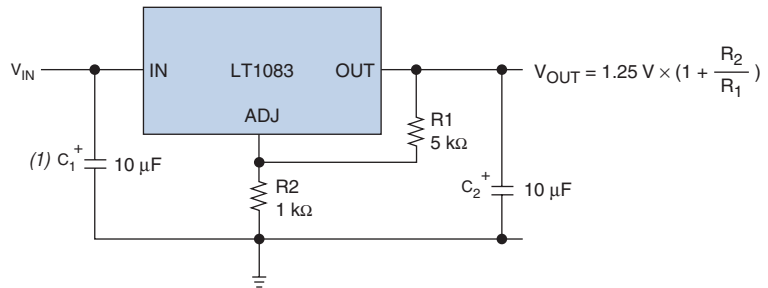
Figure 12-7. LT1573: 2.5-V-to-1.5-V/6.0-A Linear Voltage Regulator**Notes to Figure 12-7:**

- (1) C_{IN1} and C_{OUT} are AVX 100- μ F/10-V surface-mount tantalum capacitors.
- (2) Use SHDN (active high) to shut down the regulator.
- (3) C_{TIME} is a 0.5- μ F capacitor for 100-ms time out at room temperature.
- (4) C_{IN2} is an AVX 15- μ F/10-V surface-mount tantalum capacitor.

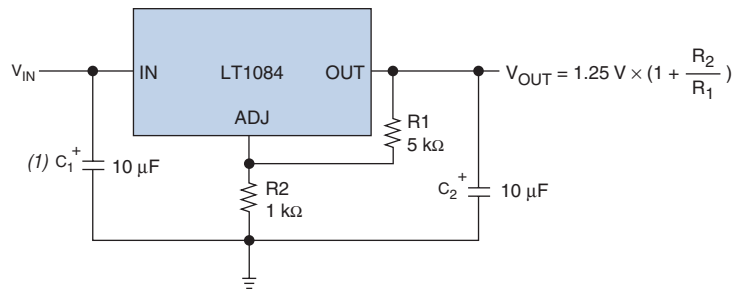
Use adjustable 5.0- to 1.5-V regulators (shown in Figures 12-8 through 12-10) for 3.0- to 7.5-A low-cost, low-device-count, board-space-efficient solutions.

Figure 12-8. LT1083: 5.0-V-to-1.5-V/7.5-A Linear Voltage Regulator**Note to Figure 12-8:**

- (1) This capacitor is necessary to maintain the voltage level at the input regulator. There could be a voltage drop at the input if the voltage supply is too far away.

Figure 12–9. LT1084: 5.0-V-to-1.5-V/5.0-A Linear Voltage Regulator**Note to Figure 12–9:**

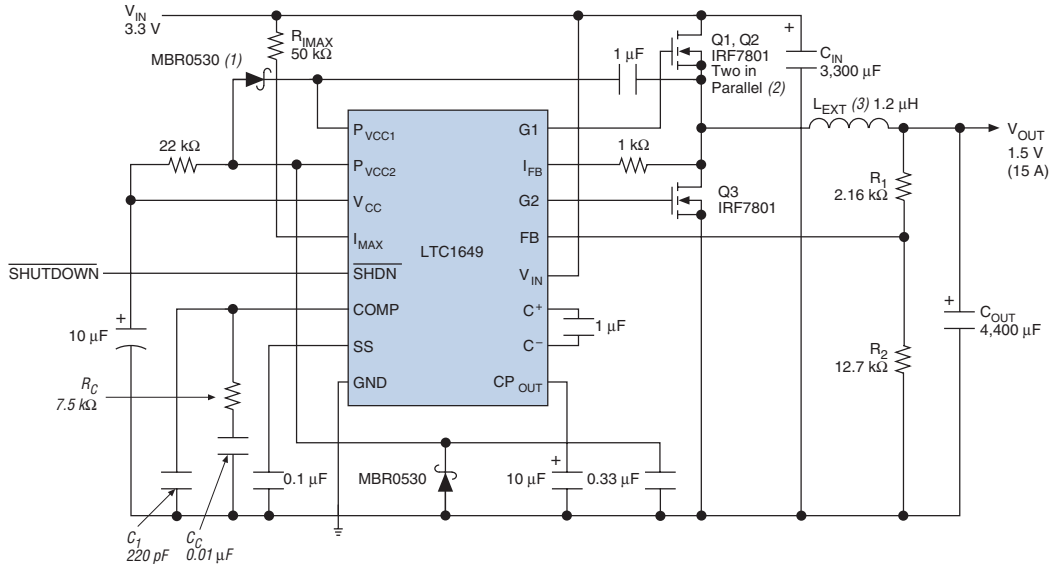
- (1) This capacitor is necessary to maintain the voltage level at the input regulator. There could be a voltage drop at the input if the voltage supply is too far away.

Figure 12–10. LT1085: 5.0-V-to-1.5-V/3-A Linear Voltage Regulator**Note to Figure 12–10:**

- (1) This capacitor is necessary to maintain the voltage level at the input regulator. There could be a voltage drop at the input if the voltage supply is too far away.

Figure 12–11 shows a high-efficiency switching regulator circuit diagram. A selectable resistor network controls the output voltage. The resistor values in Figure 12–11 are selected for 1.5-V output operation.

Figure 12–11. LT1649: 3.3-V-to-1.5-V/15-A Asynchronous Switching Regulator

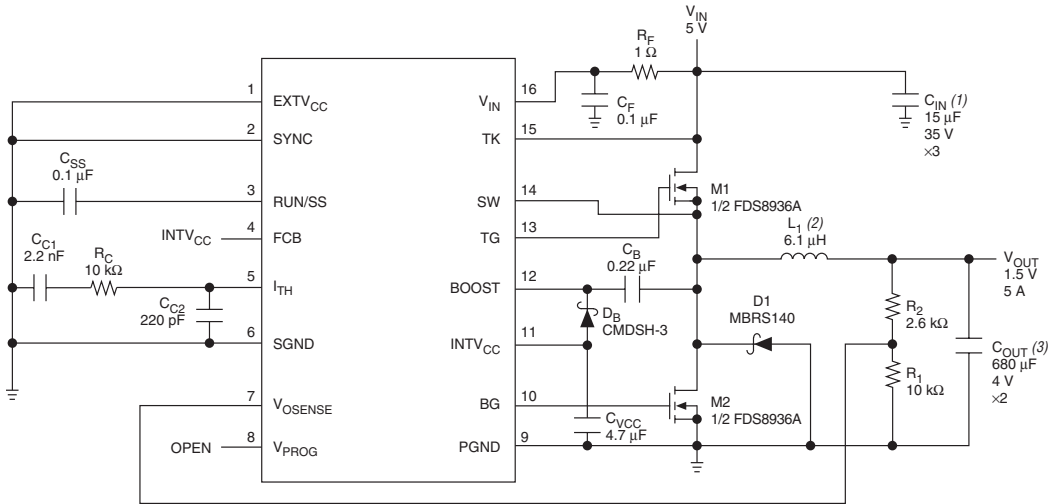


Notes to Figure 12–11:

- (1) MBR0530 is a Motorola device.
- (2) IRF7801 is a International Rectifier device.
- (3) Refer to the Panasonic 12TS-1R2HL device.

Figure 12–12 shows synchronous switching regulator with adjustable outputs.

Figure 12–12. LTC1775: 5.0-V-to-1.5-V/5-A Synchronous Switching Regulator



Notes to Figure 12–12:

- (1) This is a KEMETT495X156M035AS capacitor.
- (2) This is a Sumida CDRH127-6R1 inductor.
- (3) This is a KEMETT510X687K004AS capacitor.

Figures 12-13 through 12-17 show the circuit diagrams of Elantec voltage regulators listed in Table 12-6.

Figures 12-13 through 12-15 show the switching regulator that converts 5.0-V to 1.5-V with different output current.

Figure 12-13. EL7551C: 5.0-V-to-1.5-V/1-A Synchronous Switching Regulator

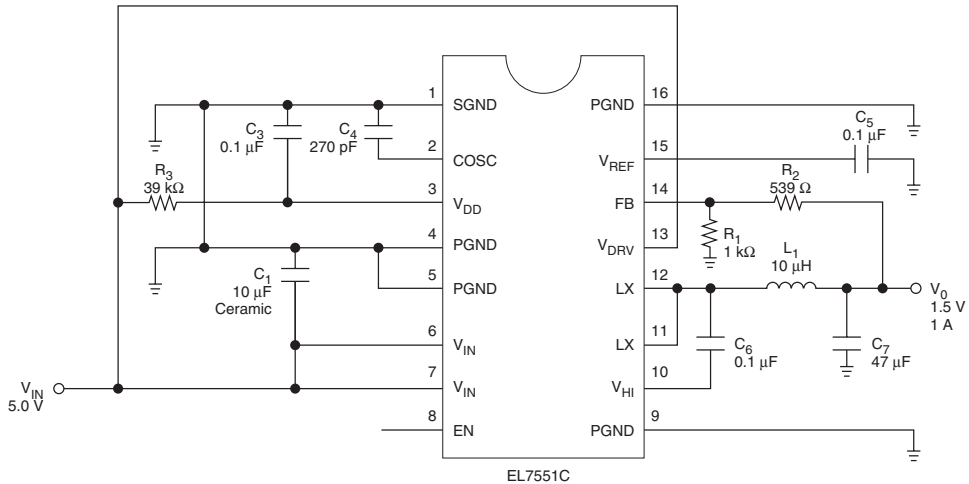


Figure 12–14. EL7564CM: 5.0-V-to-1.5-V/4-A Synchronous Switching Regulator

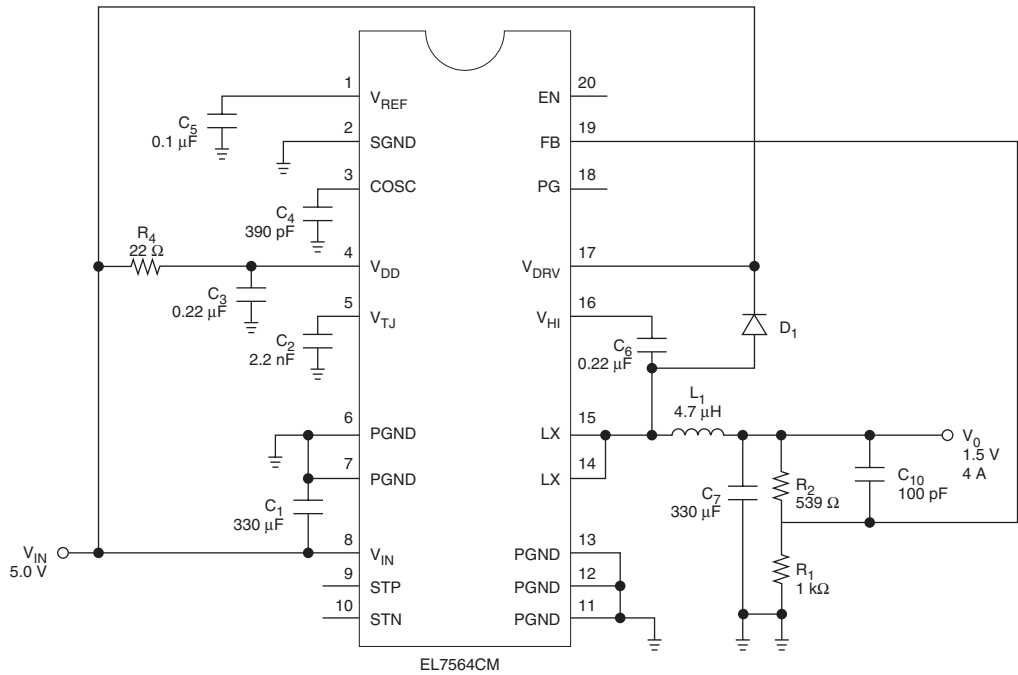
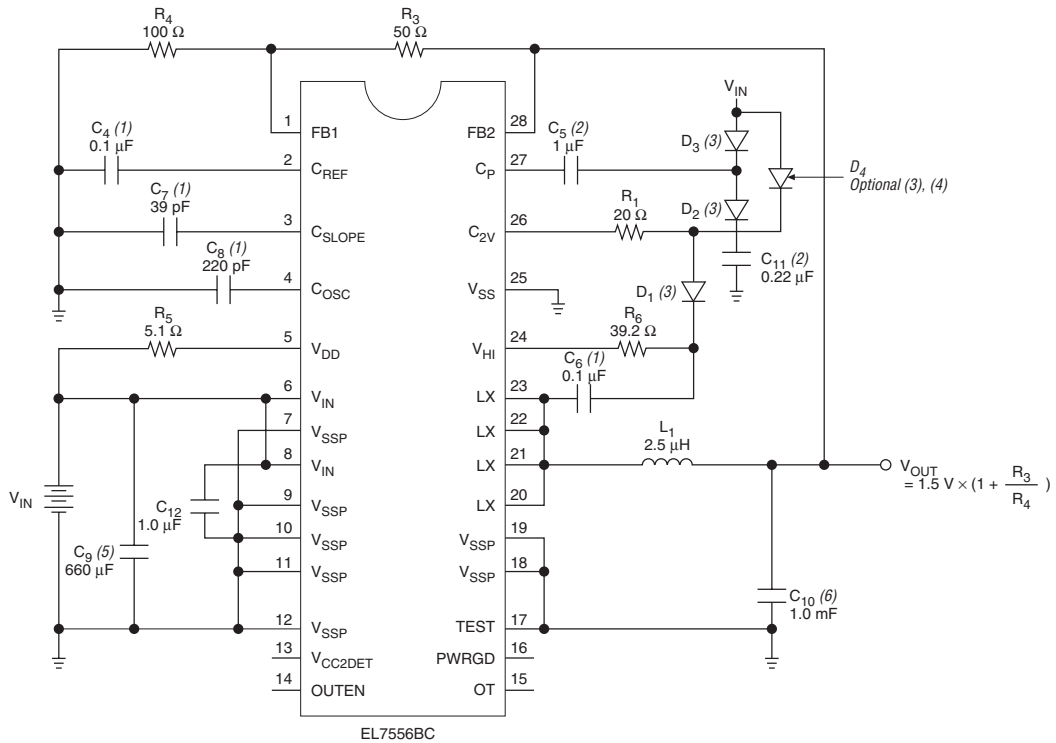


Figure 12–15. EL7556BC: 5.0-V-to-1.5-V/6-A Synchronous Switching Regulator



Notes to Figures 12–13 –12–15:

- (1) These capacitors are ceramic capacitors.
- (2) These capacitors are ceramic or tantalum capacitor.
- (3) These are BAT54S fast diodes.
- (4) D4 is only required for EL7556ACM.
- (5) This is a Sprague 293D337X96R3 2X330μF capacitor.
- (6) This is a Sprague 293D337X96R3 3X330μF capacitor.

Figures 12-16 and 12-17 show the switching regulator that converts 3.3 V to 1.5 V with different output currents.

Figure 12-16. EL7562CM: 3.3-V to 1.5-V/2-A Synchronous Switching Regulator

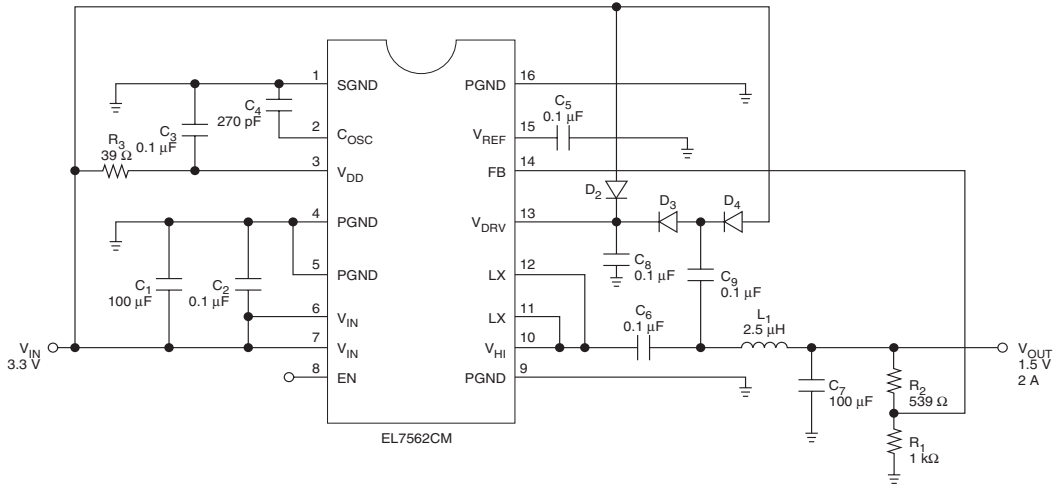
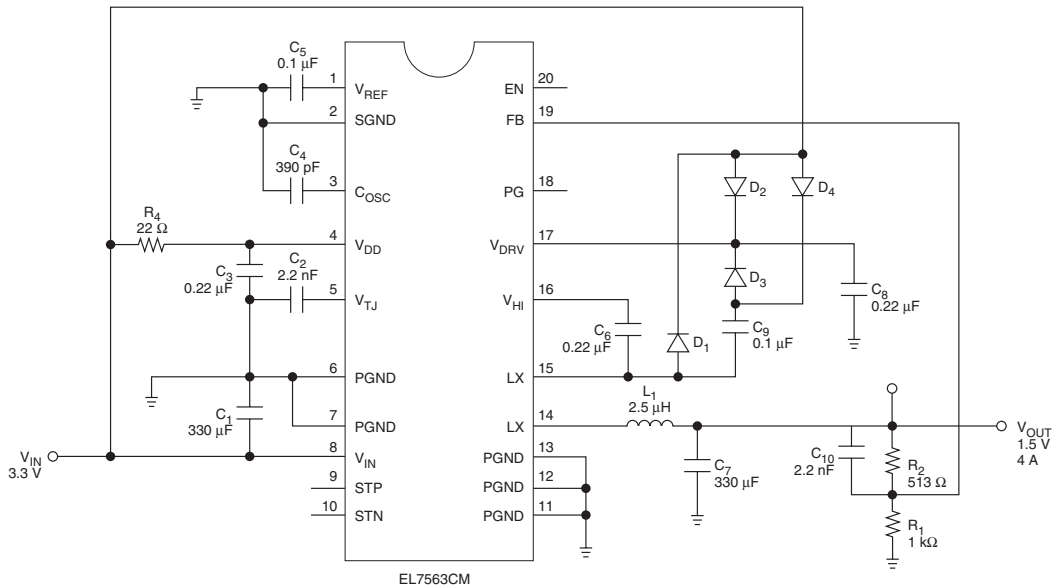


Figure 12-17. EL7563CM: 3.3-V to 1.5-V/4-A Synchronous Switching Regulator



1.5-V Regulator Application Examples

The following sections show the process used to select a voltage regulator for three sample designs. The regulator selection is based on the amount of power that the Cyclone device consumes. There are 14 variables to consider when selecting a voltage regulator. The following variables apply to Cyclone device power consumption:

- f_{MAX}
- Output and bidirectional pins
- Average toggle rate for I/O pins (to_{gIO})
- Average toggle rate for logic elements (LEs) (to_{gLC})
- User-mode I_{CC} consumption
- Maximum power-up I_{CCINT} requirement
- Utilization
- V_{CCIO} supply level
- V_{CCINT} supply level

The following variables apply to the voltage regulator:

- Output voltage precision requirement
- Supply voltage on the board
- Voltage supply output current
- Variance of board supply
- Efficiency

Different designs have different power consumptions based on the variables listed. Once you calculate the Cyclone device's power consumption, you must consider how much current the Cyclone device needs. You can use the Cyclone power calculator (available at www.altera.com) or the PowerGauge™ tool in the Quartus II software to determine the current needs. Also check the maximum power-up current requirement listed in the Power Consumption section of the Cyclone FPGA Family Data Sheet because the power-up current requirement may exceed the user-mode current consumption for a specific design.

Once you determine the minimum current the Cyclone device requires, you must select a voltage regulator that can generate the desired output current with the voltage and current supply that is available on the board using the variables listed in this section. An example is shown to illustrate the voltage regulator selection process.

Synchronous Switching Regulator Example

This example shows a worst-case scenario for power consumption where the design uses all the LEs and RAM. Table 12–7 shows the design requirements for 1.5-V design using a Cyclone EP1C12 FPGA.

Design Requirement	Value
Output voltage precision requirement	±5%
Supply voltages available on the board	3.3 V
Voltage supply output current available for this section ($I_{IN, DC(MAX)}$)	2 A
Variance of board supply (V_{IN})	±5%
f_{MAX}	150 MHz
Average t_{ogIO}	12.5%
Average t_{ogLC}	12.5%
Utilization	100%
Output and bidirectional pins	125
V_{CCIO} supply level	3.3 V
V_{CCINT} supply level	1.5 V
Efficiency	≥90%

Table 12–8 uses the checklist on page 12–8 to help select the appropriate voltage regulator.

Output voltage requirements	$V_{OUT} = 1.5 \text{ V}$
Supply voltages	V_{IN} OR $V_{CC} = 3.3 \text{ V}$
Supply variance from Linear Technology data sheet	Supply variance = ±5%
Estimated I_{CCINT} Use Cyclone Power Calculator	$I_{CCINT} = 620 \text{ mA}$
Estimated I_{CCIO} if regulator powers V_{CCIO} Use Cyclone Power Calculator (not applicable in this example because $V_{CCIO} = 3.3 \text{ V}$)	$I_{CCIO} = \text{N/A}$
Total user-mode current consumption $I_{CC} = I_{CCINT} + I_{CCIO}$	$I_{CC} = 620 \text{ mA}$

Table 12–8. Voltage Regulator Selection Process for EP1C12F324C Design (Part 2 of 2)

EP1C12 maximum power-up current requirement See Power Consumption section of the Cyclone FPGA Family Data Sheet for other densities	$I_{PUC(MAX)} = 900 \text{ mA}$
Maximum output current required Compare I_{CC} with $I_{PUC(MAX)}$	$I_{OUT(MAX)} = 900 \text{ mA}$
Voltage regulator selection See <i>Linear Technology LTC 1649 data sheet</i> See <i>Intersil (Elantec) EL7562C data sheet</i>	LTC1649 $I_{OUT(MAX)} = 15 \text{ A}$ EL7562C $I_{OUT(MAX)} = 2 \text{ A}$
LTC1649	
Nominal efficiency (η)	Nominal efficiency (η) = > 90%
Line and load regulation Line regulation + load regulation = $(0.17 \text{ mV} + 7 \text{ mV}) / 1.5 \text{ V} \times 100\%$	Line and Load Regulation = 0.478% < 5%
Minimum input voltage ($V_{IN(MIN)}$) $(V_{IN(MIN)}) = V_{IN}(1 - \Delta V_{IN}) = 3.3\text{V}(1 - 0.05)$	$(V_{IN(MIN)}) = 3.135 \text{ V}$
Maximum input current $I_{IN, DC(MAX)} = (V_{OUT} \times I_{OUT(MAX)}) / (\eta \times V_{IN(MIN)})$	$I_{IN, DC(MAX)} = 478 \text{ mA} < 2 \text{ A}$
EL7562C	
Nominal efficiency (η)	Nominal efficiency (η) = > 95%
Line and load regulation Line regulation + load regulation = $(0.17 \text{ mV} + 7 \text{ mV}) / 1.5 \text{ V} \times 100\%$	Line and Load Regulation = 0.5% < 5%
Minimum input voltage ($V_{IN(MIN)}$) $(V_{IN(MIN)}) = V_{IN}(1 - \Delta V_{IN}) = 3.3\text{V}(1 - 0.05)$	$(V_{IN(MIN)}) = 3.135 \text{ V}$
Maximum input current $I_{IN, DC(MAX)} = (V_{OUT} \times I_{OUT(MAX)}) / (\eta \times V_{IN(MIN)})$	$I_{IN, DC(MAX)} = 453 \text{ mA} < 2 \text{ A}$

Board Layout

Laying out a printed circuit board (PCB) properly is extremely important in high-frequency ($\geq 100 \text{ kHz}$) switching regulator designs. A poor PCB layout results in increased EMI and ground bounce, which affects the reliability of the voltage regulator by obscuring important voltage and current feedback signals. Altera recommends using Gerber files—pre-designed layout files—supplied by the regulator vendor for your board layout.

If you cannot use the supplied layout files, contact the voltage regulator vendor for help on re-designing the board to fit your design requirements while maintaining the proper functionality.

Altera recommends that you use separate layers for signals, the ground plane, and voltage supply planes. You can support separate layers by using multi-layer PCBs, assuming you are using two signal layers.

Figure 12–18 shows how to use regulators to generate 1.5-V and 2.5-V power supplies if the system needs two power supply systems. One regulator is used for each power supply.

Figure 12–18. Two Regulator Solution for Systems that Require 5.0-V, 2.5-V and 1.5-V Supply Levels

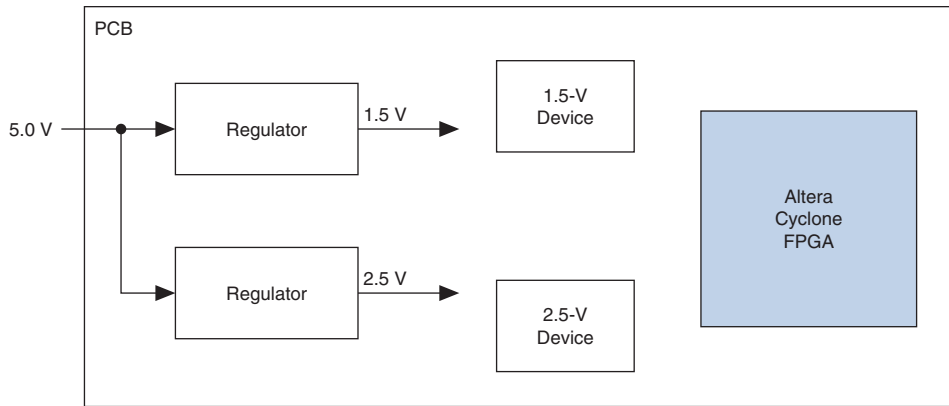
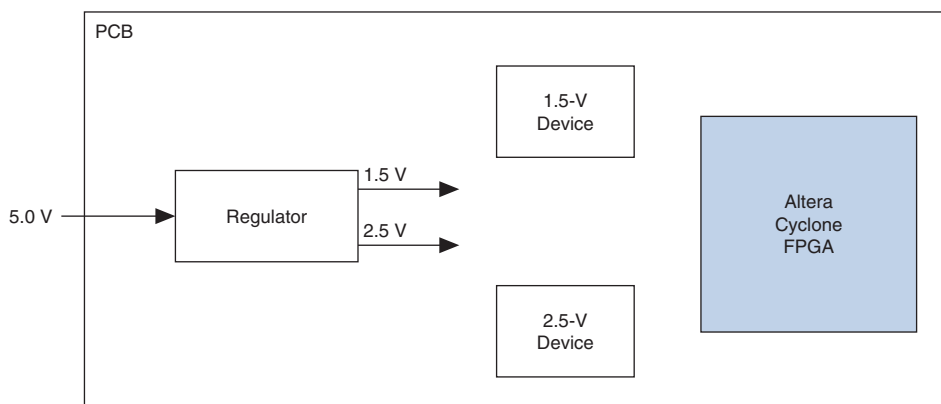


Figure 12–19 shows how to use a single regulator to generate two different power supplies (1.5-V and 2.5-V). The use of a single regulator to generate 1.5-V and 2.5-V supplies from the 5.0-V power supply can minimize the board size and thus save cost.

Figure 12–19. Single Regulator Solution for Systems that Require 5.0-V, 2.5-V and 1.5-V Supply Levels

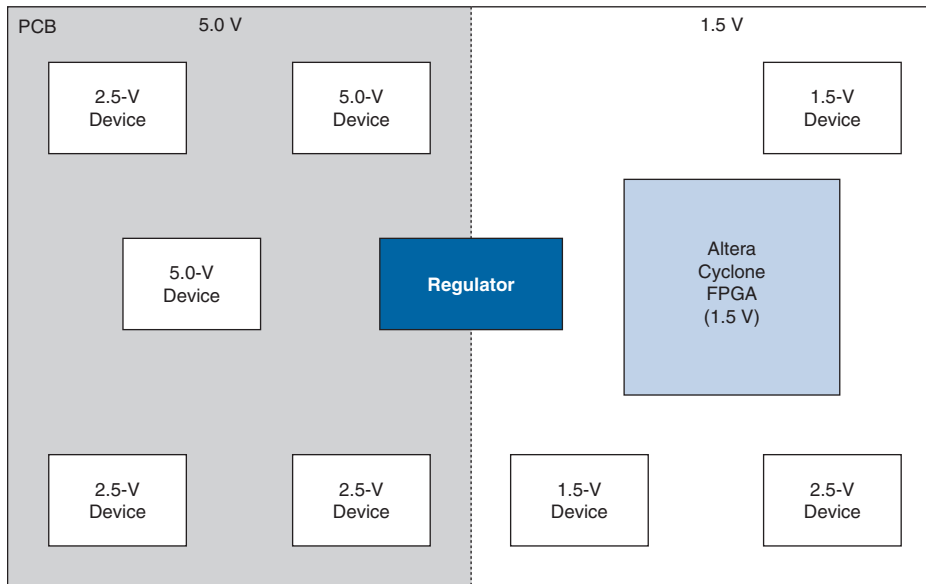


Split-Plane Method

The split-plane design method reduces the number of planes required by placing two power supply planes in one plane (see [Figure 12–20](#)). For example, the layout for this method can be structured as follows:

- One 2.5-V plane, covering the entire board
- One plane split between 5.0-V and 1.5-V

This technique assumes that the majority of devices are 2.5-V. To support MultiVolt I/O, Altera devices must have access to 1.5-V and 2.5-V planes.

Figure 12–20. Split Board Layout for 2.5-V Systems With 5.0-V and 1.5-V Devices

Conclusion

With the proliferation of multiple voltage levels in systems, it is important to design a voltage system that can support a low-power device like Cyclone devices. Designers must consider key elements of the PCB, such as power supplies, regulators, power consumption, and board layout when successfully designing a system that incorporates the low-voltage Cyclone family of devices.

References

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Intersil Corporation. *EL7563C Data Sheet (Monolithic 4 Amp DC:DC Step-Down Regulator)*. Milpitas: Intersil Corporation, 2002.

Referenced Documents

This chapter references the following document:

- *Cyclone FPGA Family Data Sheet* section of the *Cyclone Device Handbook*

Document Revision History

Table 12–9 shows the revision history for this chapter.

<i>Table 12–9. Document Revision History</i>		
Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.4	Minor textual and style changes. Added “Referenced Documents” section.	—
January 2007 v1.3	<ul style="list-style-type: none"> ● Added document revision history. ● Removed references to Stratix in “Introduction” and “Power Sequencing and Hot Socketing” sections. 	—
August 2005 v1.1	Minor updates.	—
May 2003 v1.0	Added document to Cyclone Device Handbook.	—

