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This chapter describes the design considerations that affect the external memory interface performance and the device resource usage when you use UniPHY IP in your design.

Core Logic and User Interface Data Rate

The clocking operation in the PHY is categorized into the following two domains:

- PHY-memory domain—the PHY interfaces with the external memory device and is always at full-rate.
- PHY-AFI domain—the PHY interfaces with the memory controller and can either be at full, half or quarter rate of the memory clock depending on your choice of controller and PHY.

For the memory controller to operate at full, half and quarter data rate, the UniPHY IP supports full, half and quarter data rate. The data rate defines the ratio between the frequency of the Altera® PHY Interface (AFI) clock and the frequency of the memory device clock.

Table 14–2 compares the clock cycles, data bus width and address/command bus width between the full-, half-, and quarter-rate designs.

Table 14–1. Ratio between Clock Cycles, Data Bus Width, and Address/Command Bus Width

Data Rate	Controller Clock Cycles	Bus Width	
		AFI Data	AFI Address/Command
Full	1	2	1
Half	2	4	2
Quarter	4	8	4

In general, full-rate designs require smaller data and address/command bus width. However, because the core logic runs at a high frequency, full rate designs might have difficulties in closing timing. As such, for high frequency memory interface designs, Altera recommends that you use half-rate or quarter-rate UniPHY IP and controllers.

DDR3 SDRAM interfaces are capable of running at much higher frequencies as compared to the DDR, DDR2 SDRAM, QDRII, QDRII+ SRAM, and RLDRAM II interfaces. For this reason, Altera High-Performance Controller II and UniPHY IPs do not support full rate designs using the DDR3 SDRAM interface. However, DDR3 hard controller in Arria® V devices only support full rate. Quarter rate design support is for DDR3 SDRAM interfaces targeting frequencies higher than 667 MHz.

While it is easier to close timing for half-rate and quarter-rate designs due to the lower frequency required on the core logic, full-rate interface offer better efficiency for low burst-length designs because of 1T addressing mode where the address and command signals are asserted for one memory clock cycle. Typically half-rate and quarter-rate designs operate in 2T and 4T mode, respectively, in which the address & command signals in 2T and 4T mode must be asserted for two and four memory clock cycles, respectively. To improve efficiency, the controller can operate in Quasi-1T half-rate and Quasi-2T quarter-rate modes. In Quasi-1T half-rate mode, two commands are issued to the memory on two memory clock cycles. In Quasi-2T quarter-rate mode, two commands are issued to the memory on four memory clock cycles. The controller is constrained to issue a row command on the first clock phase and a column command on the second clock phase, or vice versa. Row commands include activate and precharge commands; column commands include read and write commands.

Hard and Soft Memory PHY

The Arria V and Cyclone® V device families support hard and soft memory interfaces. Hard memory interfaces use the hard memory controllers and hard memory PHY blocks in the devices.

Currently the hard memory PHY is instantiated together with the hard memory controller. In addition to the PHY data path that uses the hard IP blocks in the devices (similar to how the soft PHY is implemented for device families supported by UniPHY), the hard memory PHY also uses the dedicated hardware circuitries in the devices for certain component managers in the sequencer, including the read write (RW) and PHY managers.

Standalone hard memory PHY instantiation will be supported in future versions of the Quartus® II software.

In soft memory PHY, the UniPHY sequencer implements the Nios® II processor and all the component managers in the core logic. The hard memory PHY uses dedicated hard IP blocks in the Arria V and Cyclone V devices to implement the RW and PHY managers to save LE resources, and to allow better performance and lower latency.

Each Arria V and Cyclone V device has a fixed number of hard PHYs. Dedicated I/O pins with specific functions for data, strobe, address, command, control, and clock must be used together with each hard PHY.

For the list of hard PHY dedicated pins, refer to the device pin-out files for your target device on the Pin-Out Files for Altera Devices page of the Altera website.

Using the soft memory PHY gives you the flexibility to choose the pins to be used for the memory interface. Soft memory PHY also supports wider interfaces as compared to hard memory PHY.

Sequencer

Starting from Quartus II software version 11.0, the UniPHY IP soft memory PHY supports the following two types of sequencer used for QDRII and QDRII+ SRAM, and RLDRAM II calibration:

- RTL-based sequencer
- Nios II-based sequencer

The RTL-based sequencer performs FIFO calibration that includes adjusting the valid-prediction FIFO (VFIFO) and latency FIFO (LFIFO) length. On top of the FIFO calibration, the Nios II-based sequencer also performs I/O calibration that includes adjusting delay chains and phase settings to center-align the data pins with respect to the strobes that sample them. I/O calibration is required for memory interfaces running at higher frequencies to increase the read and write margin.

Because the RTL-based sequencer performs relatively simpler calibration process, it does not require a Nios II processor. For this reason, the resource utilization like LE and RAM usage is lower as compared to the Nios II-based sequencer.

For more information about the RTL-based sequencer and Nios II-based sequencer, refer to the *Functional Description—UniPHY* chapter in volume 3 of the *External Memory Interface Handbook*.

For more information about the calibration process, refer to the "UniPHY Calibration Stages" section in the *Functional Description—UniPHY* chapter of the *External Memory Interface Handbook*.

PLL, DLL and OCT Resource Sharing

By default, each external memory interface in a device needs one PLL, one DLL and one OCT control block. Due to the fixed number of PLL, DLL and OCT resources available in a device, these resources can be shared by two or more memory interfaces when certain criterias are met. This method allows more memory interfaces to fit into a device and allows the remaining resources to be used for other purposes.

By sharing PLLs, apart from reducing the number of PLLs to be used, the number of clock networks and the clock input pins required are also reduced. To share PLLs, the memory interfaces must meet the following criterias:

- Run the same memory protocol (for example, DDR3 SDRAM)
- Run at the same frequency
- The controllers or PHYs run at the same rate (for example, half rate)
- Use the same phase requirements (for example, additional core-to-periphery clock phase of 90°)
- The memory interfaces are located on the same side of the device, or adjacent sides of the device if the PLL is able to drive both sides.

Altera devices have up to four DLLs available to perform phase shift on the DQS signal for capturing the read data. The DLLs are located at the device corners and some of the DLLs can access two adjacent sides of the device. To share DLLs, the memory interfaces must meet the following criterias:

- Run at the same frequency
- The memory interfaces are located on the same side of the device, or adjacent sides of the device accessible by the DLL.

Memory interface pins with OCT calibration requires the OCT control block to calibrate the OCT resistance value. Depending on the device family, the OCT control block uses either the RUP and RDN, or RZQ pins for OCT calibration. Each OCT control block can only be shared by pins powered by the same VCCIO level. Sharing of the OCT control block by interfaces operating at the same VCCIO level allows other OCT control blocks in the device to support other VCCIO levels. The unused RUP/RDN or RZQ pins can also be used for other purposes. For example, the RUP/RDN pins can be used as DQ or DQS pins. To share OCT control block, the memory interfaces must operate at the same VCCIO level.

For more information about the resources required for memory interfaces in various device families, refer to the *Planning Pin and FPGA Resources* chapter.

For more information about how to share PLL, DLL and OCT control block, refer to the *Functional Description—UniPHY* chapter in volume 3 of the *External Memory Interface Handbook*.

For more information about the DLL, refer to the external memory interface chapters in the respective device handbooks.

For more information about the OCT control block, refer to the I/O features chapters in the respective device handbooks.

Pin Placement Consideration

The Stratix® V, Arria V, and Cyclone V device families use the PHY clock (PHYCLK) networks to clock the external memory interface pins for better performance. Each PHYCLK network is driven by a PLL. In Cyclone V and Stratix V devices, the PHYCLK network spans across two I/O banks on the same side of the device, whereas for Arria V devices, each PHYCLK network spans across one I/O bank. As such, all pins for a memory interface must be placed on the same side of the device.

For more information about pin placement guidelines related to the PHYCLK network, refer to the *External Memory Interfaces in Stratix V Devices* chapter in volume 2 of the *Stratix V Device Handbook*, *External Memory Interfaces in Arria V Devices* chapter in volume 2 of the *Arria V Device Handbook*, or the *External Memory Interfaces in Cyclone V Devices* chapter in volume 2 of the *Cyclone V Device Handbook*.

Wraparound interface, in which data pins from a memory interface are placed on two adjacent sides of a device, and split interface, in which data pins are place on two opposite I/O banks, are supported in certain device families that do not use the PHY clock network to allow more flexibility in pin placement.

The x36 emulated mode is supported in certain device families that do not use the PHY clock network for QDRII and QDRII+ SRAM x36 interfaces. In x36 emulated mode, two x18 DQS groups or four x9 DQS groups can be combined to form a 36-bit wide write data bus, while two x18 DQS groups can be combined to form a 36-bit wide read data bus. This method allows a device to support x36 QDRII and QDRII+ SRAM interfaces even if the device does hot have the required number of x36 DQS groups.

Some device families might support wraparound or x36 emulated mode interfaces at slightly lower frequencies.

For information about the devices that support wraparound and x36 emulated mode interfaces, and the supported frequency for your design, refer to the External Memory Interface Spec Estimator page on the Altera website

For more information about x36 emulated mode support for QDRII and QDRII+ SRAM interfaces, refer to the *Planning Pin and FPGA Resources* chapter.

Document Revision History

Table 14–2 lists the revision history for this document.

Table 14–2. Document Revision History

Date	Version	Changes
November 2011	1.0	Initial release.