

This chapter describes the UniPHY External Memory Interface Toolkit. It explains how to enable, launch, and run the toolkit, and provides a guide for interpreting results and troubleshooting. This toolkit is a Tcl-based interface that runs on your PC and enables you to debug your external memory interface design on the circuit board, retrieve calibration status, and perform margining activities.



This toolkit supports only the DDR2 and DDR3 SDRAM Controllers with UniPHY.

## Feature Description

The External Memory Interface Toolkit consists of the following parts:

- DDR2 and DDR3 SDRAM Controllers with UniPHY
- Avalon Memory-Mapped (Avalon-MM) slave interface
- JTAG Avalon master

The EMIF toolkit allows you to display information about your external memory interface and generate calibration and margining reports. The toolkit can aid in diagnosing the type of failure that may be occurring in your external memory interface, and help identify areas of reduced margin that might be potential failure points.

## Using the External Memory Interface Toolkit

Using the external memory interface toolkit to analyze your external memory interface involves the following steps:

1. (Optional) Generating your IP core with the CSR port enabled and with the CSR communication interface type properly set.
2. Launching the debug toolkit.
3. Specifying project settings.
4. Using the toolkit to view information about your interface.
5. Interpreting results and troubleshooting your interface.

The following sections discuss each of the above steps in detail.

## Enabling Communication with the Controller via the CSR Port

Optionally, you can enable communication between the EMIF toolkit and the memory controller through the Configuration and Status Register (CSR) port on the controller.

You do not have to enable the CSR port in order to use the toolkit's report-generation functions; however, enabling the CSR port provides the following additional capabilities:

- allows the toolkit to verify memory device operation by determining whether the controller receives DQS edges from the memory device
- allows the toolkit to issue soft resets to the memory interface
- allows the toolkit to monitor PLL locked status

Before the toolkit can communicate with the controller through the CSR port, you must enable the CSR port from the Controller Settings tab of your memory interface parameter editor, as described in the following steps:

1. Open the DDR2 or DDR3 SDRAM Controller with UniPHY parameter editor from the MegaWizard Plug-in Manager, SOPC Builder, or Qsys.
2. Under **Advanced Controller Features** on the **Controller Settings** tab, specify the following options:
  - a. Turn on **Enable Configuration and Status Register Interface**.
  - b. Set **CSR port host interface** to INTERNAL\_JTAG.
3. Regenerate the IP core.
4. Compile your design in the Quartus II software.
5. Program the Altera FPGA device using the programming file from your project.

Figure 11-1 illustrates the external memory interface components with the optional CSR port and JTAG Avalon master configured.

**Figure 11-1. External Memory Interface with CSR Port Configured**

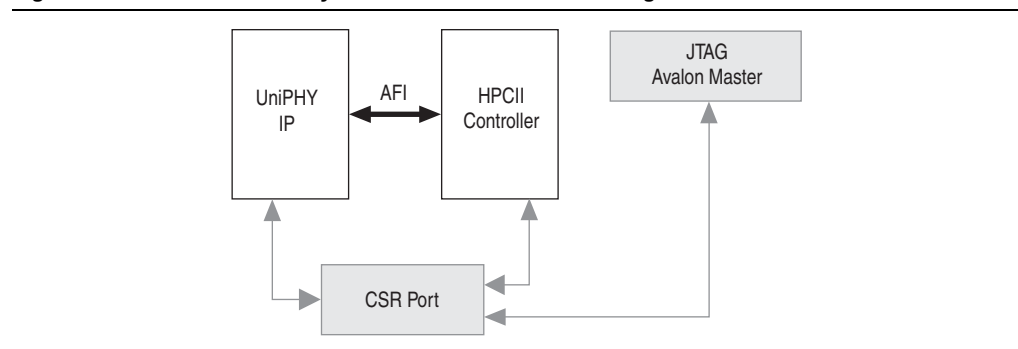


Table 11-1 shows the UniPHY and High Performance Controller II CSR address map.

**Table 11-1. CSR Address Map**

Address	Bit	Name	Default	Access	Description
0x001	15:0	Reserved	0	—	Reserved for future use.
	31:16				
0x002	15:0				
	31:16				
0x004	0	SOFT_RESET	—	WO	Initiates a soft reset of the memory interface. This bit is automatically deasserted when reset is completed.
	23:1	Reserved	0	—	Reserved for future use.
	24	AFI_CAL_SUCCESS	—	RO	Reports the value of the UniPHY <code>afi_cal_success</code> output. Writing to this bit has no effect.
	25	AFI_CAL_FAIL	—	RO	Reports the value of the UniPHY <code>afi_cal_fail</code> output. Writing to this bit has no effect.
	31:26	Reserved	0	—	Reserved for future use.
0x005	7:0	FOM_IN	—	RO	The figure of merit <sup>(1)</sup> for read as calculated by the sequencer. Only applicable if <code>AFI_CAL_SUCCESS</code> is 1.
	15:8	Reserved	0	—	Reserved for future use.
	23:16	FOM_OUT	—	RO	The figure of merit <sup>(1)</sup> for write as calculated by the sequencer. Only applicable if <code>AFI_CAL_SUCCESS</code> is 1.
	31:24	Reserved	0	—	Reserved for future use.
0x006	7:0	INIT_FAILING_STAGE	—	RO	In cases of calibration failure, shows a binary representation of the stage at which failure occurred. <sup>(2)</sup>
	15:8	Reserved	0	—	Reserved for future use
	23:16	INIT_FAILING_GROUP	—	RO	In cases of calibration failure, shows a binary representation of the group that was being calibrated at the time of failure. <sup>(2)</sup>
	31:24	Reserved	0	—	Reserved for future use
0x007	31:0	DQS_DETECT	—	RO	Indicates whether DQS edges have been identified for each group. Each bit corresponds to 1 DQS group.

**Note to Table 11-1:**

- (1) The figure of merit (FOM) is a measure of the health of the read (or write) interface; it is calculated as the sum over all groups of the minimum margin on DQ plus the margin on DQS, divided by 2.
- (2) In cases of calibration failure, values are valid only if failure occurred during the Read Calibration, Write Leveling, or Write Per-bit deskew and Centering stages of calibration. Values are not valid if failure occurred during Read Latency Tuning.

## Launching the External Memory Interface Debug Toolkit

To launch the debug toolkit from the Quartus II software, perform the following steps:

1. Program the Altera FPGA device using the programming file from your project.
2. To open the External Memory Interface Toolkit in the System Console, click **External Memory Interface Toolkit** on the **Tools** menu in the Quartus II software.
3. On the File menu in the System Console window, select **Load Design** to load your Quartus II Project File (.qpf) into the EMIF toolkit. When your project is loaded, your design folder appears under **designs** in the System Explorer tree.
4. In the System Explorer tree, right-click the *<instance\_name>.qpf* file in your design folder, and click **Link design instance to device** to link the design instance to the target device.
5. Under **Hardware Setup**, click **Apply Linked Design** to load the project. Your interface connection now appears under **New Memory Interface Connection**.
6. Under **Hardware Setup** on the **External Memory Interface Toolkit** tab, select your hardware and device. The **Hardware** list shows all the detected connections between your board and the PC; the **Device** list shows all the devices on your board, detected by the selected connection.
7. If you have more than one interface, select the interface you want from the **Memory Interface** list, under **New Memory Interface Connection**.

Once you have selected your interface, the **New Memory Interface Connection** group box displays the UniPHY instance name, and—if you have set up communication with the CSR port—the CSR instance name and PLL status.

8. Under **New Memory Interface Connection**, click **Establish Connection** to create a tab for your external memory interface.

You can optionally repeat this step to create tabs for any other external memory interfaces in your design.

9. If you turn on the **Efficiency Monitor and Protocol Checker** option in your design, under **New Efficiency Monitor Connection**, select the efficiency monitor instance from the **Efficiency Monitor** list.
10. Click **Establish Connection** to create a tab for the efficiency monitor and protocol checker.

## Specifying Project Settings

Before rerunning calibration or generating reports, you must establish project settings to allow for correct calibration and margining results. To establish the project settings, perform the following steps:

1. On the **Project Settings** tab, ensure the **Settings Type** field is set to **Device Settings**.
2. Under **Project FPGA Settings**, select values for the **FPGA Family** and **FPGA Speedgrade**.
3. Under **Project PLL Settings**, type your memory interface frequency.

4. Click **Update Project Settings** to save the information for your project in memory.

## Viewing Information About Your External Memory Interface

The following steps explain how to use the External Memory Interface Toolkit to view information about your interface.

1. When you establish a connection for your memory interface, a memory interface tab appears in the External Memory Interface Toolkit parameter editor.
2. In the memory interface tab, go to **Memory Interface Status and Control** tab and click **Generate Calibration Report** to generate detailed calibration information for your interface.
3. To view the calibration report, on the **Reports** tab, under **Report Type**, select **Calibration report per DQ group** or **Calibration report**.

The Calibration report per DQ group lists read and write data valid windows and calibration status for each group and rank.


The Calibration report is comprehensive, and includes the following information:

- Group and rank mask status
  - Calibration status
  - Margins observed during calibration, per DQ group
  - DQ and DQS I/O settings
4. To view read and write margining and data valid window information, click **Generate margining report**.
  5. Under **Report Type**, select **Margining Report** or **DVW Report**.

The Margining report lists each DQ pin and DQS group margin observed following calibration. Any reduced margins on DQ pins can be indicative of possible problems with the PCB layout of the memory interface.

The DVW report is a graphical representation of the Margining report, and can help you visualize the range of the data valid window per DQ pin. The black line in the report represents the point within the window to which the DQ pin is calibrated.

6. Click **Save Report** to save all generated reports in HTML format on your computer.

 You cannot save the DVW report.

7. On the **Summary** tab, select **Connection Summary** to review the interface and its connection properties.
8. If you have turned on the **Efficiency Monitor and Protocol Checker** option in your design, and established the efficiency monitor connection, an efficiency monitor tab appears in the External Memory Interface Toolkit parameter editor.

9. In the efficiency monitor tab, use the **Efficiency Monitor Controls** parameters to do the following tasks:
  - Start or stop the efficiency monitor
  - Reset the efficiency monitor
  - Reset the protocol checker
  - Read the efficiency monitor data
10. On the **Summary** tab, you get the following details:
  - Interface and efficiency monitor connection properties
  - Efficiency monitor properties summary
  - Efficiency monitor statistics summary
  - Protocol checker summary
11. Select **Result Summary** to display read and write latency values, as well as the DQS Captured Status. (If your design does not contain a CSR port, or you have not enabled the CSR port for use, the DQS Captured Status is not available.)

 For information about using the CSR port, refer to “[Enabling Communication with the Controller via the CSR Port](#)” on page 11-2.

## Interpreting Results and Troubleshooting

This section provides information on how to interpret the results returned by the toolkit.

### Calibration Successful

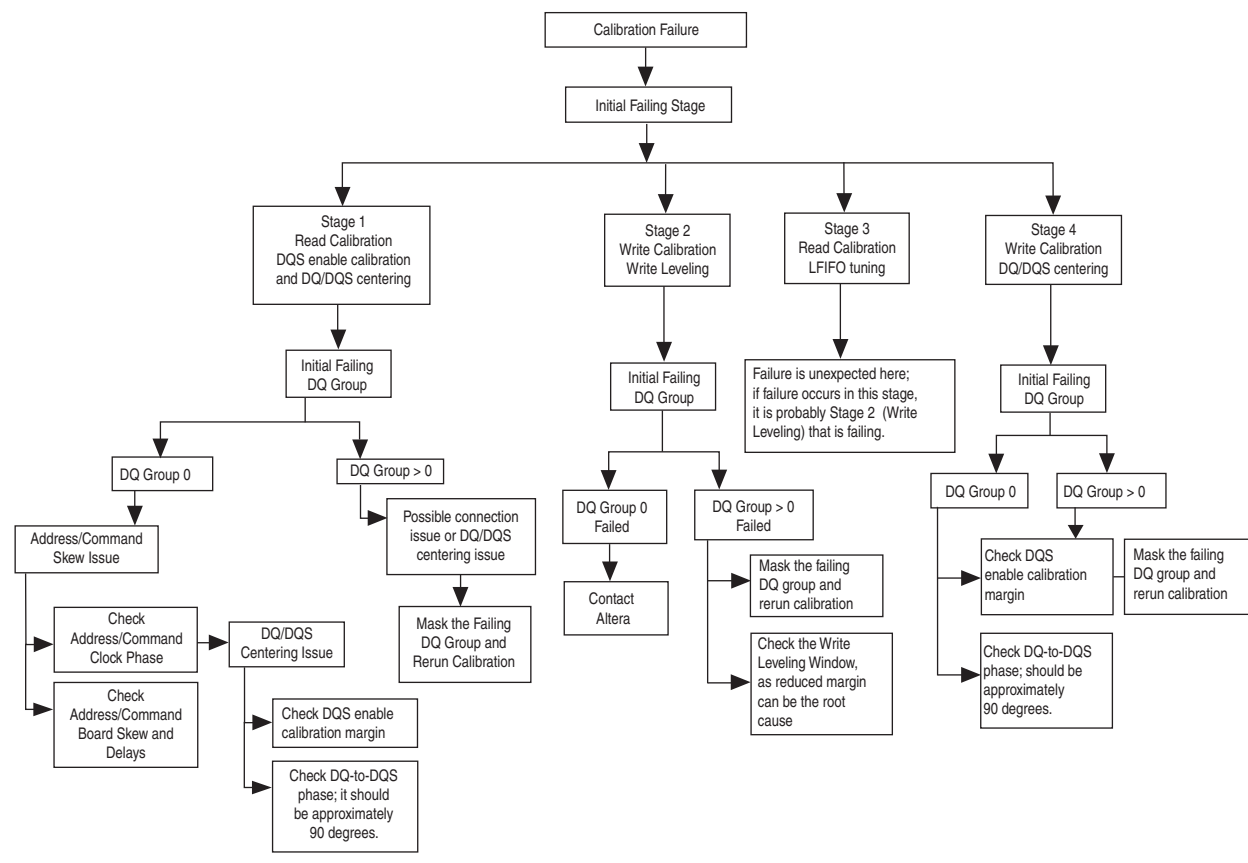
When both calibration and post-calibration tests complete successfully, you can use the debug toolkit to retrieve information about your memory interface and to identify areas of reduced margin. DQ pins with small margins tend to be the pins most susceptible to the effects of data corruption, board delays, and noise.


### Calibration Failed

In the event of calibration failure, you should check the DQS Capture Status in the Summary results to verify that the memory interface is functioning. If DQS edges are not detected, it is likely that the memory interface is not functioning. If DQS edges are detected, refer to [Figure 11-2](#) to assist in troubleshooting your design.

Figure 11-2 shows a flowchart of debugging tips to assist in resolving calibration failure.

Figure 11-2. Debugging Tips



 For detailed information about each calibration stage, refer to [UniPHY Calibration Stages](#) in section 1 of this volume.

## Document Revision History

Table 11-2 lists the revision history for this document.

Table 11-2. Document Revision History

Date	Version	Changes
November 2011	1.0	Harvested 11.0 DDR2 and DDR3 SDRAM Controller with UniPHY EMIF Toolkit content.

