

Altera defines read and write latencies in terms of memory clock cycles. There are two types of latencies that exist while designing with memory controllers—read and write latencies, which have the following definitions:

- Read latency—the amount of time it takes for the read data to appear at the local interface after initiating the read request.
- Write latency—the amount of time it takes for the write data to appear at the memory interface after initiating the write request.

For a half-rate controller, the local side frequency is half of the memory interface frequency. For a full-rate controller, the local side frequency is equal to the memory interface frequency.

Simulating the whole memory interface is a good way to determine the latency of your system. However, the latency found in simulation may be different than the latency found on the board because functional simulation does not take into account board trace delays and different process, voltage, and temperature scenarios. For a given design on a given board, the latency found may differ by one clock cycle (for full-rate designs) or two clock cycles (for half-rate or quarter-rate designs) upon resetting the board. Different boards can also show different latencies even with the same design.

## DDR2 and DDR3

Table 9–1 shows the DDR2 SDRAM latency in full rate memory clock cycles.

**Table 9–1. DDR2 SDRAM Controller Latency (In Full-Rate Memory Clock Cycles) <sup>(1)</sup> <sup>(2)</sup>**

Latency in Full-Rate Memory Clock Cycles							
Rate	Controller Address & Command	PHY Address & Command	Memory Maximum Read	PHY Read Return	Controller Read Return	Round Trip	Round Trip Without Memory
Half	10	EWL: 3	3–7	6	4	EWL: 26–30	EWL: 23
		OWL: 4				OWL: 27–31	OWL: 24
Full	5	0	3–7	4	10	27–31	24

**Notes:**

- (1) EWL = Even write latency
- (2) OWL = Odd write latency

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Table 9-2 shows the DDR3 SDRAM latency in full rate memory clock cycles.

**Table 9-2. DDR3 SDRAM Controller Latency (In Full-Rate Memory Clock Cycles) <sup>(1) (2) (3) (4)</sup>**

Latency in Full-Rate Memory Clock Cycles							
Rate	Controller Address & Command	PHY Address & Command	Memory Maximum Read	PHY Read Return	Controller Read Return	Round Trip	Round Trip Without Memory
Quarter	20	EWER : 8	5-11	EWER: 16	8	EWER: 57-61	EWER: 52
		EWOR: 8		EWOR: 17		EWOR: 58-62	EWOR: 53
		OWER: 11		OWER: 17		OWER: 61-65	OWER: 56
		OWOR: 11		OWOR: 14		OWOR: 58-62	OWOR: 53
Half	10	EWER: 3	5-11	EWER: 7	4	EWER: 29-35	EWER: 24
		EWOR: 3		EWOR: 6		EWOR: 28-34	EWOR: 23
		OWER: 4		OWER: 6		OWER: 29-35	OWER: 24
		OWOR: 4		OWOR: 7		OWOR: 30-36	OWOR: 25
Full	5	0	5-11	4	10	24-30	19

**Notes:**

- (1) EWER = Even write latency and even read latency
- (2) EWOR = Even write latency and odd read latency
- (3) OWER = Odd write latency and even read latency
- (4) OWOR = Odd write latency and odd read latency

## QDR II and QDR II+

Table 9-3 shows the latency in full rate memory clock cycles.

**Table 9-3. QDR II Latency (In Full-Rate Memory Clock Cycles) (Part 1 of 2) <sup>(1)</sup>**

Latency in Full-Rate Memory Clock Cycles							
Rate	Controller Address & Command	PHY Address & Command	Memory Maximum Read	PHY Read Return	Controller Read Return	Round Trip	Round Trip Without Memory
Half	2	1	1.5, 2.0, 2.5	RL 1.5: 5.5	0	RL 1.5: 10	RL 1.5: 8.5
				RL 2.0: 5.0		RL 2.0: 10	RL 2.0: 8
				RL 2.5: 4.5		RL 2.5: 10	RL 2.5: 7.5

**Table 9-3. QDR II Latency (In Full-Rate Memory Clock Cycles) (Part 2 of 2) <sup>(1)</sup>**

Latency in Full-Rate Memory Clock Cycles							
Rate	Controller Address & Command	PHY Address & Command	Memory Maximum Read	PHY Read Return	Controller Read Return	Round Trip	Round Trip Without Memory
Full	1	1	1.5, 2.0, 2.5	RL 1.5: 4.5	0	RL 1.5: 8	RL 1.5: 6.5
				RL 2.0: 4.0		RL 2.0: 8	RL 2.0: 6.0
				RL 2.5 :4.5		RL 2.5: 9	RL 2.5: 6.5

**Note:**

(1) RL = Read latency

## RLDRAM II

Table 9-4 shows the latency in full rate memory clock cycles.

**Table 9-4. RLDRAM II Latency (In Full-Rate Memory Clock Cycles) <sup>(1)</sup> <sup>(2)</sup>**

Latency in Full-Rate Memory Clock Cycles							
Rate	Controller Address & Command	PHY Address & Command	Memory Maximum Read	PHY Read Return	Controller Read Return	Round Trip	Round Trip Without Memory
Half	4	EWL: 1	3-8	EWL: 4	0	EWL: 12-17	EWL: 9
		OWL: 2		OWL: 4		OWL: 13-18	OWL: 10
Full	2	1	3-8	4	0	10-15	7

**Notes:**

(1) EWL = Even write latency

(2) OWL = Odd write latency

## Variable Controller Latency

The variable controller latency feature allows you to take advantage of lower latency for variations designed to run at lower frequency. When deciding whether to vary the controller latency from the default value of 1, be aware of the following considerations:

- Reduced latency can help achieve a reduction in resource usage and clock cycles in the controller, but might result in lower  $f_{MAX}$ .
- Increased latency can help achieve greater  $f_{MAX}$ , but might consume more clock cycles in the controller and result in increased resource usage.

If you select a latency value that is inappropriate for the target frequency, the system displays a warning message in the text area at the bottom of the parameter editor.

You can change the controller latency by altering the value of the **Controller Latency** setting in the **Controller Settings** section of the **General Settings** tab of the QDR II and QDR II+ SRAM controller with UniPHY parameter editor.

## Document Revision History

Table 9-5 lists the revision history for this document.

**Table 9-5. Document Revision History**

Date	Version	Changes
November 2011	1.0	<ul style="list-style-type: none"> <li data-bbox="505 407 1425 495">■ Consolidated latency information from 11.0 <b>DDR2 and DDR3 SDRAM Controller with UniPHY User Guide, QDR II and QDR II+ SRAM Controller with UniPHY User Guide, and RLDRAM II Controller with UniPHY IP User Guide.</b></li> <li data-bbox="505 506 760 533">■ Updated data for 11.1.</li> </ul>