

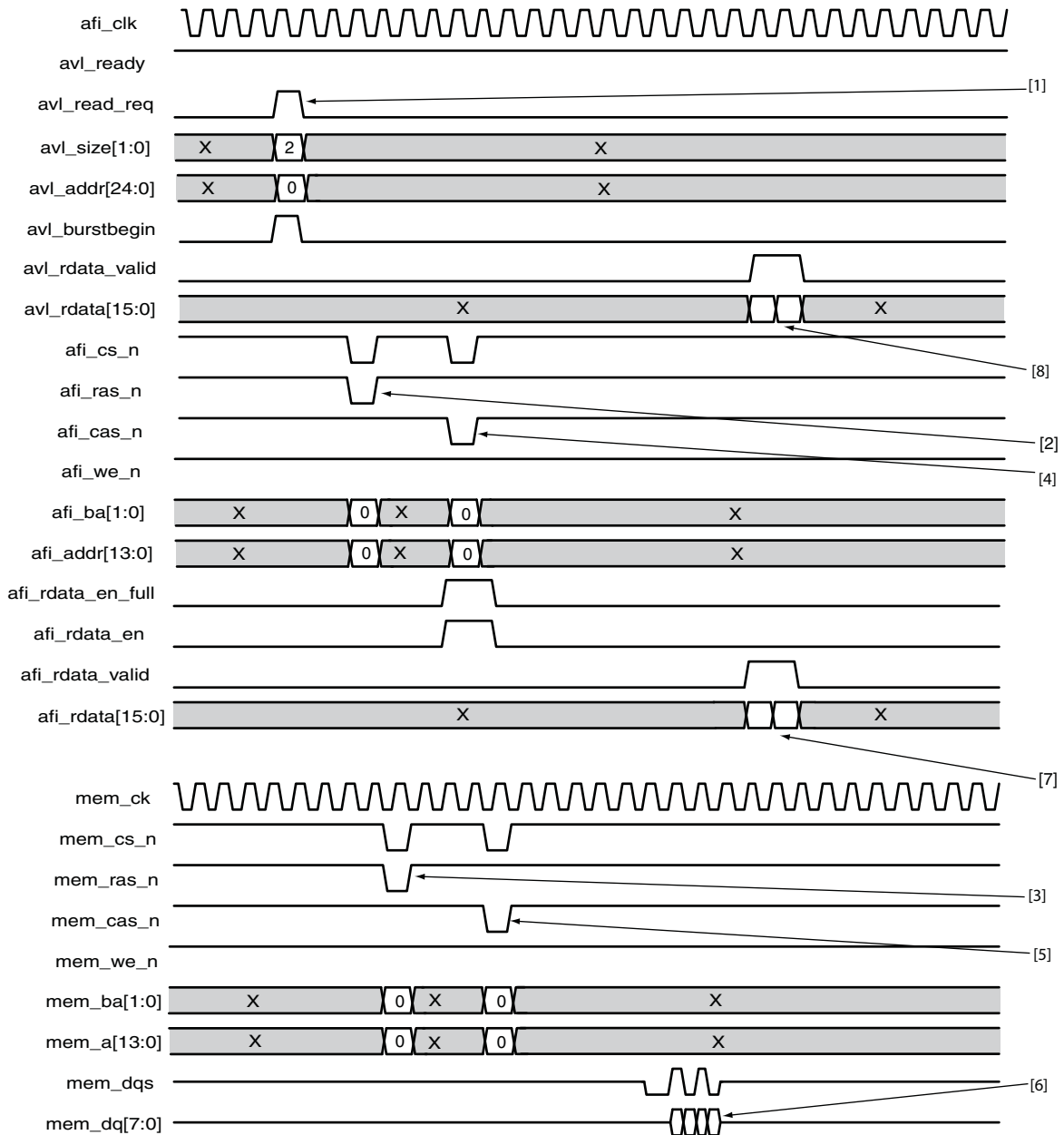
This chapter contains timing diagrams for the UniPHY-based external memory interface IP.

DDR2 and DDR3 Timing Diagrams

This section contains timing diagrams for DDR2 and DDR3 protocols.

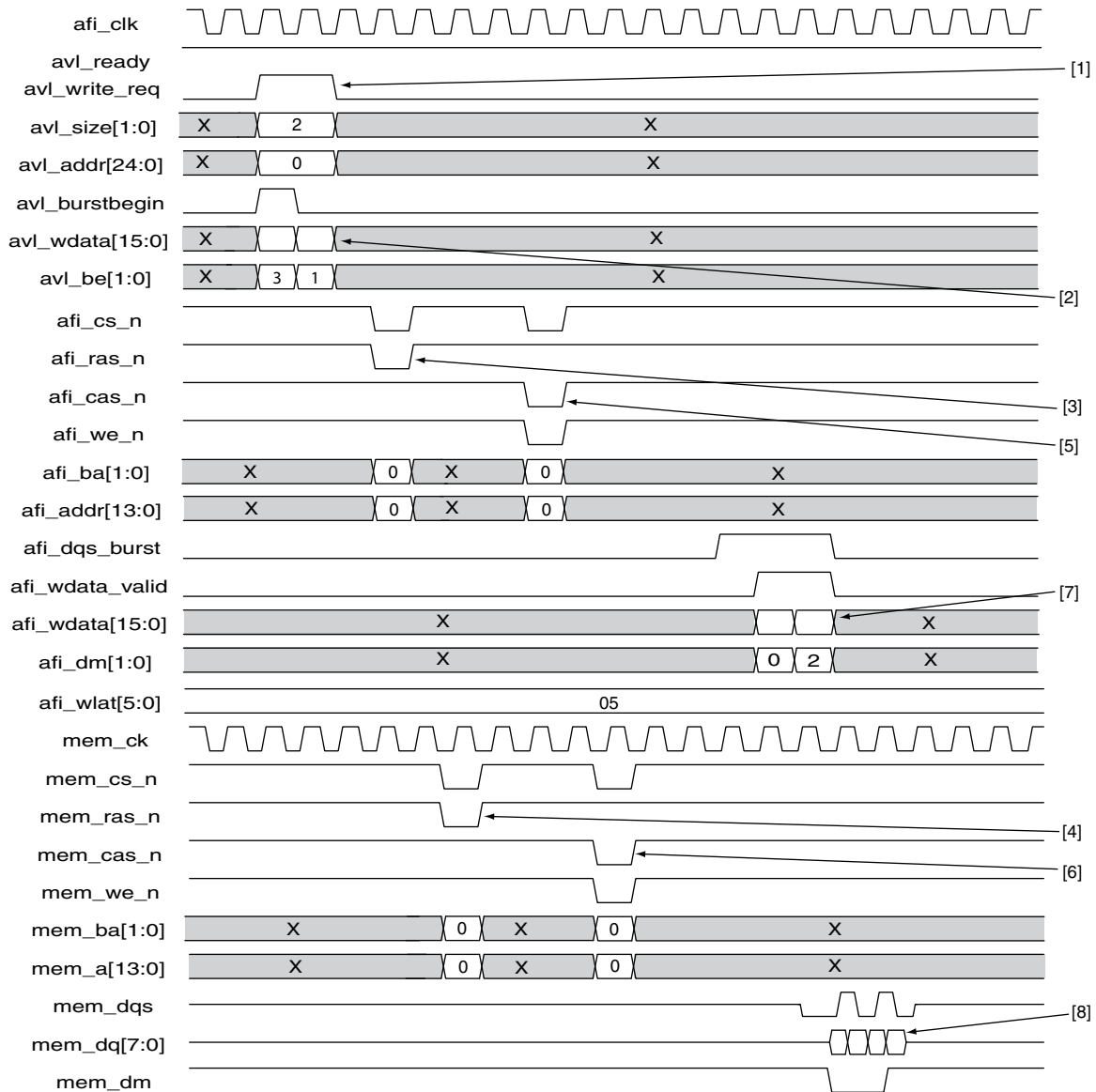
Figure 10–1 through Figure 10–6 present the following timing diagrams, based on a Stratix III device:

- Full-Rate DDR2 SDRAM Read
- Full-Rate DDR2 SDRAM Write
- Half-Rate DDR2 SDRAM Read
- Half-Rate DDR2 SDRAM Write
- Half-Rate DDR3 SDRAM Read
- Half-Rate DDR3 SDRAM Writes
- Quarter-Rate DDR3 SDRAM Reads
- Quarter-Rate DDR3 SDRAM Writes

Figure 10-1. Full-Rate DDR2 SDRAM Read**Notes for Figure 10-1**

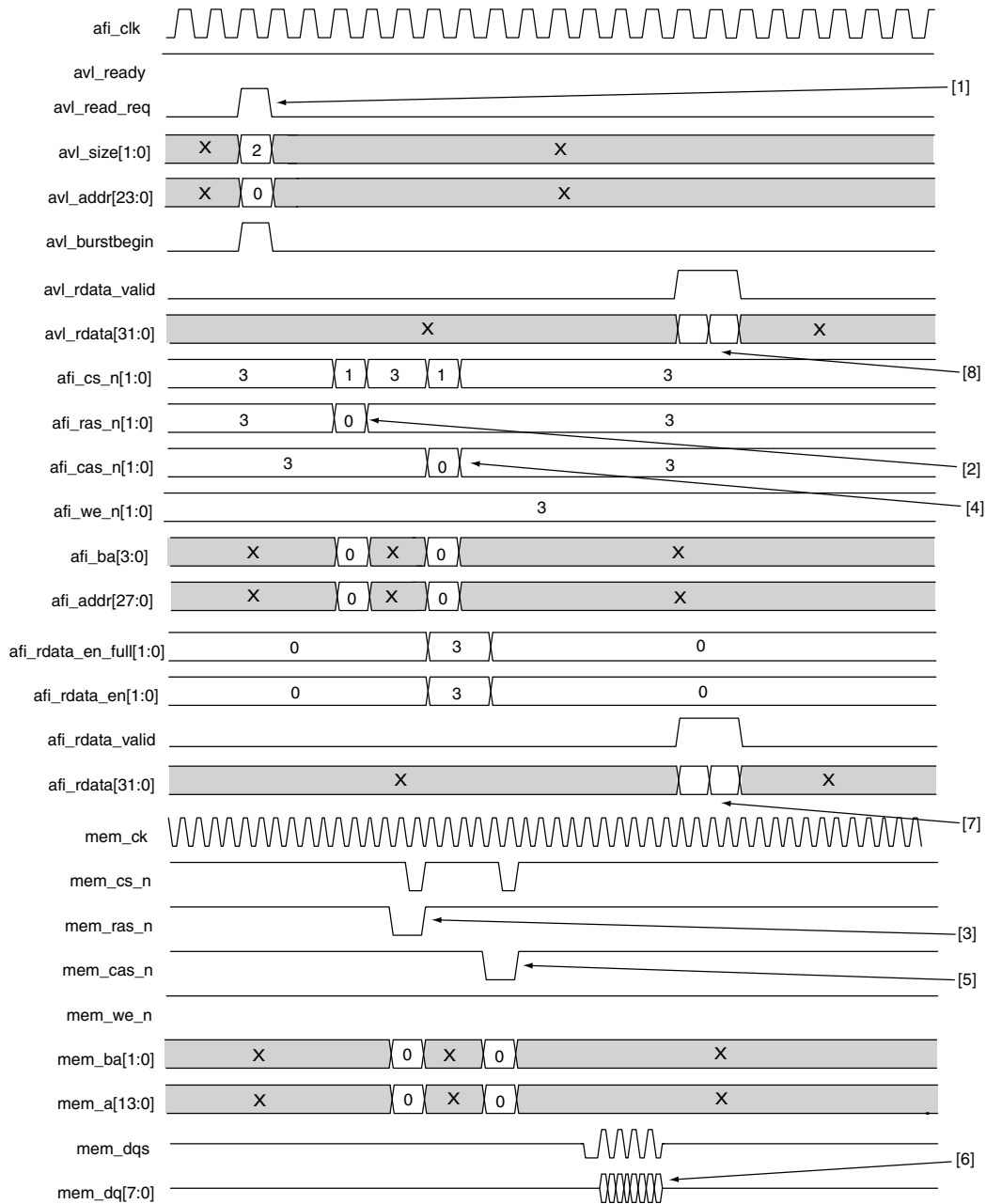
- (1) Controller receives read command.
- (2) Controller issues activate command to PHY.
- (3) PHY issues activate command to memory.
- (4) Controller issues read command to PHY.
- (5) PHY issues read command to memory.
- (6) PHY receives read data from memory.
- (7) Controller receives read data from PHY.
- (8) User logic receives read data from controller.

Figure 10–2. Full-Rate DDR2 SDRAM Write



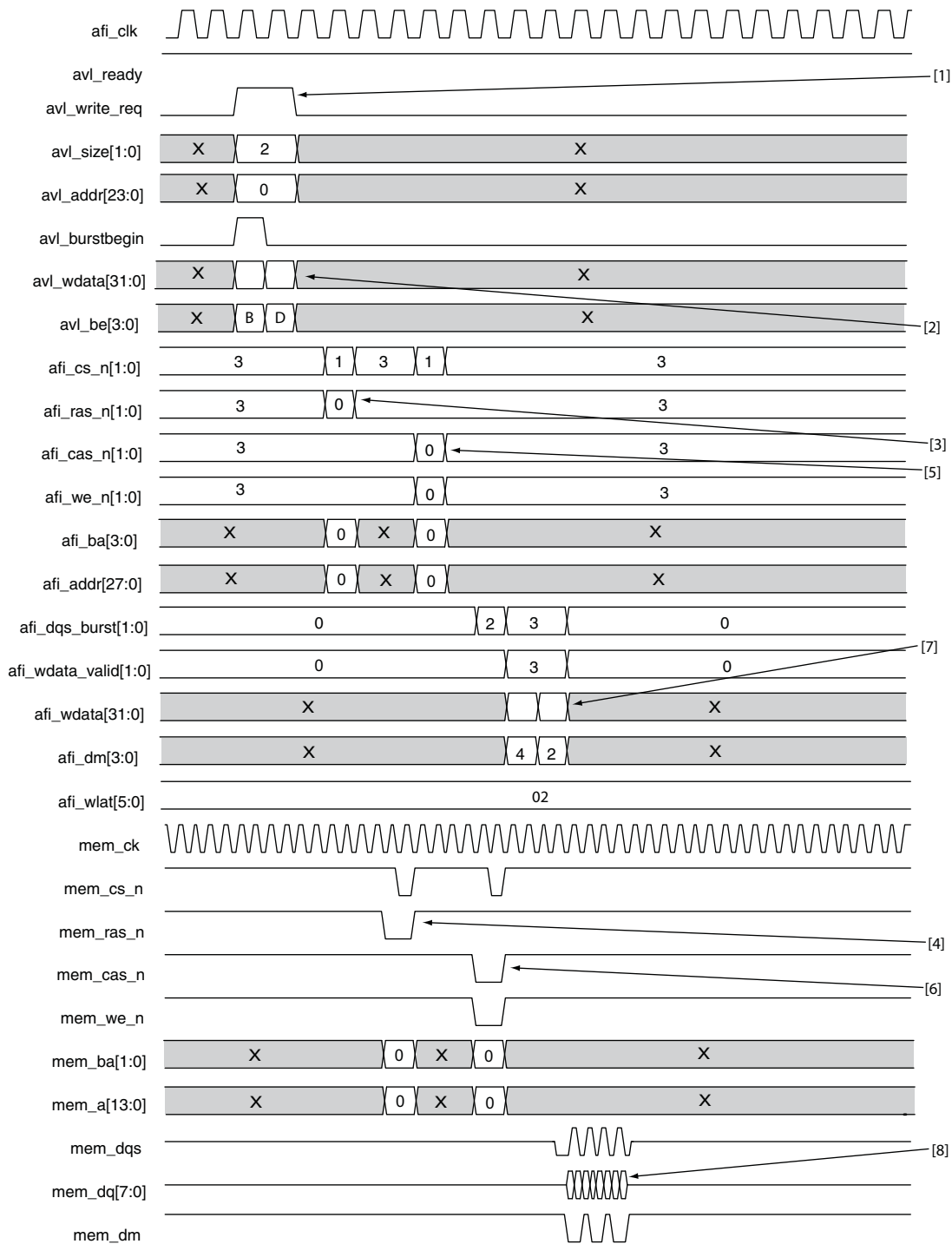
Notes for Figure 10–2:

- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues activate command to PHY.
- (4) PHY issues activate command to memory.
- (5) Controller issues write command to PHY.
- (6) PHY issues write command to memory.
- (7) Controller sends write data to PHY.
- (8) PHY sends write data to memory.

Figure 10-3. Half-Rate DDR2 SDRAM Read**Notes for Figure 10-3:**

- (1) Controller receives read command.
- (2) Controller issues activate command to PHY.
- (3) PHY issues activate command to memory.
- (4) Controller issues read command to PHY.
- (5) PHY issues read command to memory.
- (6) PHY receives read data from memory.
- (7) Controller receives read data from PHY.
- (8) User logic receives read data from controller.

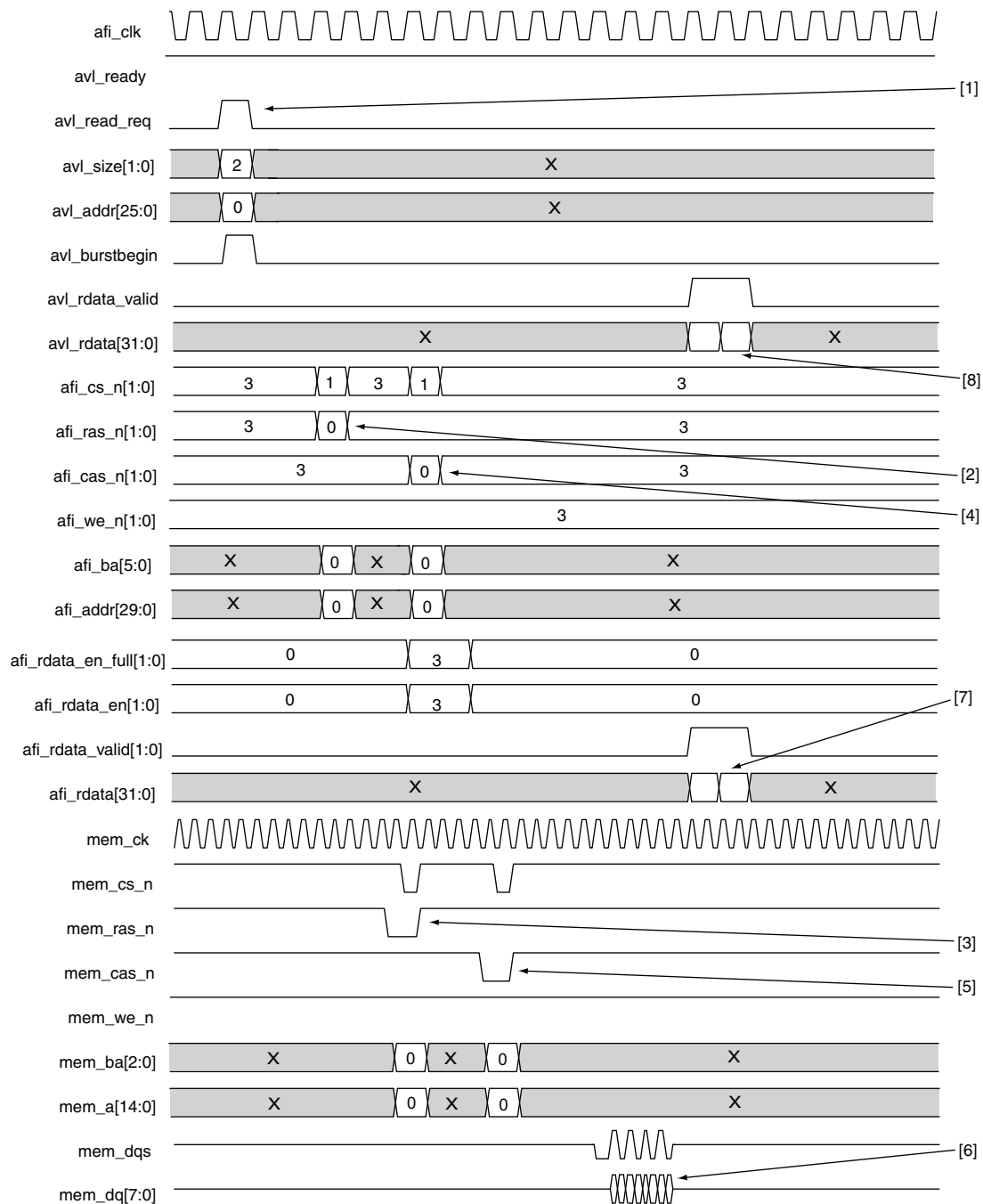
Figure 10–4. Half-Rate DDR2 SDRAM Write



Notes for Figure 10–4:

- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues activate command to PHY.
- (4) PHY issues activate command to memory.

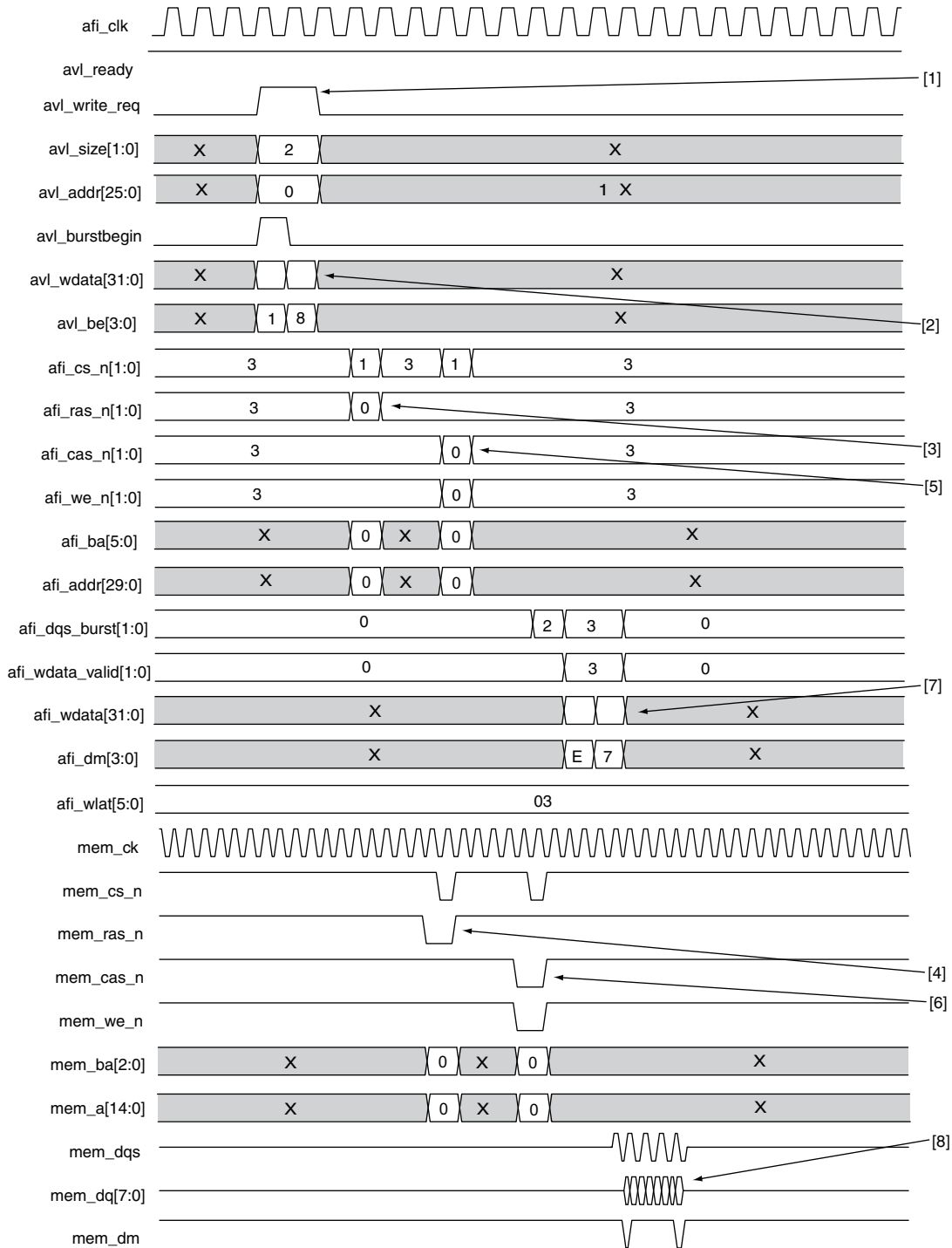
- (5) Controller issues write command to PHY.
- (6) PHY issues write command to memory.
- (7) Controller sends write data to PHY.
- (8) PHY sends write data to memory.

Figure 10-5. Half-Rate DDR3 SDRAM Read**Notes for Figure 10-5:**

- (1) Controller receives read command.
- (2) Controller issues activate command to PHY.
- (3) PHY issues activate command to memory.

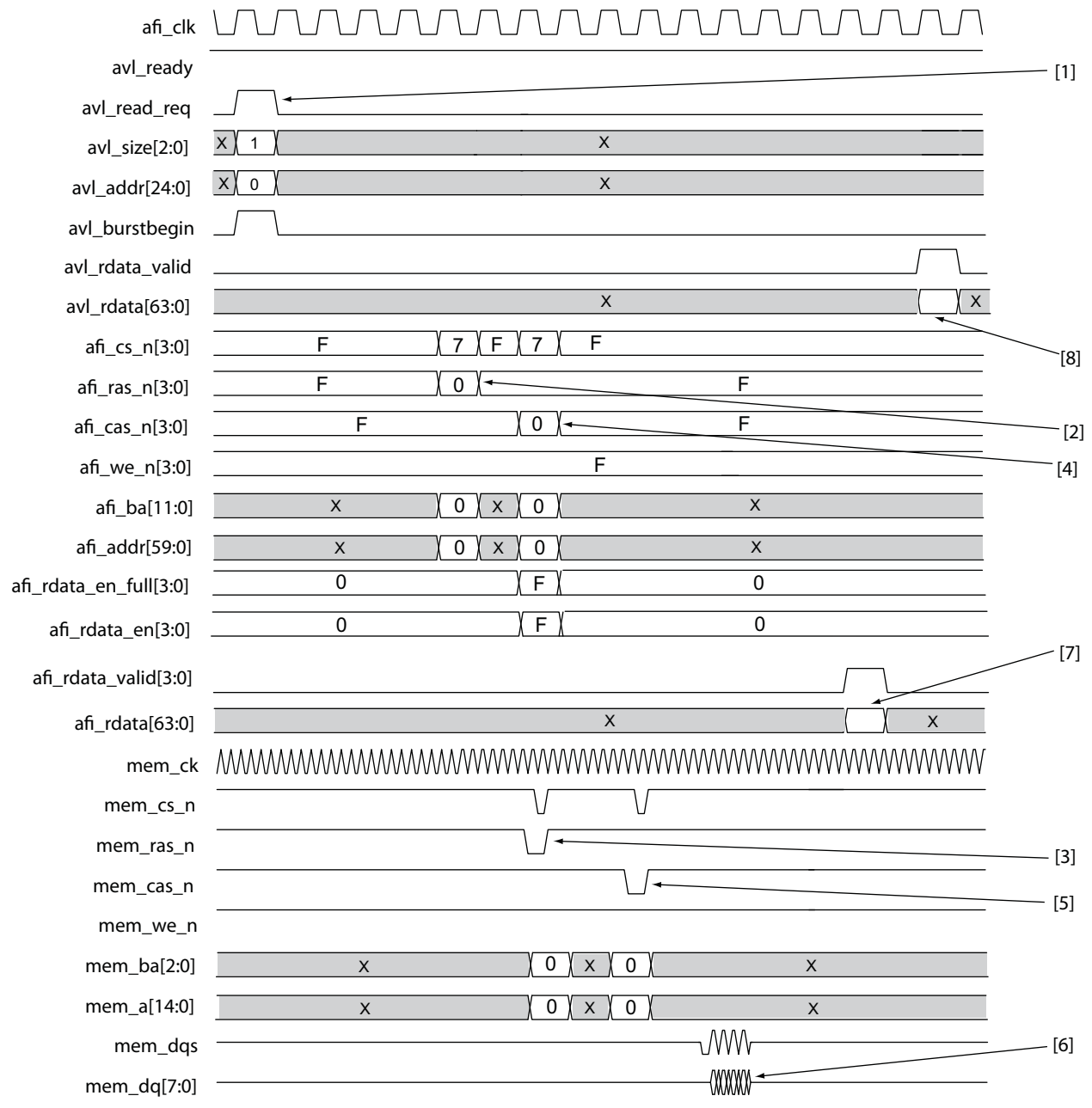
- (4) Controller issues read command to PHY.
- (5) PHY issues read command to memory.
- (6) PHY receives read data from memory.
- (7) Controller receives read data from PHY.
- (8) User logic receives read data from controller.

Figure 10-6. Half-Rate DDR3 SDRAM Writes



Notes for Figure 10-6:

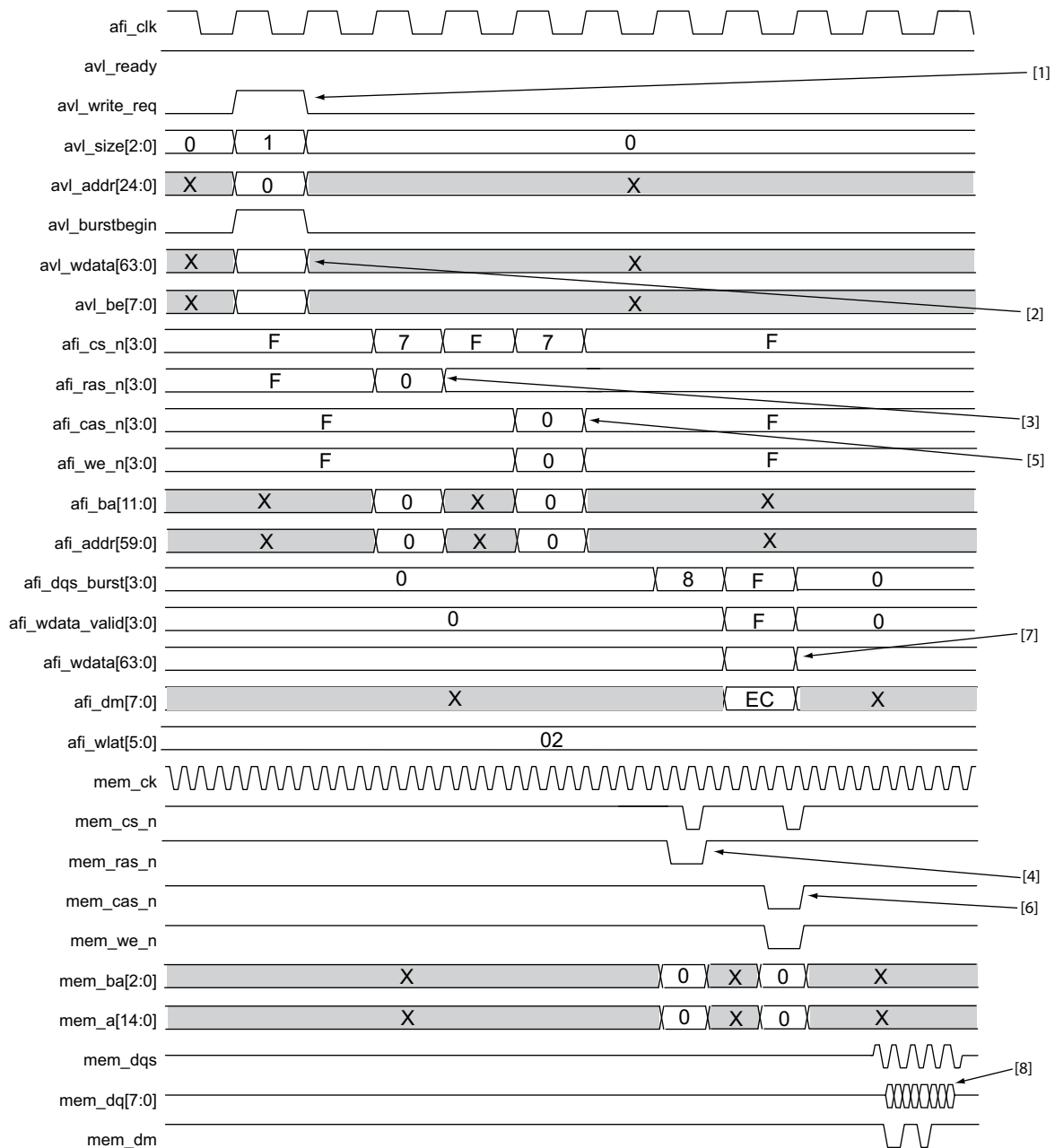
- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues activate command to PHY.
- (4) PHY issues activate command to memory.
- (5) Controller issues write command to PHY.
- (6) PHY issues write command to memory.
- (7) Controller sends write data to PHY.
- (8) PHY sends write data to memory.

Figure 10-7. Quarter-Rate DDR3 SDRAM Reads

Notes for Figure 10-7:

- (1) Controller receives read command.
- (2) Controller issues activate command to PHY.
- (3) PHY issues activate command to memory.
- (4) Controller issues read command to PHY.
- (5) PHY issues read command to memory.
- (6) PHY receives read data from memory
- (7) Controller receives read data from PHY
- (8) User logic receives read data from controller.

Figure 10-8. Quarter-Rate DDR3 SDRAM Writes



Notes for Figure 10-8:

- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues activate command to PHY
- (4) PHY issues activate command to memory.
- (5) Controller issues write command to PHY
- (6) PHY issues write command to memory
- (7) Controller sends write data to PHY
- (8) PHY sends write data to memory.

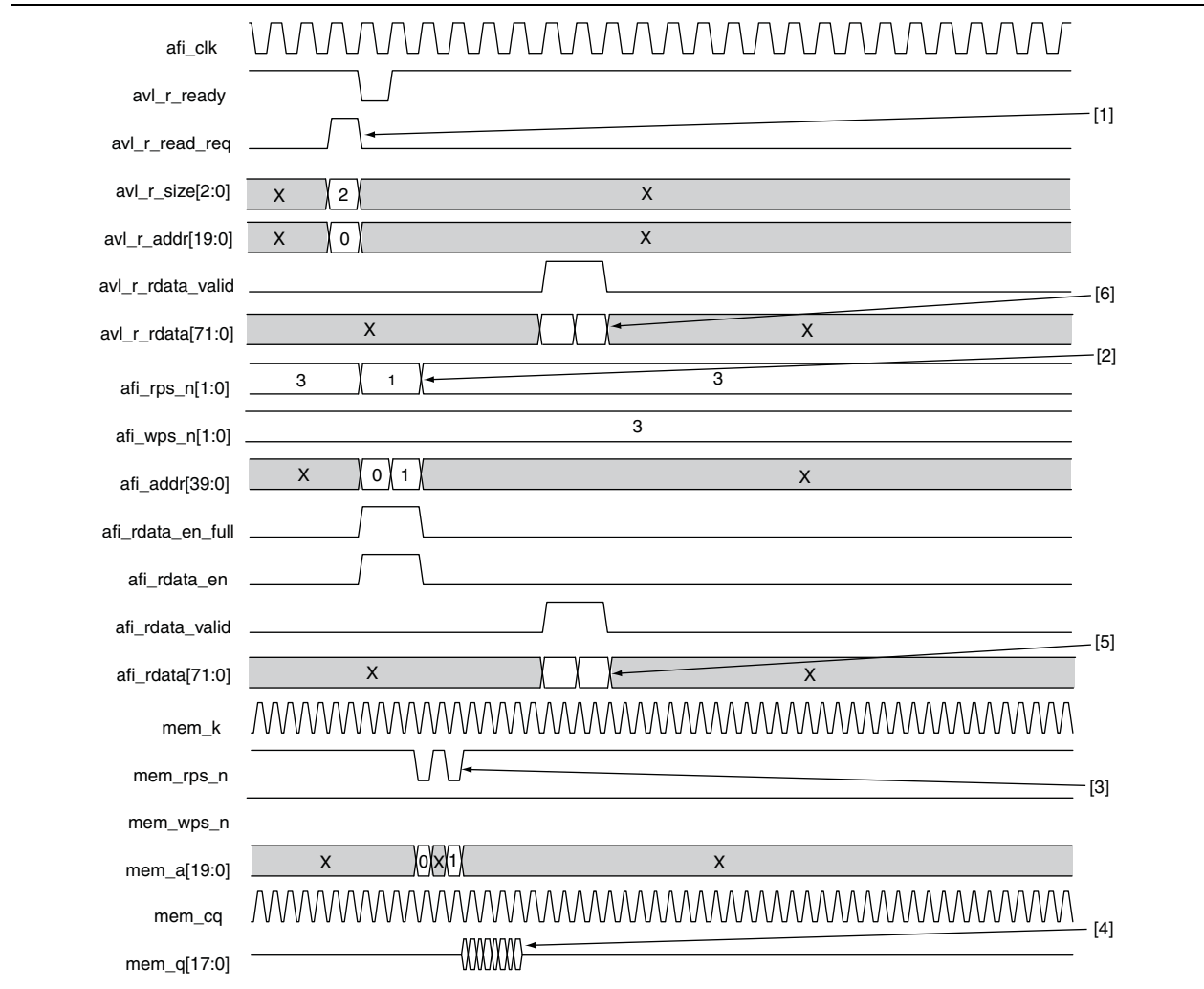
QDR II and QDR II+ Timing Diagrams

This section contains timing diagrams for QDR II and QDR II+ protocols.

Figure 10-9 through Figure 10-12 present the following timing diagrams, based on a Stratix III device:

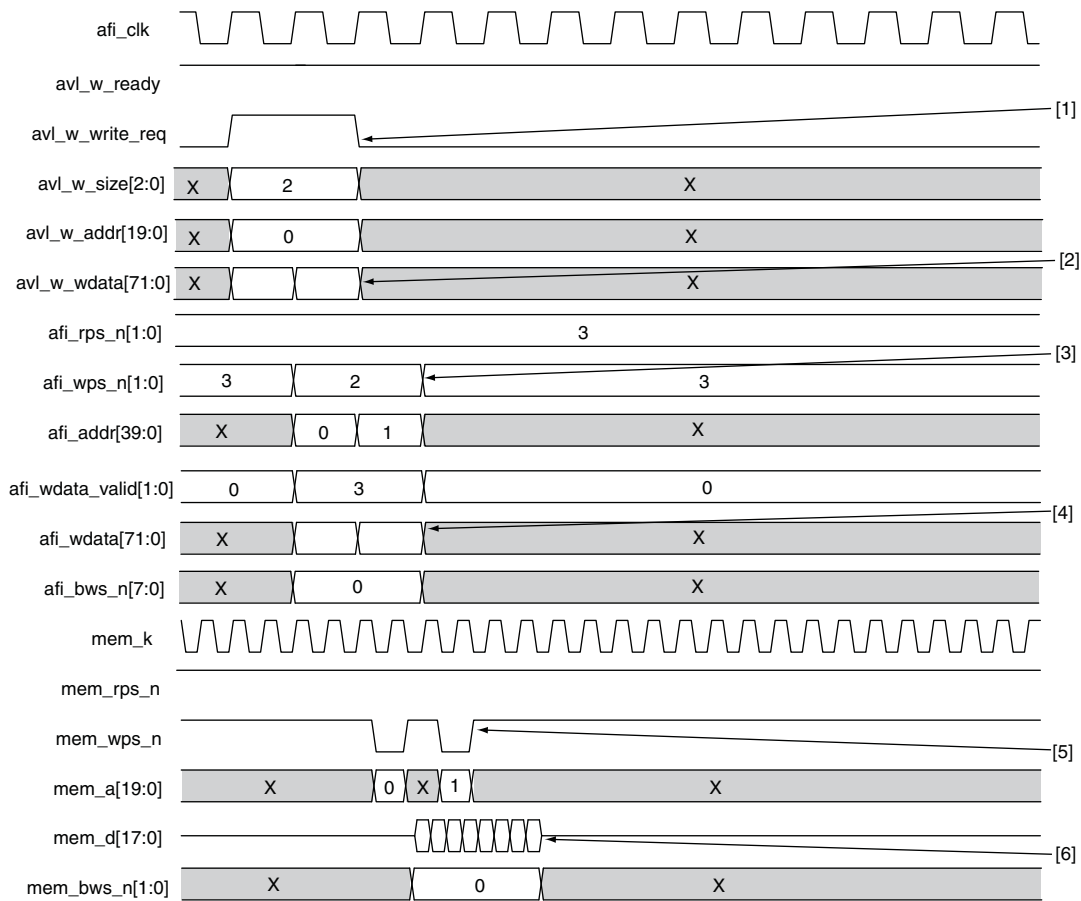
- Half-Rate QDR II and QDR II+ SRAM Read
- Half-Rate QDR II and QDR II+ SRAM Write
- Full-Rate QDR II and QDR II+ SRAM Read
- Full-Rate QDR II and QDR II+ SRAM Write

Figure 10-9. Half-Rate QDR II and QDR II+ SRAM Read



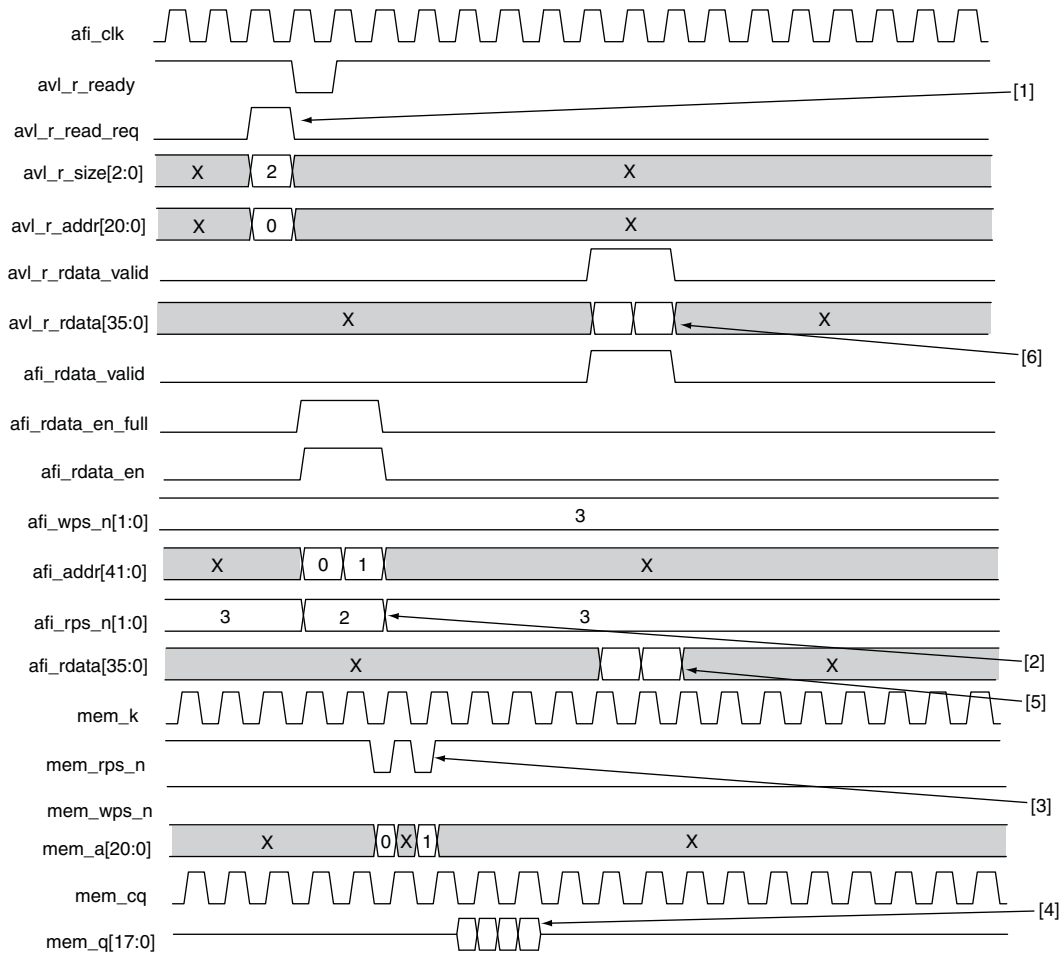
Notes for Figure 10-9:

- (1) Controller receives read command.
- (2) Controller issues two read commands to PHY.
- (3) PHY issues two read commands to memory.
- (4) PHY receives read data from memory.
- (5) Controller receives read data from PHY.
- (6) User logic receives read data from controller.

Figure 10-10. Half-Rate QDR II and QDR II+ SRAM Write**Notes for Figure 10-10:**

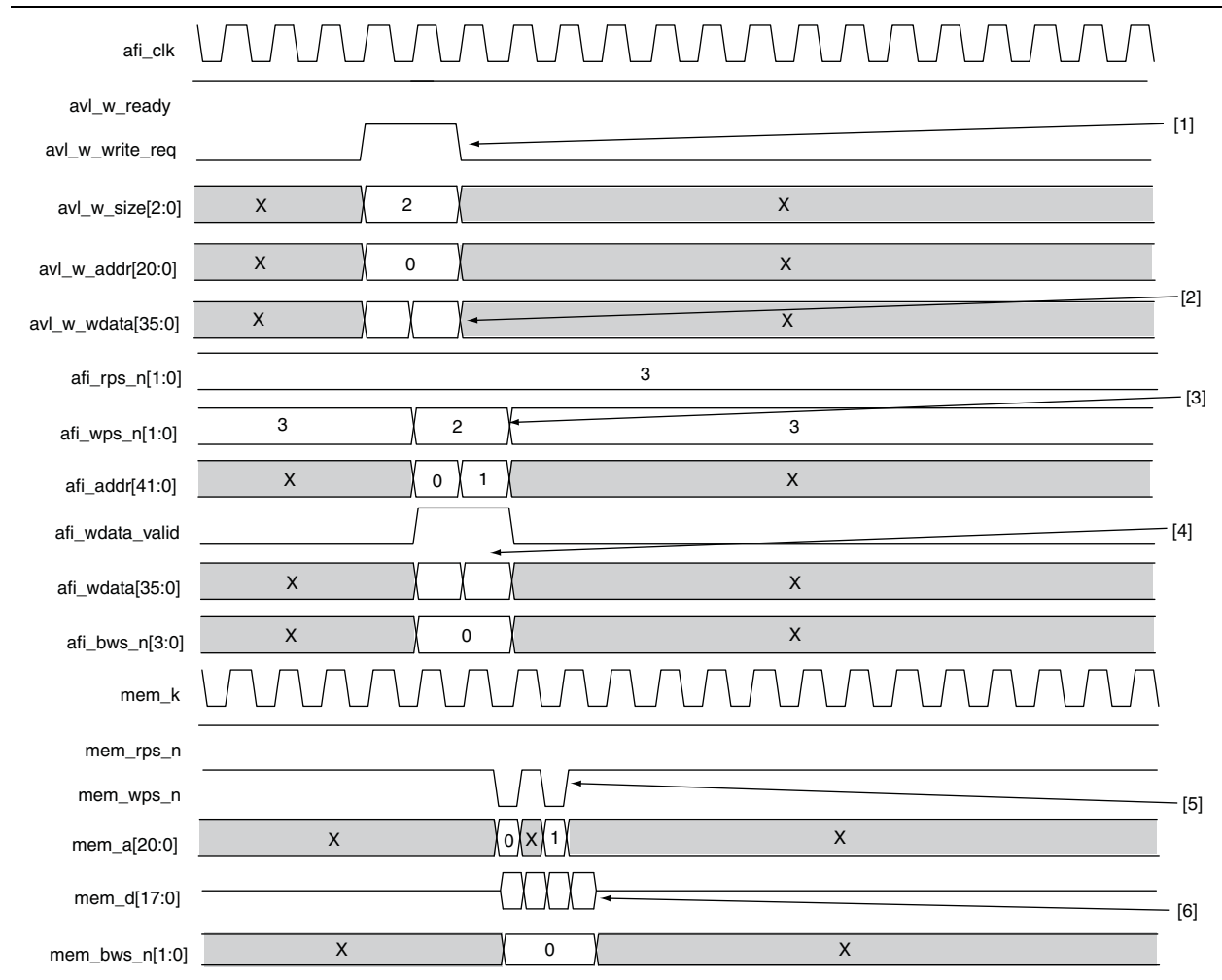
- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues two write commands to PHY.
- (4) Controller sends write data to PHY.
- (5) PHY issues two write commands to memory.
- (6) PHY sends write data to memory.

Figure 10-11. Full-Rate QDR II and QDR II+ SRAM Read



Notes for Figure 10-11:

- (1) Controller receives read command.
- (2) Controller issues two read commands to PHY.
- (3) PHY issues two read commands to memory.
- (4) PHY receives read data from memory.
- (5) Controller receives read data from PHY.
- (6) User logic receives read data from controller.

Figure 10-12. Full-Rate QDR II and QDR II+ SRAM Write**Notes for Figure 10-12:**

- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues two write commands to PHY.
- (4) Controller sends write data to PHY.
- (5) PHY issues two write commands to memory.
- (6) PHY sends write data to memory.

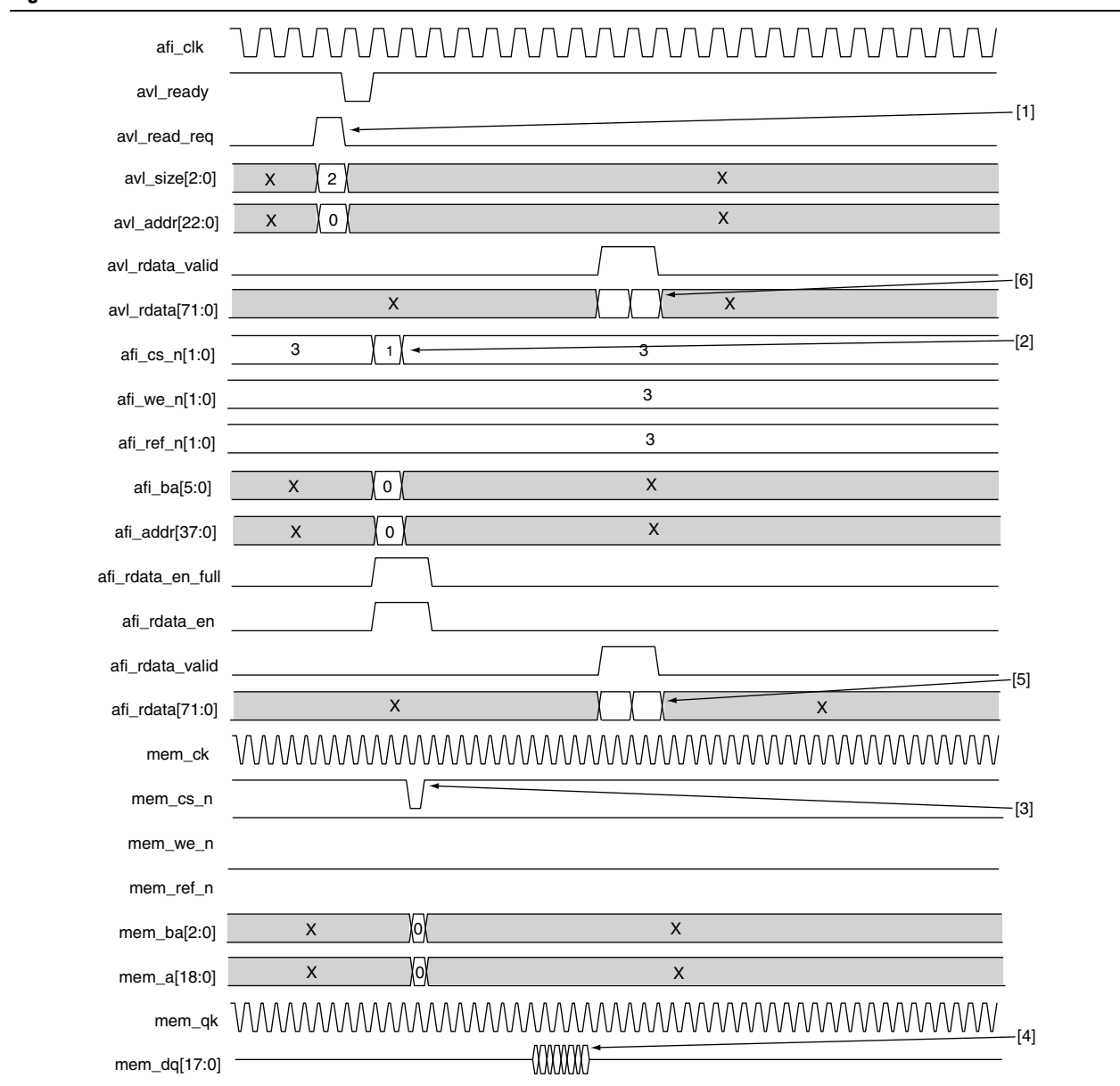
RLDRAM II Timing Diagrams

This section contains timing diagrams for RLDRAM protocols.

Figure 10-13 through Figure 10-16 present the following timing diagrams, based on a Stratix III device:

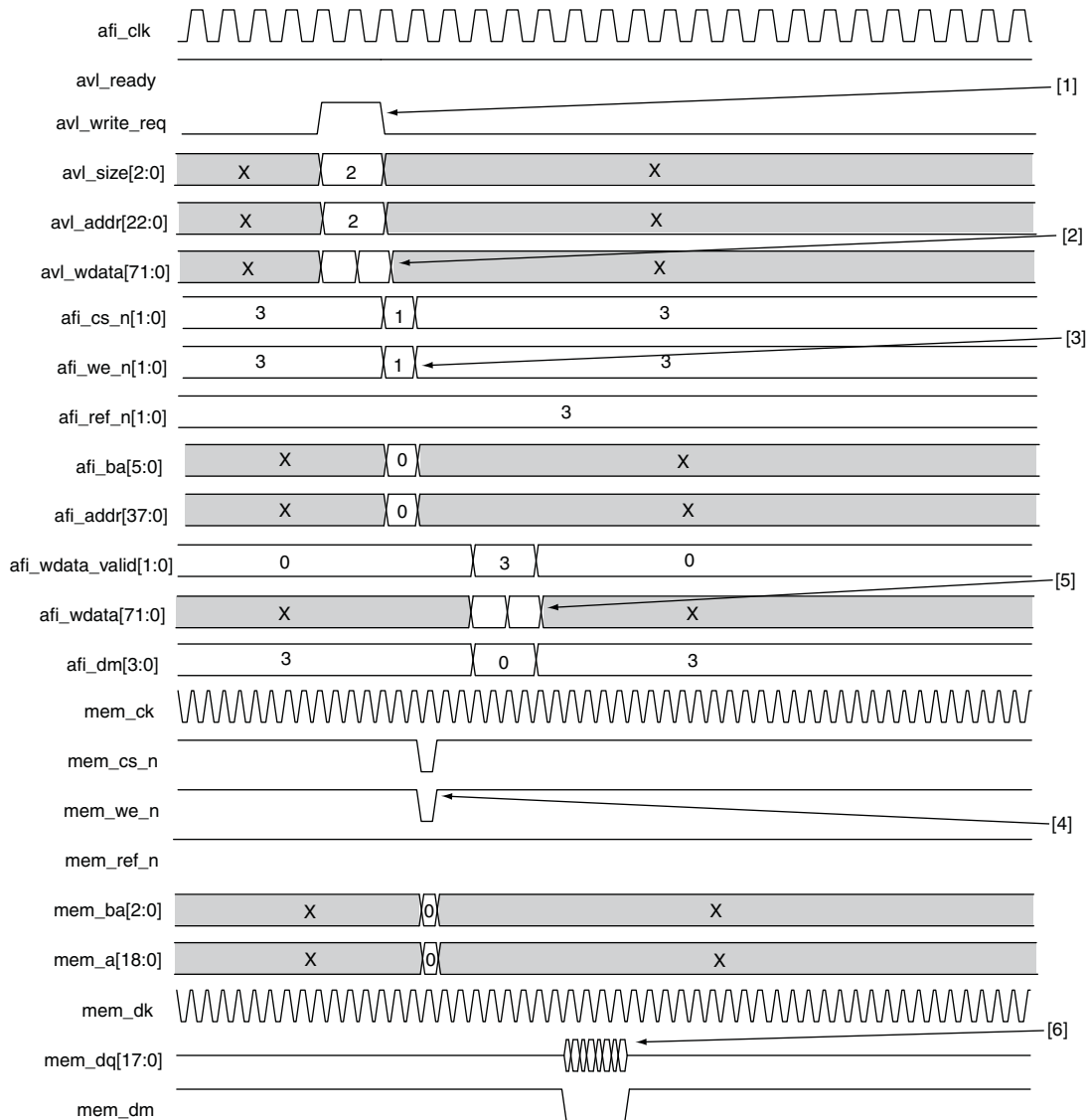
- Half-Rate RLDRAM II Read
- Half-Rate RLDRAM II Write
- Full-Rate RLDRAM II Read
- Full-Rate RLDRAM II Write

Figure 10-13. Half-Rate RLDRAM II Read



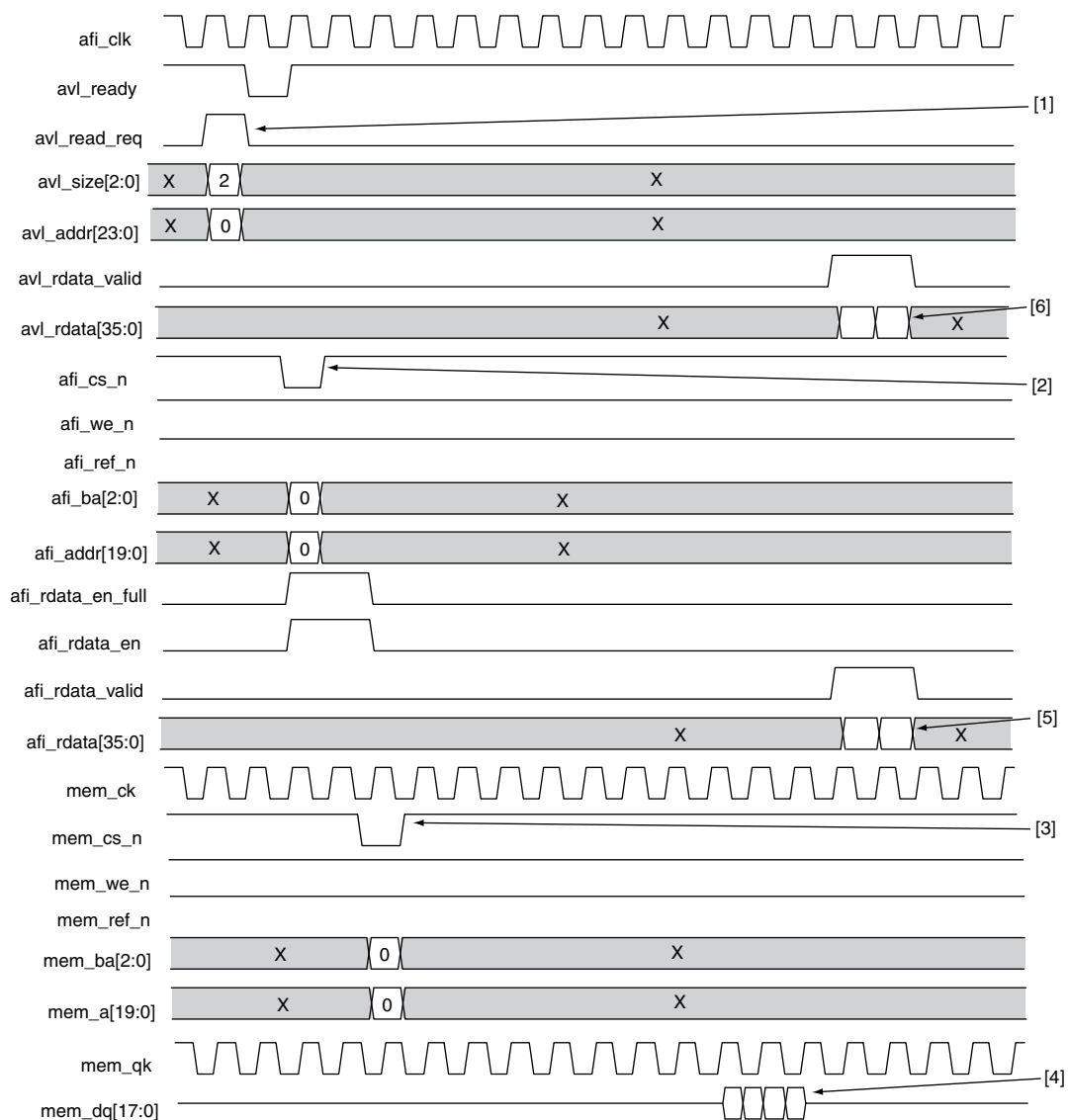
Notes for Figure 10-13:

- (1) Controller receives read command.
- (2) Controller issues read command to PHY.
- (3) PHY issues read command to memory.
- (4) PHY receives read data from memory.
- (5) Controller receives read data from PHY.
- (6) User logic receives read data from controller.

Figure 10-14. Half-Rate RLDRAM II Write**Notes for Figure 10-14:**

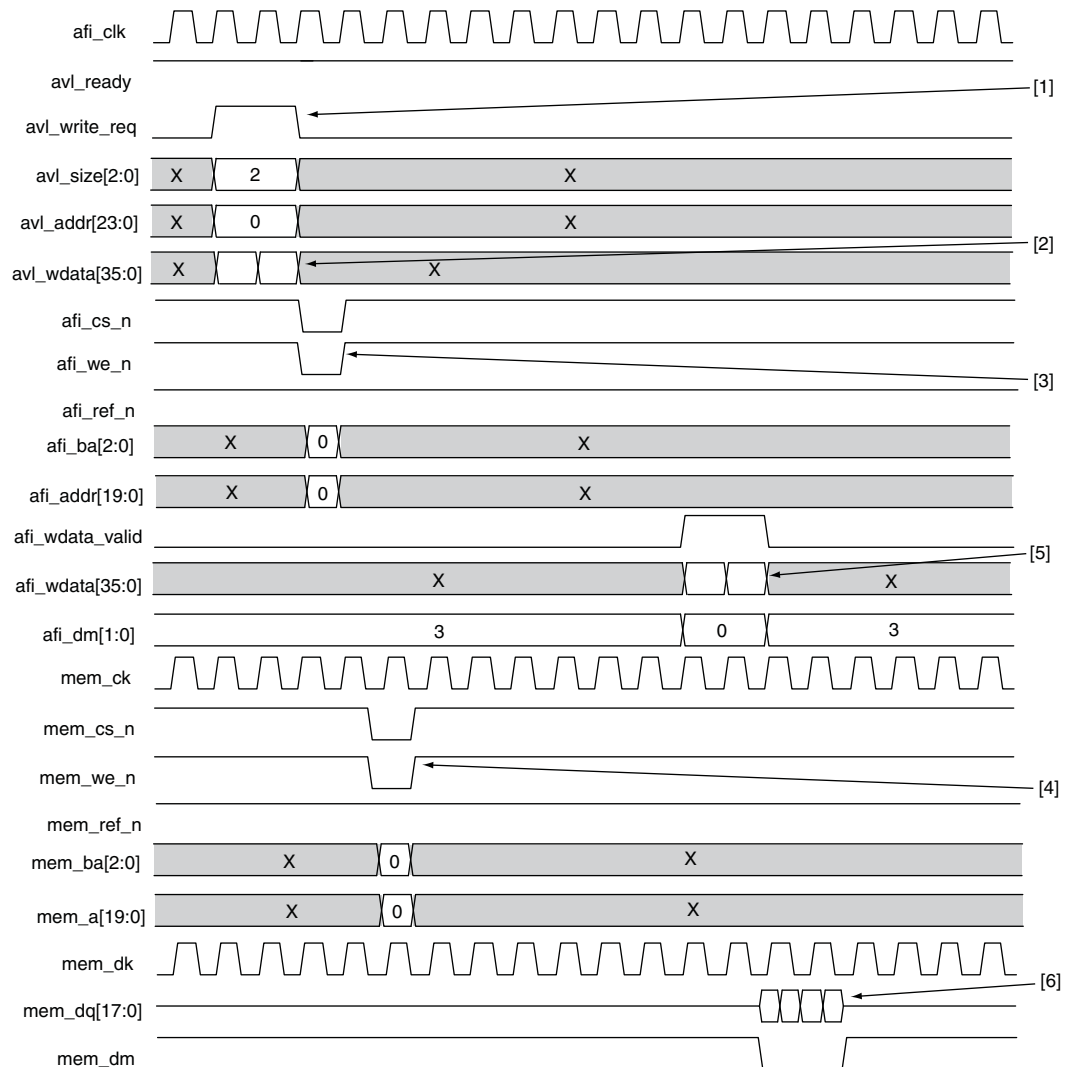
- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues write command to PHY.
- (4) PHY issues write command to memory.
- (5) Controller sends write data to PHY.
- (6) PHY sends write data to memory.

Figure 10-15. Full-Rate RLDRAM II Read



Notes for Figure 10-15:

- (1) Controller receives read command.
- (2) Controller issues read command to PHY.
- (3) PHY issues read command to memory.
- (4) PHY receives read data from memory.
- (5) Controller receives read data from PHY.
- (6) User logic receives read data from controller.

Figure 10-16. Full-Rate RLDRAM II Write**Notes for Figure 10-16:**

- (1) Controller receives write command.
- (2) Controller receives write data.
- (3) Controller issues write command to PHY.
- (4) PHY issues write command to memory.
- (5) Controller sends write data to PHY.
- (6) PHY sends write data to memory.

Document Revision History

Table 10-1 lists the revision history for this document.

Table 10-1. Document Revision History

Date	Version	Changes
November 2011	1.1	<ul style="list-style-type: none"><li data-bbox="506 405 1417 491">■ Consolidated timing diagrams from 11.0 DDR2 and DDR3 SDRAM Controller with UniPHY User Guide, QDR II and QDR II+ SRAM Controller with UniPHY User Guide, and RLDRAM II Controller with UniPHY IP User Guide.<li data-bbox="506 506 1084 531">■ Added Read and Write diagrams for DDR3 quarter-rate.

