

Introduction

Stratix[®] III devices have dedicated high-performance digital signal processing (DSP) blocks that are distributed throughout the core fabric. These hard-wired DSP blocks are ideal for applications such as high performance computing (HPC), video compression/decompression, and voice over internet protocol (VoIP). Such applications typically require a large number of mathematical computations. Stratix III DSP blocks consist of a combination of dedicated elements that perform multiplication, addition, subtraction, accumulation, summation, and dynamic shift operations. In HardCopy[®] III devices, these DSP functions are constructed using HCells instead of dedicated DSP blocks. HCells allow HardCopy III devices to have the same functionality as Stratix III DSP blocks. In addition, DSP blocks implemented with HCells provide significant static power savings because only the HCells needed to implement the functions are used.

DSP Function Implementation

Stratix III devices have dedicated DSP blocks to implement various DSP functions. A Stratix III DSP block consists of an input register bank, multiplier adders, pipeline register bank, second stage adders/accumulator, round and saturation units, and second adder register and output register bank. In the HardCopy III devices, HCells make up part of the device core fabric. HCells are a collection of logic transistors that are connected together to provide the same DSP functions as the Stratix III DSP blocks. HCells are also used to implement the Stratix III adaptive logic module (ALM) and logic array block (LAB) functions in the HardCopy III devices.



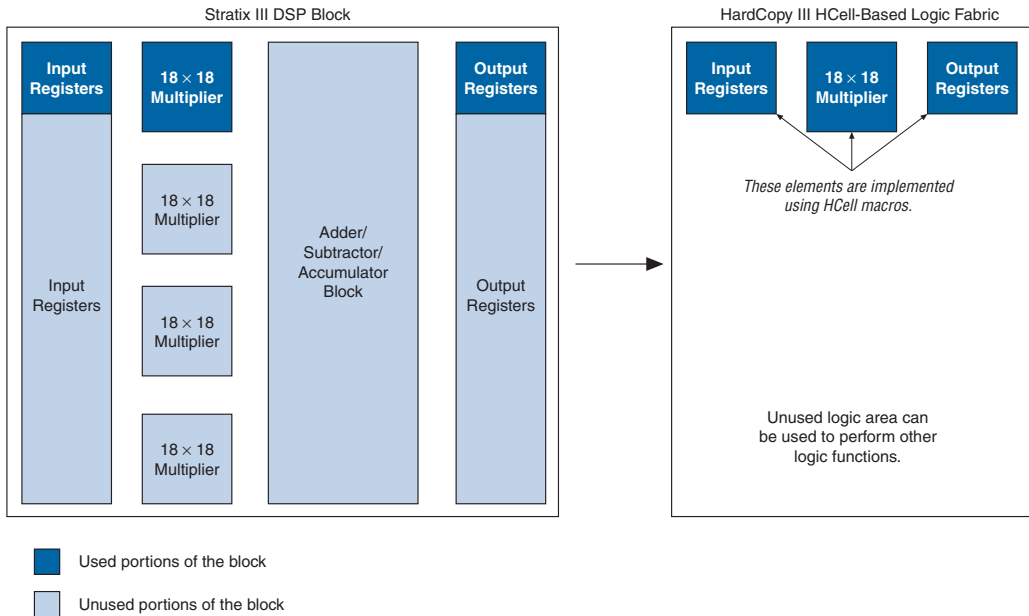
For more information about ALM, LAB, and memory logic array block (MLAB) implementation in HardCopy III devices, refer to the [Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices](#) chapter in volume 1 of the *HardCopy III Device Handbook*.

The Quartus[®] II software uses a library of pre-characterized HCell macros to place Stratix III DSP configurations into the HardCopy III HCell-based logic fabric. An HCell macro (HCM) defines how a group of HCells are connected together. Based on design requirements, the Quartus II software chooses the appropriate DSP HCell macros to implement the DSP functionality. In HardCopy III devices, HCell macros implement Stratix III DSP block functionality with area efficiency and performance on par with the dedicated DSP blocks in Stratix III devices.

Only HCells that are required to implement the design's DSP functions are enabled. HCells not needed for DSP functions can be used for ALM configurations, which results in efficient logic usage. In addition to area management, the placement of these HCell macros allows for optimized routing and performance.

An example of efficient logic area usage can be seen when comparing the 18×18 independent multiplier implementation in Stratix III devices using the dedicated DSP block versus the implementation in HardCopy III devices using HCells. If the Stratix III DSP function only calls for one 18×18 multiplier, the other three 18×18 multipliers and the DSP block's adder output block are not used, as shown in Figure 3-1. In HardCopy III devices, the HCell-based logic fabric that is not used for DSP functions can be used to implement other combinational logic, adder, register, and MLAB functions.

Figure 3-1. Stratix III DSP Block versus HardCopy III HCell 18×18 -bit Independent Multiplier Implementation



DSP Operational Mode and Feature Support

HardCopy III devices support all Stratix III DSP configurations (9×9 , 12×12 , 18×18 , and 36×36 multipliers) and all Stratix III DSP block features, such as dynamic sign controls, dynamic addition/subtraction, dynamic rounding and saturation, and dynamic input shift registers.

HardCopy III devices use DSP HCell macros to implement all five operational modes of the Stratix III DSP block:

- Independent Multiplier (9×9 , 12×12 , 18×18 , 36×36)
- Two-Multiplier Adder
- Four-Multiplier Adder
- Multiply Accumulate
- Shift Mode



For more information about Stratix III DSP blocks, refer to the *DSP Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Depending on the Stratix III DSP configurations, the Quartus II software partitions the DSP function into a combination of DSP HCell macros for the HardCopy III devices. This optimizes the DSP function and allows the core fabric to be more efficiently used.

Conclusion

HardCopy III devices use HCells to implement the DSP block functions of Stratix III devices. All the Stratix III DSP operational modes are supported. Implementing DSP functions using HCells allows the HardCopy III device core fabric to be efficiently used and offers significant static power savings compared with Stratix III prototype devices.

Referenced Documents

This chapter references the following documents:

- *DSP Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*
- *Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*

Document Revision History

Table 3–1 shows the revision history for this document.

<i>Table 3–1. Document Revision History</i>		
Date and Document Version	Changes Made	Summary of Changes
May 2008, v1.0	Initial release.	—