

## Introduction

HardCopy<sup>®</sup> III devices offer TriMatrix embedded memory blocks to efficiently address the needs of ASIC designs. The TriMatrix memory comes in three different sizes and includes 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks. The MLABs have been optimized to implement filter delay lines, small first-in first-out (FIFO) buffers, and shift registers. You can use the M9K blocks for general purpose memory applications, while the M144K blocks are ideal for processor code storage, packet buffering, and video frame buffering.

The TriMatrix memory in HardCopy III devices supports the same memory functions and features as Stratix<sup>®</sup> III devices. You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register via the MegaWizard<sup>®</sup> Plug-in Manager in the Quartus<sup>®</sup> II software. You can stitch together multiple blocks of the same type to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of dedicated embedded static random access memory (SRAM). This chapter describes TriMatrix memory blocks, modes, features, and design considerations in the HardCopy III devices.

## Memory Resources and Features

HardCopy III embedded memory consists of MLAB, M9K, and M144K memory blocks and has a one-to-one mapping from the Stratix III memory. However, the number of available memory blocks differs based on density, package, and Stratix III device to HardCopy III ASIC migration paths as shown in [Table 4-1](#).

**Table 4-1. HardCopy III Embedded Memory Resources (Part 1 of 2)**  
*Note (1), (2)*

HardCopy III Device	Stratix III Device	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs)
HC311	EP3SL110	275	12	4203 Kb
HC321	EP3SL150	355	16	5499 Kb
HC322	EP3SL150	355	16	5499 Kb
HC331	EP3SE110	639	16	8055 Kb
HC332	EP3SE110	639	16	8055 Kb

**Table 4–1. HardCopy III Embedded Memory Resources (Part 2 of 2)**  
*Note (1), (2)*

HardCopy III Device	Stratix III Device	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs)
HC351	EP3SL200	468	24	7668 Kb
HC352	EP3SL200	468	36	9396 Kb
HC361	EP3SE260	864	24	11,232 Kb
HC362	EP3SE260	864	48	14,688 Kb
HC372	EP3SL340	1040	48	16,272 Kb

**Notes to Table 4–1:**

- (1) In addition to device resource usage, Stratix III packages also determine the optimal HardCopy III device migration path. For example, the EP3SL150 device comes in F780 and F1152 packages. The migration paths for the F780 and F1152 packages are the HC321 and HC322 devices, respectively.
- (2) HardCopy III devices do not have dedicated MLAB blocks but can support the same Stratix III MLAB functionality. The number of MLABs that can be supported in HardCopy III devices varies depending on resource usage and Stratix III device to HardCopy III device migration path.

Functionally, memory in HardCopy III devices and Stratix III devices is identical. The memory blocks can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO. Table 4–2 shows the size and features of the different memory blocks. In addition, unused memory blocks in HardCopy III devices are powered down, allowing the HardCopy III devices to have significant power savings.

**Table 4–2. HardCopy III Embedded Memory Features (Part 1 of 2)**

Feature	MLABs	M9K Blocks	M144K Blocks
Maximum performance	TBD	TBD	TBD
Total RAM bits (including parity bits)	640	9,216	147,456
Configurations (depth × width)	64 × 8 64 × 9 64 × 10 32 × 16 32 × 18 32 × 20	8K × 1 4K × 2 2K × 4 1K × 8 1K × 9 512 × 16 512 × 18 256 × 32 256 × 36	16K × 8 16K × 9 8K × 16 8K × 18 4K × 32 4K × 36 2K × 64 2K × 72

**Table 4–2. HardCopy III Embedded Memory Features (Part 2 of 2)**

Feature	MLABs	M9K Blocks	M144K Blocks
Parity bits	✓	✓	✓
Byte enable	✓	✓	✓
Packed mode	—	✓	✓
Address clock enable	✓	✓	✓
Single-port memory	✓	✓	✓
Simple dual-port memory	✓	✓	✓
True dual-port memory	—	✓	✓
Embedded shift register	✓	✓	✓
ROM	✓	✓	✓
FIFO buffer	✓	✓	✓
Simple dual-port mixed width support	—	✓	✓
True dual-port mixed width support	—	✓	✓
Memory initialization file (.mif)	Not supported, except in ROM mode	Not supported, except in ROM mode	Not supported, except in ROM mode
Mixed-clock mode	✓	✓	✓
Power-up condition	Outputs cleared if registered, otherwise reads memory contents. (1)	Outputs cleared	Outputs cleared
Register clears	Outputs cleared	Outputs cleared	Outputs cleared
Write/Read operation triggering	Write: Falling clock edges Read: Rising clock edges	Write and Read: Rising clock edges	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to old data or don't care	Outputs set to old or new data	Outputs set to old or new data
Mixed-port read-during-write	Outputs set to don't care	Outputs set to old data	Outputs set to old data
ECC Support	Soft IP support via Quartus II	Soft IP support via Quartus II	Built-in support in x64 wide SDP mode or soft IP support via Quartus II

Note to [Table 4–2](#):

(1) The memory contents for the MLAB in RAM mode are initialized to zero on power-up.



For more information about embedded memory support in Stratix III devices, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

## MLAB Implementation

While the M9K and M144K memory blocks are dedicated resources that function the same in Stratix III and HardCopy III devices, the MLABs are implemented differently in the two device families. In Stratix III devices, the MLABs are dedicated blocks and can be configured for regular logic functions or memory functions. In HardCopy III devices, the MLAB memory blocks are implemented using HCells. HCells are a collection of logic transistors connected together to form HCell macros (HCMs). The Quartus II software maps the Stratix III MLAB function to the appropriate memory HCell macro that preserves the memory function. This allows the HardCopy III core fabric to be more efficiently used, freeing up unused HCells for adaptive logic module (ALM) or DSP functions.



Refer to the *Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook* for more information about HCells in HardCopy III devices.

## Design Considerations

Unlike Stratix III devices, HardCopy III devices do not have device configuration, so memories that are configured as RAM power-up with random content. Thus, the memory block contents cannot be pre-loaded or initialized with a memory initialization file (.mif) in HardCopy III devices. You must make sure that your Stratix III design does not require .mif files if the memory blocks are used as RAM. However, if the memory blocks are used as ROM, they will be mask programmed to the design's ROM contents.



You may use the `altmem_init` megafunction to initialize the RAM after power-up for HardCopy III devices. This megafunction reads from an internal ROM (inside the megafunction) or an external ROM (on-chip or off-chip), and writes to the RAM after power-up.

When using the non-registered output mode for the HardCopy III MLAB memory blocks, the outputs power-up with memory content. When using the registered output mode for these memory blocks, the outputs are cleared on power-up. You must take this into consideration when designing logic that might evaluate the initial power-up values of the MLAB memory block.

## Conclusion

HardCopy III devices offer three TriMatrix embedded memory blocks of different sizes that efficiently meet all your design needs. The embedded memories in HardCopy III devices and Stratix III devices are functionally equivalent. Unlike Stratix III devices, memory blocks used as RAM in

HardCopy III devices cannot be pre-loaded with a .mif pattern. ROM patterns, however, can be implemented for all memory types since they will be mask programmed into the memory.

## Referenced Documents

This chapter references the following documents:

- *Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*
- *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*

## Document Revision History

Table 4–3 shows the revision history for this document.

<i>Table 4–3. Document Revision History</i>		
<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2008, v1.0	Initial release.	—

