

This chapter describes TriMatrix memory blocks, modes, features, and design considerations in HardCopy® IV devices.

HardCopy IV devices offer TriMatrix embedded memory blocks to efficiently address the needs of ASIC designs. TriMatrix memory comes in three different sizes and includes 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks. The MLABs have been optimized to implement filter delay lines, small FIFO buffers, and shift registers. You can use the M9K blocks for general purpose memory applications; you can use the M144K blocks for processor code storage, packet buffering, and video frame buffering.

TriMatrix memory in HardCopy IV devices support the same memory functions and features as Stratix® IV devices. You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register using the MegaWizard™ Plug-in Manager in the Quartus® II software. You can stitch together multiple blocks of the same type to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 20,736 Kbits of dedicated embedded static random access memory (SRAM).

This chapter contains the following sections:

- “Memory Resources and Features”
- “Design Considerations” on page 4-4

Memory Resources and Features

HardCopy IV embedded memory consists of MLAB, M9K, and M144K memory blocks and has a one-to-one mapping from Stratix IV memory. However, the number of available memory blocks differs based on density, package, and the Stratix IV device-to-HardCopy IV ASIC mapping paths, as shown in Table 4-1.

Table 4-1. Embedded Memory Resources for HardCopy IV Devices (Part 1 of 2) (Note 1), (2)

HardCopy IV ASIC	Stratix IV FPGA Prototype	M9K Blocks	M144K Blocks (3)	Total Dedicated RAM Bits (not including MLABs)
HC4GX15	EP4SGX70	462	16	6,462 Kb
	EP4SGX110	660	16	8,244 Kb
	EP4SGX180	660	20	8,820 Kb
	EP4SGX230	660	22	9,108 Kb
	EP4SGX290	660	24	9,396 Kb
	EP4SGX360	660	24	9,396 Kb

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Table 4-1. Embedded Memory Resources for HardCopy IV Devices (Part 2 of 2) (Note 1), (2)

HardCopy IV ASIC	Stratix IV FPGA Prototype	M9K Blocks	M144K Blocks (3)	Total Dedicated RAM Bits (not including MLABs)
HC4GX25	EP4SGX110	660	16	8,244 Kb
	EP4SGX180	936	20	11,304 Kb
	EP4SGX230	936	22	11,592 Kb
	EP4SGX290	936	36	13,608 Kb
	EP4SGX360	936	36	13,608 Kb
	EP4SGX530	936	36	13,608 Kb
HC4GX35	EP4SGX180	950	20	11,430 Kb
	EP4SGX230	1,235	22	14,283 Kb
	EP4SGX290	936	36	13,608 Kb
	EP4SGX360	1,248	48	18,144 Kb
	EP4SGX530	1,280	64	20,736 Kb
HC4E25	EP4SE230	864	22	10,944 Kb
	EP4SE360	864	32	12,384 Kb
HC4E35	EP4SE360	1,248	48	18,144 Kb
	EP4SE530	1,280	48	18,432 Kb
	EP4SE820	1,320	48	18,792 Kb

Notes to Table 4-1:

- (1) In addition to device resource usage, Stratix IV device packages also determine the optimal HardCopy IV device mapping path. For example, the EP4SE360 device comes in H780 and F1152 packages. The mapping paths for the H780 and F1152 packages are the HC4E25 and HC4E35 devices, respectively.
- (2) HardCopy IV devices do not have dedicated MLAB blocks but can support the same Stratix IV MLAB functionality. The number of MLABs that are supported in HardCopy IV devices varies depending on resource usage and the Stratix IV device-to-HardCopy IV device mapping path.
- (3) The M144K blocks may lock up if there is a glitch in the clock source when rden equals 1. For more information and the workaround solution, refer to *M144K RAM Block Lock-Up* in the *Stratix IV GX Errata Sheet*, *Stratix IV GT Errata Sheet*, or *Stratix IV E Errata Sheet*.

With regards to functionality, memory in HardCopy IV devices and Stratix IV devices is identical. The memory blocks can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO. Table 4-2 lists the size and features of the different memory blocks. In addition, unused memory blocks in HardCopy IV devices are powered down, allowing the HardCopy IV devices to have significant power savings.

Table 4-2. Embedded Memory Features for HardCopy IV Devices (Part 1 of 2) (Note 1)

Feature	MLABs	M9K Blocks	M144K Blocks
Maximum performance	TBD	TBD	TBD
Total RAM bits (including parity bits)	640	9,216	147,456

Table 4-2. Embedded Memory Features for HardCopy IV Devices (Part 2 of 2) (Note 1)

Feature	MLABs	M9K Blocks	M144K Blocks
Configurations (depth × width)		8K × 1	16K × 8
		4K × 2	16K × 9
	64 × 8	2K × 4	8K × 16
	64 × 9	1K × 8	8K × 18
	64 × 10	1K × 9	4K × 32
	32 × 16	512 × 16	4K × 36
	32 × 18	512 × 18	2K × 64
	32 × 20	256 × 32	2K × 72
	256 × 36		
Parity bits	✓	✓	✓
Byte enable	✓	✓	✓
Packed mode	—	✓	✓
Address clock enable	✓	✓	✓
Single-port memory	✓	✓	✓
Simple dual-port memory	✓	✓	✓
True dual-port memory	—	✓	✓
Embedded shift register	✓	✓	✓
ROM (2)	✓	✓	✓
FIFO buffer	✓	✓	✓
Simple dual-port mixed width support	—	✓	✓
True dual-port mixed width support	—	✓	✓
Memory initialization file (.mif)	Not supported, except in ROM mode	Not supported, except in ROM mode	Not supported, except in ROM mode
Mixed-clock mode	✓	✓	✓
Power-up condition	Outputs cleared if registered, otherwise reads memory contents (2)	Outputs cleared	Outputs cleared
Register clears	Outputs cleared	Outputs cleared	Outputs cleared
Write and Read operation triggering	Write: Falling clock edges Read: Rising clock edges	Write and Read: Rising clock edges	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to old data or don't care	Outputs set to old or new data	Outputs set to old or new data
Mixed-port read-during-write	Outputs set to old data or don't care	Outputs set to old data	Outputs set to old data
ECC Support	Soft IP support using the Quartus II software	Soft IP support using the Quartus II software	Built-in support in ×64-wide SDP mode or soft IP support using the Quartus II software

Notes to Table 4-2:

- (1) Violating the setup and hold time on the memory block address registers could corrupt the memory contents. This applies to both read and write operations.
- (2) The memory contents for the MLAB in RAM mode are initialized to zero on power-up.



Violating the setup and hold time on the memory block address registers could corrupt the memory contents. This applies to both read and write operations.



For more information about embedded memory support in Stratix IV devices, refer to the *TriMatrix Embedded Memory Blocks in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*.

MLAB Implementation

While the M9K and M144K memory blocks are dedicated resources that function the same in Stratix IV and HardCopy IV devices, the MLABs are implemented differently in the two device families. In Stratix IV devices, the MLABs are dedicated blocks that you can configure for regular logic functions or memory functions. In HardCopy IV devices, the MLAB memory blocks are implemented using HCells. HCells are a collection of logic transistors connected together to form HCell macros (HCMs). The Quartus II software maps the Stratix IV MLAB function to the appropriate memory HCell macro that preserves the memory function. This allows the HardCopy IV core fabric to be used more efficiently, freeing up unused HCells for adaptive logic module (ALM) or digital signal processing (DSP) functions.



For more information about HCells in HardCopy IV devices, refer to the *Logic Array Block and Adaptive Logic Module Implementation in HardCopy IV Devices* chapter.

Design Considerations

Unlike Stratix IV devices, HardCopy IV devices do not have device configuration, so memories that are configured as RAM power up with random content. Therefore, the memory block contents cannot be pre-loaded or initialized with a memory initialization file (.mif) in HardCopy IV devices. You must ensure that your Stratix IV design does not require .mifs if you use the memory blocks as RAM. However, if you use the memory blocks as ROM, they are mask programmed to the design's ROM contents.



You can use the ALTMEM_INIT megafunction to initialize the RAM after power up for HardCopy IV devices. This megafunction reads from an internal ROM (inside the megafunction) or an external ROM (on chip or off chip) and writes to the RAM after power up.

When using non-registered output mode for the HardCopy IV MLAB memory blocks, the outputs power up with memory content. When using registered output mode for these memory blocks, the outputs are cleared on power up. You must take this into consideration when designing logic that might evaluate the initial power up values of the MLAB memory block.

Document Revision History

Table 4-3 lists the revision history for this chapter.

Table 4-3. Document Revision History

Date	Version	Changes
January 2011	2.2	<ul style="list-style-type: none">■ Updated Table 4-1.■ Updated the “Memory Resources and Features” section.■ Minor text edits.
January 2010	2.1	<ul style="list-style-type: none">■ Updated Table 4-1.■ Minor text edits.2011
June 2009	2.0	<ul style="list-style-type: none">■ Updated Table 4-1.■ Minor text edits.■ Removed the Conclusion and Referenced Documents sections.
December 2008	1.0	Initial release.

