

This chapter discusses the available options for mapping from a Stratix® IV device to a HardCopy® IV device.

The Quartus II software limits resources to those available to both the Stratix IV FPGA and the HardCopy IV ASIC. It also ensures that the design revision targeting a HardCopy IV device retains the same functionality as the original Stratix IV design.

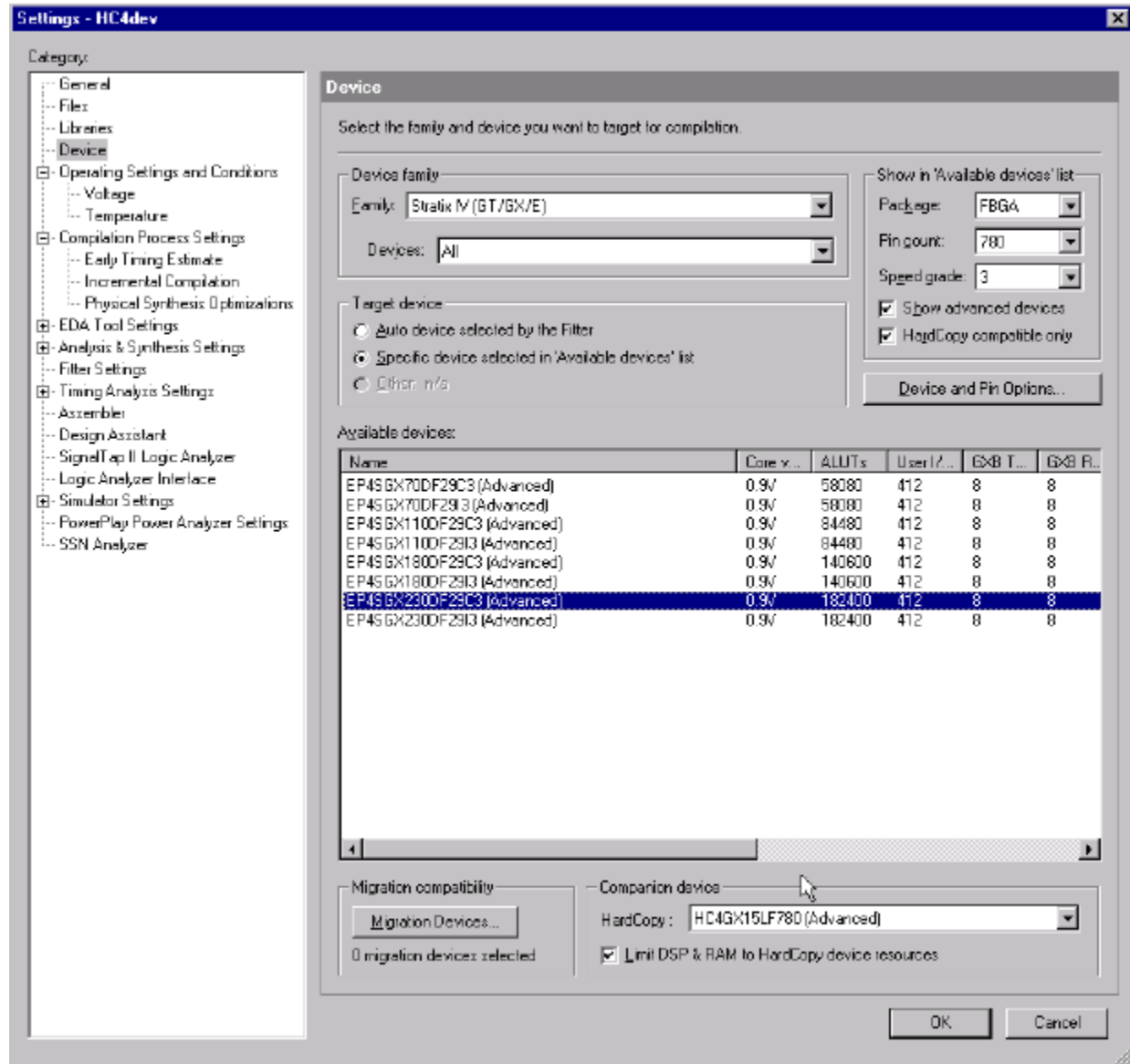
When compiling designs with the Quartus II software, you can specify one HardCopy IV target device and one or more Stratix IV mapping devices. When you specify at least one mapping device, the Quartus II compiler constrains I/O pins and relevant hard IP blocks to the minimum resources available in any of the selected mapping devices. This feature allows vertical mapping between devices using the same package footprint.

Selecting a HardCopy IV device as a companion device is similar to adding another Stratix IV device to the mapping device chain. The Quartus II software compiles the design to use the common resources available in all of the selected Stratix IV and HardCopy IV devices.


The HardCopy IV companion device becomes the target device when you create the HardCopy companion revision.

Figure 3-1 shows the **Device** page of the **Settings** dialog box, where you choose the companion device for the target device selected. The **Device** panel lists appropriate companion devices based on the target device you select.

Figure 3-1. Quartus II Device Settings Page with HardCopy IV Device Selected as Companion Device



When you select a HardCopy IV companion device, the Quartus II software fits your design to common resources in the I/Os, clock structures, PLLs, memory blocks, and core logic for digital signal processing (DSP).

 For more information about compiling with Stratix IV and HardCopy IV companion revisions using the Quartus II software, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

HardCopy IV and Stratix IV Mapping Options

HardCopy IV ASICs offer a wide range of family options that can map with various Stratix IV FPGAs.

Table 3–1 and Table 3–2 lists the available HardCopy IV and Stratix IV companion pairs.

Table 3–1. HardCopy IV GX and Stratix IV GX Companion Devices

Companion Pair		HardCopy IV Package
HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	
HC4GX15LAF780N	EP4SGX70DF29 (F780)	780-pin FineLine BGA
	EP4SGX110DF29 (F780)	
	EP4SGX180DF29 (F780)	
	EP4SGX230DF29 (F780)	
HC4GX15LF780N	EP4SGX290FH29 (H780)	780-pin FineLine BGA
	EP4SGX360FH29 (H780)	
HC4GX25LF780N	EP4SGX290FH29 (H780)	780-pin FineLine BGA
	EP4SGX360FH29 (H780)	
HC4GX25LF1152N	EP4SGX110FF35 (F1152)	1152-pin FineLine BGA
	EP4SGX180FF35 (F1152)	
	EP4SGX230FF35 (F1152)	
	EP4SGX290FF35 (F1152)	
	EP4SGX360FF35 (F1152)	
HC4GX25FF1152N	EP4SGX180HF35 (F1152)	1152-pin FineLine BGA
	EP4SGX230HF35 (F1152)	
	EP4SGX290HF35 (F1152)	
	EP4SGX360HF35 (F1152)	
	EP4SGX530HH35 (H1152)	
HC4GX35FF1152N	EP4SGX230HF35 (F1152)	1152-pin FineLine BGA
	EP4SGX360HF35 (F1152)	
	EP4SGX530HH35 (H1152)	
HC4GX35FF1517N	EP4SGX180KF40 (F1517)	1517-pin FineLine BGA
	EP4SGX230KF40 (F1517)	
	EP4SGX290KF40 (F1517)	
	EP4SGX360KF40 (F1517)	
	EP4SGX530KH40 (H1517)	

Table 3–2. HardCopy IV E and Stratix IV E Companion Devices (Part 1 of 2)

Companion Pair		HardCopy IV Package
HardCopy IV E ASIC	Stratix IV E FPGA Prototype	
HC4E25WF484N (1)	EP4SE230F29 (F780)	484-pin FineLine BGA Wire Bond
HC4E25FF484N (1)	EP4SE230F29 (F780)	484-pin FineLine BGA

Table 3-2. HardCopy IV E and Stratix IV E Companion Devices (Part 2 of 2)

Companion Pair		HardCopy IV Package
HardCopy IV E ASIC	Stratix IV E FPGA Prototype	
HC4E25WF780N	EP4SE230F29 (F780)	780-pin FineLine BGA Wire Bond
	EP4SE360H29 (H780)	
HC4E25FF780N	EP4SE230F29 (F780)	780-pin FineLine BGA
	EP4SE360H29 (H780)	
HC4E35LF1152N	EP4SE360F35 (F1152)	1152-pin FineLine BGA
	EP4SE530H35 (H1152)	
	EP4SE820H35 (H1152)	
HC4E35FF1152N	EP4SE360F35 (F1152)	1152-pin FineLine BGA
	EP4SE530H35 (H1152)	
	EP4SE820H35 (H1152)	
HC4E35LF1517N	EP4SE530H40 (H1517)	1517-pin FineLine BGA
	EP4SE820H40 (H1517)	
HC4E35FF1517N	EP4SE530H40 (H1517)	1517-pin FineLine BGA
	EP4SE820H40 (H1517)	

Note to Table 3-2:

- (1) This mapping is a non-socket replacement path that requires a different board design for the Stratix IV E device and the HardCopy IV E device. The Stratix IV E device is in a 780-pin FBGA package while the HardCopy IV E device is in a 484-pin FBGA package.

When the Quartus II software successfully compiles a design, the HardCopy Device Resource Guide in the Fitter Compilation Report contains information about mapping compatibility to a HardCopy IV device. Use this information to select the optimal HardCopy IV device for the prototype Stratix IV device based on resource and package requirements.

Table 3-3 and Table 3-4 show the available resources for prototyping on a Stratix IV device when choosing a HardCopy IV device.

Table 3-3. HardCopy IV GX ASIC Features

HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	ASIC Equivalent Gates (1)	Transceivers 6.5+Gbps (2)	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs) (3)	18 x 18-Bit Multipliers (FIR Mode)	PLLs
HC4GX15	EP4SGX70	2.8 M	8, 0	462	16	6,462 Kb	384	3
	EP4SGX110	3.8 M	8, 0	660	16	8,244 Kb	512	3
	EP4SGX180	6.7 M	8, 0	660	20	8,820 Kb	920	3
	EP4SGX230	9.2 M	8, 0	660	22	9,108 Kb	1288	3
	EP4SGX290	7.7 M	8, 0	660	24	9,396 Kb	832	2
	EP4SGX360	9.4 M	8, 0	660	24	9,396 Kb	1040	2
HC4GX25	EP4SGX110	3.8 M	16, 0	660	16	8,244 Kb	512	4
	EP4SGX180	6.7 M	16, 8 (6)	936	20	11,304 Kb	920	6
	EP4SGX230	9.2M	16, 8 (6)	936	22	11,592 Kb	1288	6
	EP4SGX290	7.7 M	16, 8 (6)	936	36	13,608 Kb	832	6 (4)
	EP4SGX360	9.4 M	16, 8 (6)	936	36	13,608 Kb	1040	6 (4)
	EP4SGX530	11.5 M	16, 8	936	36	13,608 Kb	1024	6
HC4GX35	EP4SGX180	6.7 M	24, 12 (7)	950	20	11,430 Kb	920	8
	EP4SGX230	9.2 M	24, 12 (7)	1235	22	14,283 Kb	1288	8 (5)
	EP4SGX290	7.7 M	24, 12 (7)	936	36	13,608 Kb	832	8
	EP4SGX360	9.4 M	24, 12 (7)	1248	48	18,144 Kb	1040	8 (5)
	EP4SGX530	11.5 M	24, 12 (7)	1280	64	20,736 Kb	1024	8 (5)

Notes to Table 3-3:

- (1) This is the number of ASIC-equivalent gates available in the HardCopy IV GX base array, shared between both adaptive logic module (ALM) logic and DSP functions from a Stratix IV GX FPGA prototype. The number of usable ASIC equivalent gates is bounded by the number of ALMs in the companion Stratix IV GX FPGA device.
- (2) The first number indicates the number of transceivers and the second number indicates the number of CMU (PMA only) transceivers.
- (3) HardCopy IV GX devices do not have dedicated MLABs, but the Stratix IV GX MLAB features and functions are supported in HardCopy IV GX devices.
- (4) This device has six PLLs in the F1152 package and four PLLs in the F780 package.
- (5) This device has eight PLLs in the F1517 package and six PLLs in the F1152 package.
- (6) Devices in the cost optimized LF780 and the LF1152 package have 16 transceivers and no CMU transceiver. Devices in the performance optimized FF1152 package have 16 transceivers and 8 CMU transceivers.
- (7) Devices in the F1152 package have 16 transceivers and eight CMU transceivers. Devices in the performance optimized FF1517 package have 24 transceivers and 12 CMU transceivers.

Table 3-4. HardCopy IV E ASIC Features

HardCopy IV E ASIC	Stratix IV E FPGA Prototype	ASIC Equivalent Gates (1)	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs) (2)	18 x 18-Bit Multipliers (FIR Mode)	PLLs
HC4E25	EP4SE230	9.2 M	864	22	10,944 Kb	1288	4
	EP4SE360	9.4 M	864	32	12,384 Kb	1040	4
HC4E35	EP4SE360	9.4 M	1,248	48	18,144 Kb	1040	8
	EP4SE530	11.5 M	1,280	48	18,432 Kb	1024	12 (3)
	EP4SE820	14.6 M	1,320	48	18,792 Kb	960	12 (3)

Notes to Table 3-4:

- (1) This is the number of ASIC-equivalent gates available in the HardCopy IV E base array, shared between both adaptive logic module (ALM) logic and DSP functions from a Stratix IV E FPGA prototype. The number of usable ASIC equivalent gates is bounded by the number of ALMs in the companion Stratix IV E FPGA device.
- (2) HardCopy IV E devices do not have dedicated MLABs, but the Stratix IV E MLAB features and functions are supported in HardCopy IV devices.
- (3) This device has 12 PLLs in the F1517 package and 8 PLLs in the F1152 package.

HardCopy IV ASICs offer pin-to-pin compatibility to the Stratix IV prototype, making them drop-in replacements for FPGAs. Due to this compatibility, the same system board and software developed for prototyping and field trials can be retained, enabling faster time-to-market for high-volume production.

HardCopy IV devices also offer non-socket replacement mapping for further cost reduction. For example, the EP4SE230 device in the 780-pin FBGA package can be mapped to the HC4E25 device in the 484-pin FBGA package. Because the pinout for the two packages are not the same, a separate board design is required for the Stratix IV device and the HardCopy IV device.



For the non-socket replacement path, select I/Os in the Stratix IV device that can be mapped to the HardCopy IV device. Not all I/Os in the Stratix IV device are available in the HardCopy IV non-socket replacement device. Check pinout information for both the Stratix IV device and the HardCopy IV device to ensure that you can map successfully, and select the HardCopy IV companion device when designing for the Stratix IV device.

Table 3-5 and Table 3-6 show available I/O pin counts by package for each Stratix IV and HardCopy IV companion pair.

Table 3-5. HardCopy IV GX and Stratix IV GX Package and I/O Pin Count Mapping

HardCopy IV GX ASIC (1)	Stratix IV GX FPGA Prototype	484-Pin FineLine BGA	780-Pin FineLine BGA (2)	1152-Pin FineLine BGA (3)	1517-Pin FineLine BGA (4)	1760-Pin FineLine BGA
HC4GX15LA	EP4SGX70	—	372	—	—	—
	EP4SGX110	—	372	—	—	—
	EP4SGX180	—	372	—	—	—
	EP4SGX230	—	372	—	—	—
HC4GX15L	EP4SGX290	—	257	—	—	—
	EP4SGX360	—	257	—	—	—
HC4GX25L	EP4SGX110	—	—	372	—	—
	EP4SGX180	—	—	564	—	—
	EP4SGX230	—	—	564	—	—
	EP4SGX290	—	289	564	—	—
	EP4SGX360	—	289	564	—	—
	EP4SGX530	—	—	—	—	—
HC4GX25F	EP4SGX110	—	—	—	—	—
	EP4SGX180	—	—	564	—	—
	EP4SGX230	—	—	564	—	—
	EP4SGX290	—	—	564	—	—
	EP4SGX360	—	—	564	—	—
	EP4SGX530	—	—	564	—	—
HC4GX35F	EP4SGX180	—	—	—	744	—
	EP4SGX230	—	—	564	744	—
	EP4SGX290	—	—	—	744	—
	EP4SGX360	—	—	564	744	—
	EP4SGX530	—	—	564	744	—

Notes to Table 3-5:

- (1) The last letter (two letters in the LA package) in the HardCopy IV GX name refers to the following package types: F—Performance-optimized flip chip package, L or LA—Cost-optimized flip-chip package.
- (2) The I/O pin count for the LAF780 package includes the four dedicated clock inputs (CLK1n, CLK1p, CLK3n, CLK3p). The I/O pin count for the LF780 package includes one dedicated clock input (CLK1p).
- (3) All I/O pin counts include four dedicated clock inputs (CLK1p, CLK1n, CLK10p, and CLK10n) that can be used as data inputs.
- (4) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) that can be used as data inputs.

Table 3-6. HardCopy IV E and Stratix IV E Package and I/O Pin Count Mapping (Part 1 of 2)

HardCopy IV E ASIC (1)	Stratix IV E FPGA Prototype	484-Pin FineLine BGA (2)	780-Pin FineLine BGA (2)	1152-Pin FineLine BGA (2)	1517-Pin FineLine BGA (3)	1760-Pin FineLine BGA
HC4E25W	EP4SE230	296 (4)	392	—	—	—
	EP4SE360	—	392	—	—	—

Table 3-6. HardCopy IV E and Stratix IV E Package and I/O Pin Count Mapping (Part 2 of 2)

HardCopy IV E ASIC (1)	Stratix IV E FPGA Prototype	484-Pin FineLine BGA (2)	780-Pin FineLine BGA (2)	1152-Pin FineLine BGA (2)	1517-Pin FineLine BGA (3)	1760-Pin FineLine BGA
HC4E25F	EP4SE230	296 (4)	488	—	—	—
	EP4SE360	—	488	—	—	—
HC4E35L	EP4SE360	—	—	744	—	—
	EP4SE530	—	—	744	880	—
	EP4SE820	—	—	744	880	—
HC4E35F	EP4SE360	—	—	744	—	—
	EP4SE530	—	—	744	880	—
	EP4SE820	—	—	744	880	—

Notes to Table 3-6:

- (1) The last letter in the HardCopy IV E device name refers to the following package types: F—Performance-optimized flip-chip package, L—Cost-optimized flip-chip package, W—Low-cost wirebond package.
- (2) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) that can be used for data inputs.
- (3) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used as data inputs.
- (4) This mapping is a non-socket replacement path and requires a different board design for the Stratix IV E device and the HardCopy IV E device. The Stratix IV E device is in a 780-Pin FineLine BGA package while the HardCopy IV E device is in a 484-Pin FineLine BGA package.

Summary of Differences Between HardCopy IV and Stratix IV Devices

HardCopy IV ASICs are functionally equivalent to Stratix IV FPGAs, but they have architectural differences. When implementing your design and laying out your board, consider the differences to ensure successful design mapping from the Stratix IV FPGA to the HardCopy IV ASIC.

Architectural differences between the Stratix IV FPGA and the HardCopy IV ASIC include:

- HardCopy IV devices have up to 20 I/O banks and 880 I/O pins, while the largest Stratix IV companion devices have up to 24 I/O banks and 976 I/O pins in the 1517-pin FBGA package.
- The number of global and regional clocks is identical for Stratix IV and HardCopy IV devices, but Stratix IV devices have up to 116 peripheral clocks, while HardCopy IV devices have up to 88. The Quartus II software limits the clock availability on Stratix IV and HardCopy IV companion pairs to ensure device compatibility.

- Configuration is not required for HardCopy IV devices; therefore, these Stratix IV features are not supported:
 - Programming modes and features such as remote update and Programmer Object File (.pof) encryption.
 - Cyclical redundancy check (CRC) for configuration error detection.
 - 256-bit (AES) volatile and non-volatile security key to protect designs.
 - JTAG instructions used for configuration.
 - FPGA configuration emulation mode is not supported.
- Boundary scan (BSCAN) chain length is different and varies with device density.
- Memory Initialization Files (.mif) for embedded memories used as RAM are not supported.
- Stratix IV LAB/MLAB and DSP functions are implemented with HCells in HardCopy IV devices instead of dedicated blocks.
- Stratix IV Programmable Power Technology is not supported in HardCopy IV devices. However, the HardCopy IV ASIC architecture offers performance on par with the Stratix IV devices with significantly low power.

Designing with HardCopy IV I/Os

HardCopy IV ASICs support a wide range of industry standards that match Stratix IV supported standards. HardCopy IV devices support 3.3 V I/O standards. The 3.3 V LVTTTL/LVCMOS I/O standard is supported using V_{CCIO} at 3.0 V.

HardCopy IV I/O standards support the same specifications as their Stratix IV companion equivalent. The I/O arrangement matches Stratix IV such that I/O pins located on the left and right side I/O banks contain circuits dedicated to high-speed differential I/O interfaces, but have the ability to support external memory devices if required. The top and bottom I/O banks contain dedicated circuitry to optimize external memory interfaces. They also have the ability to support high-speed differential inputs and outputs at lower speed than the left and right side banks.

 For more information, refer to the *HardCopy IV Device I/O Features* chapter.

Mapping HardCopy IV and Stratix IV I/Os and Modular I/O Banks

I/O pins in Stratix IV and HardCopy IV devices are arranged in groups called modular I/O banks. On Stratix IV devices, the number of I/O banks can range from 16 to 24 banks. On HardCopy IV devices, the number of I/O banks can range from 12 to 20 banks.

In both Stratix IV and HardCopy IV devices, the maximum number of I/O banks per side is four or six, depending on the device density. When migrating between devices with a different number of I/O banks per side, the middle or “B” bank is removed or inserted. For example, when moving from a 24-bank Stratix IV device to a 16-bank Stratix IV or HardCopy IV device, the banks that are dropped are “B” banks, namely 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B.

HardCopy IV devices do not have banks 1B, 2B, 5B, and 6B. When you design with a Stratix IV device that has 24 banks, the Quartus II software limits the available banks common to all devices selected if a HardCopy IV device is selected as a companion pair. If you try to assign I/O pins to a non-existent bank in a mapping or companion device, the Quartus II compilation halts with an error.

The following are examples of Quartus II compilation errors:

Error: I/O pins (xx) assigned in I/O bank 1B. The I/O bank does not exist in the selected device

Error: Device migration enabled -- compilation may have failed due to additional constraints when migrating

Error: Can't fit design in device

The sizes of each bank are 24, 26, 32, 40, 42, 48, or 50 I/O pins (including up to two dedicated input pins per bank). During mapping from a smaller device to a larger device, the bank size increases or remains the same but never decreases. For example, banks may increase from a size of 24 I/O to a bank of size 32, 40, 48, or 50 I/O, but will never decrease.

Table 3-7 summarizes the number of I/O pins available in each I/O bank for all companion pairs of Stratix IV GX and HardCopy IV GX devices.

Table 3-7. HardCopy IV GX ASIC and Stratix IV GX FPGA I/O Bank and Pin Count Mapping (Part 1 of 2) (Note 1)

Bank	780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		1152-Pin FineLine BGA (3)		1152-Pin FineLine BGA (3)		1517-Pin FineLine BGA (4)	
	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype (5)	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype (5)	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype
	HC4GX15	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	HC4GX15	EP4SGX290 EP4SGX360	HC4GX25L	EP4SGX290 EP4SGX360	HC4GX25L (8)	EP4SGX110	HC4GX25L HC4GX25F HC4GX35F	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (6)	HC4GX35F	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (7)
1A	32	32	—	—	—	—	32	32	48	48	48	48
1B	—	—	—	—	—	—	—	—	—	—	—	—
1C	26	26	1	1	1	1	26	26	42	42	42	42
2A	32	32	—	—	—	—	—	—	—	—	48	48
2B	—	—	—	—	—	—	—	—	—	—	—	—
2C	26	26	—	—	—	—	—	—	—	—	42	42
3A	40	40	40	40	40	40	40	40	40	40	40	40
3B	—	—	—	—	—	—	—	—	24	24	24	24
3C	24	24	24	32	32	32	24	24	32	32	32	32
4A	40	40	40	40	40	40	40	40	40	40	40	40
4B	—	—	—	—	—	—	—	—	24	24	24	24
4C	24	24	24	32	32	32	24	24	32	32	32	32
5A	—	—	—	—	—	—	—	—	—	—	48	48
5B	—	—	—	—	—	—	—	—	—	—	—	—
5C	—	—	—	—	—	—	—	—	—	—	42	42
6A	—	—	—	—	—	—	32	32	48	48	48	48
6B	—	—	—	—	—	—	—	—	—	—	—	—
6C	—	—	—	—	—	—	26	26	42	42	42	42

Table 3–7. HardCopy IV GX ASIC and Stratix IV GX FPGA I/O Bank and Pin Count Mapping (Part 2 of 2) (Note 1)

Bank	780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		1152-Pin FineLine BGA (3)		1152-Pin FineLine BGA (3)		1517-Pin FineLine BGA (4)	
	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype (5)	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype (5)	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype
	HC4GX15	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	HC4GX15	EP4SGX290 EP4SGX360	HC4GX25L	EP4SGX290 EP4SGX360	HC4GX25L (8)	EP4SGX110	HC4GX25L HC4GX25F HC4GX35F	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (6)	HC4GX35F	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (7)
7A	40	40	40	40	40	40	40	40	40	40	40	40
7B	—	—	—	—	—	—	—	—	24	24	24	24
7C	24	24	24	32	32	32	24	24	32	32	32	32
8A	40	40	40	40	40	40	40	40	40	40	40	40
8B	—	—	—	—	—	—	—	—	24	24	24	24
8C	24	24	24	32	32	32	24	24	32	32	32	32
Total I/O	372	372	257	289	289	289	372	372	564	564	744	744

Notes to Table 3–7:

- (1) User I/O pin counts are preliminary.
- (2) All I/O pin counts include four dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n) that can be used for data inputs. The EP4SGX290 and EP4SGX360 mappings include only one dedicated clock input (CLK1p) that can be used as data input.
- (3) All I/O pin counts include four dedicated clock inputs (CLK1p, CLK1n, CLK10p, and CLK10n) that can be used as data inputs.
- (4) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) that can be used as data inputs.
- (5) The EP4SGX290 and EP4SGX360 FPGAs are offered in the H780 package.
- (6) The EP4SGX530 FPGA is offered in the H1152 package.
- (7) The EP4SGX530 FPGA is offered in the H1517 package.
- (8) The HC4GX25L has 564 I/Os, but only 372 I/Os can be mapped if the FPGA EP4SGX110 is selected.

Table 3-8 and Table 3-9 summarize the number of I/O pins available in each I/O bank for all companion pairs of Stratix IV E and HardCopy IV E devices for socket replacement and non-socket replacement flows, respectively.

Table 3-8. HardCopy IV E ASIC and Stratix IV E FPGA Prototype I/O Pin Bank and Pin Count Mapping with Socket Replacement Flow (Part 1 of 2) (Note 1)

Bank	780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC (2)	Stratix IV E FPGA Prototype	HardCopy IV E ASIC (3)	Stratix IV E FPGA Prototype
	HC4E25W	EP4SE230 EP4SE360 (4)	HC4E25F	EP4SE230 EP4SE360 (4)	HC4E35F HC4E35L	EP4SE360 EP4SE530 (5) EP4SE820 (5)	HC4E35L HC4E35F	EP4SE530 (6) EP4SE820
1A	24	32	32	32	48	48	50	50
1B	—	—	—	—	—	—	—	24
1C	42	26	26	26	42	42	42	42
2A	24	32	32	32	48	48	50	50
2B	—	—	—	—	—	—	—	24
2C	42	26	26	26	42	42	42	42
3A	—	40	40	40	40	40	48	48
3B	—	—	—	—	24	24	48	48
3C	32	24	24	24	32	32	32	32
4A	—	40	40	40	40	40	48	48
4B	—	—	—	—	24	24	48	48
4C	32	24	24	24	32	32	32	32
5A	24	32	32	32	48	48	50	50
5B	—	—	—	—	—	—	—	24
5C	42	26	26	26	42	42	42	42
6A	24	32	32	32	48	48	50	50
6B	—	—	—	—	—	—	—	24
6C	42	26	26	26	42	42	42	42
7A	—	40	40	40	40	40	48	48
7B	—	—	—	—	24	24	48	48
7C	32	24	24	24	32	32	32	32
8A	—	40	40	40	40	40	48	48
8B	—	—	—	—	24	24	48	48
8C	32	24	24	24	32	32	32	32

Table 3–8. HardCopy IV E ASIC and Stratix IV E FPGA Prototype I/O Pin Bank and Pin Count Mapping with Socket Replacement Flow (Part 2 of 2) (Note 1)

Bank	780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC (2)	Stratix IV E FPGA Prototype	HardCopy IV E ASIC (3)	Stratix IV E FPGA Prototype
	HC4E25W	EP4SE230 EP4SE360 (4)	HC4E25F	EP4SE230 EP4SE360 (4)	HC4E35F HC4E35L	EP4SE360 EP4SE530 (5) EP4SE820 (5)	HC4E35L HC4E35F	EP4SE530 (6) EP4SE820
Total I/O	392	488	488	488	744	744	880	976

Notes to Table 3–8:

- (1) User I/O pin counts are preliminary.
- (2) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p and CLK10n) that can be used for data inputs.
- (3) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.
- (4) The EP4SE360 FPGA is offered in the H780 package.
- (5) The EP4SE530 and EP4SE820 FPGAs are offered in the H1152 package.
- (6) The EP4SE530 FPGA is offered in the H1517 package.

HardCopy IV ASICs offer the non-socket replacement flow to reduce design board space and cost. Because HardCopy IV and Stratix IV device packages are different, some Stratix IV device I/Os are not available in the HardCopy IV device. Table 3–9 shows the number of I/Os in each bank on Stratix IV and HardCopy IV devices for the non-socket replacement flow.

Table 3–9. HardCopy IV E and Stratix IV E I/O Bank and Count Mapping with Non-Socket Replacement Flow (Part 1 of 2) (Note 1)

Bank	484-pin FineLine BGA	780-Pin FineLine BGA
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25W HC4E25F	EP4SE230
1A	24	32
1B	—	—
1C	26	26
2A	24	32
2B	—	—
2C	26	26
3A	—	40
3B	—	—
3C	24	24
4A	—	40
4B	—	—

Table 3-9. HardCopy IV E and Stratix IV E I/O Bank and Count Mapping with Non-Socket Replacement Flow (Part 2 of 2) (Note 1)

Bank	484-pin FineLine BGA	780-Pin FineLine BGA
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25W HC4E25F	EP4SE230
4C	24	24
5A	24	32
5B	—	—
5C	26	26
6A	24	32
6B	—	—
6C	26	26
7A	—	40
7B	—	—
7C	24	24
8A	—	40
8B	—	—
8C	24	24
Total I/O	296	488

Note to Table 3-9:

- (1) User I/O pin counts are preliminary.

HardCopy IV Supported I/O Standards

HardCopy IV ASICs support the same I/O standards as Stratix IV FPGAs.

Table 3-10 lists I/O standards that HardCopy IV ASIC support.

Table 3-10. I/O Standards and Voltage Levels for HardCopy IV Devices (Part 1 of 3) (Note 1)

I/O Standard	Standard Support	V _{CCIO} (V)				V _{CCPD} (V) (Pre-Driver Voltage)	V _{REF} (V) (Input Ref Voltage)	V _{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
3.3-V LVTTTL (2)	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
3.3-V LVCMOS (2)	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
2.5-V LVTTTL/LVCMOS	JESD8-5	3.0/2.5	3.0/2.5	2.5	2.5	2.5	—	—
1.8-V LVTTTL/LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	—	—
1.5-V LVTTTL/LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	—	—

Table 3-10. I/O Standards and Voltage Levels for HardCopy IV Devices (Part 2 of 3) (Note 1)

I/O Standard	Standard Support	V _{CCIO} (V)				V _{CCPD} (V) (Pre-Driver Voltage)	V _{REF} (V) (Input Ref Voltage)	V _{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
1.2-V LVTTTL/LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	—	—
3.0-V PCI	PCI Rev 2.1	3.0	3.0	3.0	3.0	3.0	—	—
3.0-V PCI-X	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	—	—
SSTL-2 Class I	JESD8-9B	(3)	(3)	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	(3)	(3)	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	(3)	(3)	1.8	1.8	2.5	0.90	0.90
SSTL-18 Class II	JESD8-15	(3)	(3)	1.8	1.8	2.5	0.90	0.90
SSTL-15 Class I	—	(3)	(3)	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II	—	(3)	(3)	1.5	—	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	(3)	(3)	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	(3)	(3)	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	(3)	(3)	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II	JESD8-6	(3)	(3)	1.5	—	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	(3)	(3)	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II	JESD8-16A	(3)	(3)	1.2	—	2.5	0.6	0.6
Differential SSTL-2 Class I	JESD8-9B	(3)	(3)	2.5	2.5	2.5	—	1.25
Differential SSTL-2 Class II	JESD8-9B	(3)	(3)	2.5	2.5	2.5	—	1.25
Differential SSTL-18 Class I	JESD8-15	(3)	(3)	1.8	1.8	2.5	—	0.90
Differential SSTL-18 Class II	JESD8-15	(3)	(3)	1.8	1.8	2.5	—	0.90
Differential SSTL-15 Class I	—	(3)	(3)	1.5	1.5	2.5	—	0.75
Differential SSTL-15 Class II	—	(3)	(3)	1.5	—	2.5	—	0.75
Differential HSTL-18 Class I	JESD8-6	(3)	(3)	1.8	1.8	2.5	—	0.90
Differential HSTL-18 Class II	JESD8-6	(3)	(3)	1.8	1.8	2.5	—	0.90
Differential HSTL-15 Class I	JESD8-6	(3)	(3)	1.5	1.5	2.5	—	0.75
Differential HSTL-15 Class II	JESD8-6	(3)	(3)	1.5	—	2.5	—	0.75
Differential HSTL-12 Class I	JESD8-16A	(3)	(3)	1.2	1.2	2.5	—	0.60

Table 3-10. I/O Standards and Voltage Levels for HardCopy IV Devices (Part 3 of 3) (Note 1)

I/O Standard	Standard Support	V _{CCIO} (V)				V _{CCPD} (V) (Pre-Driver Voltage)	V _{REF} (V) (Input Ref Voltage)	V _{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
Differential HSTL-12 Class II	JESD8-16A	(3)	(3)	1.2	—	2.5	—	0.60
LVDS (4), (5)	ANSI/TIA/EIA-644	(3)	(3)	2.5	2.5	2.5	—	—
RSDS (6), (7)	—	(3)	(3)	2.5	2.5	2.5	—	—
mini-LVDS (6), (7)	—	(3)	(3)	2.5	2.5	2.5	—	—
LVPECL	—	(4)	2.5	—	—	2.5	—	—

Notes to Table 3-10:

- (1) V_{CCPD} is either 2.5 or 3.0 V. For V_{CCIO} = 3.0 V, V_{CCPD} = 3.0 V. For V_{CCIO} = 2.5 V or less, V_{CCPD} = 2.5 V.
- (2) The 3.3-V LVTTTL/LVCMOS standard is supported using V_{CCIO} at 3.0 V.
- (3) Single-ended HSTL/SSTL, differential SSTL/HSTL, and LVDS input buffers are powered by V_{CCPD}. Row I/O banks support both true differential input buffers and true differential output buffers. Column I/O banks support true differential input buffers, but not true differential output buffers. I/O pins are organized in pairs to support differential standards. Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip R_D support.
- (4) Column I/O banks support LVPECL I/O standards for input clock operation. Clock inputs on column I/O are powered by V_{CCCLKIN} when configured as differential clock input. They are powered by V_{CCIO} when configured as single-ended clock input. Differential clock inputs in row I/O are powered by V_{CCPD}.
- (5) Column and row I/O banks support LVDS outputs using two single-ended output buffers, an external one-resistor (LVDS_E_1R), and a three-resistor (LVDS_E_3R) network.
- (6) Row I/O banks support RSDS and mini-LVDS I/O standards using a dedicated LVDS output buffer without a resistor network.
- (7) Column and row I/O banks support RSDS and mini-LVDS I/O standards using two single-ended output buffers with one-resistor (RSDS_E_1R and mini-LVDS_E_1R) and three-resistor (RSDS_E_3R and mini-LVDS_E_3R) networks.

External Memory Interface I/Os in Stratix IV and HardCopy IV Devices

As with the Stratix IV I/O structure, the redesign of the HardCopy IV I/O structure provides flexible and high-performance support for existing and emerging external memory standards including DDR3, DDR2, DDR SDRAM, QDRII+, QDRII SRAM, and RLD RAM II.

HardCopy IV devices offer the same external memory interface features found in Stratix IV devices. These features include delay-locked loops (DLLs), phase-locked loops (PLLs), dynamic on-chip termination (OCT), trace mismatch compensation, read and write leveling, deskew circuitry, half data rate (HDR) blocks, 4- to 36-bit DQ group widths, and DDR external memory support on all sides of the HardCopy IV device.

As with Stratix IV devices, HardCopy IV devices allow a memory interface to be located on any side of the device. The only limitation is if the left and right sides have to be reserved for high-speed I/O applications, as described in the following section.

Table 3-11 and Table 3-12 show the number of DQ and DQS buses supported per companion device pair.

Table 3-11. Number of DQS/DQ Groups in HardCopy IV GX Devices per Side (Note 1)

HardCopy IV GX ASIC	Package	Side	x4 (2)	x8/x9	x16/x18	x32/x36
HC4GX15LA	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	0	0	0	0
		Top	17	8	2	0
HC4GX15L	780-pin FineLine BGA	Left	0	0	0	0
		Bottom	17	8	2	0
		Right	0	0	0	0
		Top	17	8	2	0
HC4GX25	1152-pin FineLine BGA	Left	13	6	2	0
		Bottom	26	12	4	0
		Right	13	6	2	0
		Top	26	12	4	0
HC4GX35	1152-pin FineLine BGA	Left	13	6	2	0
		Bottom	26	12	4	0
		Right	13	6	2	0
		Top	26	12	4	0
HC4GX35	1517-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0

Notes to Table 3-11:

- (1) These numbers are preliminary.
- (2) Some of the DQS and DQ pins can also be used as R_{UP}/R_{DN} pins. You lose one DQS/DQ group if you use these pins as R_{UP}/R_{DN} pins for OCT calibration. Make sure that the DQS/DQ groups that you have chosen are not also used for OCT calibration.

Table 3-12. Number of DQS/DQ Groups in HardCopy IV E Devices per Side (Note 1) (Part 1 of 2)


HardCopy IV E ASIC	Package	Side	x4 (2)	x8/x9	x16/x18	x32/x36
HC4E25	484-pin FineLine BGA	Left	12	4	0	0
		Bottom	5	2	0	0
		Right	12	4	0	0
		Top	5	2	0	0
HC4E25	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0

Table 3-12. Number of DQS/DQ Groups in HardCopy IV E Devices per Side (Note 1) (Part 2 of 2)

HardCopy IV E ASIC	Package	Side	x4 (2)	x8/x9	x16/x18	x32/x36
HC4E35	1152-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
HC4E35	1517-pin FineLine BGA	Left	26	12	4	0
		Bottom	38	18	8	4
		Right	26	12	4	0
		Top	38	18	8	4

Notes to Table 3-12:

- (1) These numbers are preliminary.
- (2) Some of the DQS and DQ pins can also be used as R_{UP}/R_{DN} pins. You lose one DQS/DQ group if you use these pins as R_{UP}/R_{DN} pins for OCT calibration. Make sure that the DQS/DQ groups that you have chosen are not also used for OCT calibration.

 For more information about external memory interfaces, refer to the *External Memory Interfaces in HardCopy IV Devices* chapter.

Mapping Stratix IV High-Speed Differential I/O Interfaces with HardCopy IV Devices

HardCopy IV ASICs have the same dedicated circuitry as Stratix IV devices for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog PLLs (located on left and right sides of the device)

For high-speed differential interfaces, HardCopy IV devices support the following differential I/O standards:

- Low-voltage differential signaling (LVDS)
- Mini-LVDS
- Reduced swing differential signaling (RSDS)
- Differential HSTL
- Differential SSTL

HardCopy IV ASICs support LVDS on all I/O banks. True LVDS makes use of dedicated LVDS I/O buffers that are optimized for performance. There are true LVDS input and output buffers at the left and right side I/O banks. There are true LVDS input buffers on the top and bottom I/O banks only.

You can configure all I/Os in all banks as emulated LVDS output buffers. Emulated output buffers make use of single-ended buffers and an external resistor network to mimic LVDS operation. Emulated LVDS is useful for low-speed, low-voltage differential applications.

 For more information about high-speed I/O performance, refer to the *High Speed Differential I/O Interface with DPA in HardCopy IV Devices* chapter.

All dedicated circuitry for high-speed differential I/O applications are located in the left and right I/O banks of the Stratix IV and HardCopy IV devices. The top and bottom I/O banks also have support for high-speed receiver applications that do not require the use of the DPA, synchronizer, data realignment, and differential termination. Top and bottom differential I/O buffers have a slower data rate than the high-speed receivers on the left and right I/O banks.

Table 3-13 shows the LVDS channels supported in HardCopy IV GX and Stratix IV GX companion devices.

Table 3-13. LVDS Channels Supported In HardCopy IV GX and Stratix IV GX Companion Devices (Note 1), (2) (Part 1 of 3)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype
	HC4GX15	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	HC4GX25	EP4SGX110	HC4GX25	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX230 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (4)
1A	8Rx + 8Tx	8Rx + 8Tx	8Rx + 8Tx	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
1B	—	—	—	—	—	—	—	—	—	—
1C	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
2A	8Rx + 8Tx	8Rx + 8Tx	8Rx + 8Tx	8Rx + 8Tx	—	12Rx + 12Tx	—	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
2B	—	—	—	—	—	—	—	—	—	—
2C	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	—	10Rx + 10Tx	—	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
3A (5)	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx	10Rx + 10eTx
	or 20eTx	or 20eTx	or 20eTx	or 20eTx	or 20eTx	or 20eTx	or 20eTx	or 20eTx	or 20eTx	or 20eTx

Table 3-13. LVDS Channels Supported In HardCopy IV GX and Stratix IV GX Companion Devices (Note 1), (2) (Part 2 of 3)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype
	HC4GX15	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	HC4GX25	EP4SGX110	HC4GX25	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX230 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (4)
3B (5)	—	—	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx
3C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
4A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx
4B (5)	—	—	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx
4C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
5A	—	—	—	—	—	12Rx + 12Tx	—	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
5B	—	—	—	—	—	—	—	—	—	—
5C	—	—	—	—	—	10Rx + 10Tx	—	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
6A	—	—	—	6Rx + 6Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
6B	—	—	—	—	—	—	—	—	—	—
6C	—	—	—	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
7A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx

Table 3-13. LVDS Channels Supported In HardCopy IV GX and Stratix IV GX Companion Devices (Note 1), (2) (Part 3 of 3)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype
	HC4GX15	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	HC4GX25	EP4SGX110	HC4GX25	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX230 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (4)
7B (5)	—	—	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx
7C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
8A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx
8B (5)	—	—	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx
8C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx

Notes to Table 3-13:

- (1) Channel counts are preliminary.
- (2) Rx = true LVDS input buffers with OCT RD, Tx = true LVDS output buffers, and eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
- (3) The EP4SGX530 FPGA is offered only in the H1152 package.
- (4) The EP4SGX530 FPGA is offered only in the H1517 package.
- (5) Top and bottom I/O banks do not have DPA, synchronizer, data realignment, and differential termination support in Stratix IV GX and HardCopy IV GX devices. Use left and right I/O banks if these features and maximum performance is required.

Table 3-15 and Table 3-14 show the LVDS channels supported in HardCopy IV E and Stratix IV E companion devices for the socket replacement and non-socket replacement flows, respectively.

Table 3-14. LVDS Channels Supported In HardCopy IV E and Stratix IV E Companion Devices with Socket Replacement Flow (Note 1), (2) (Part 1 of 2)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25	EP4SE230 EP4SE360 (3)	HC4E35	EP4SE360 EP4SE530 (4) EP4SE820 (4)	HC4E35	EP4SE530 (5) EP4SE820
1A	8Rx + 8Tx (7)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
1B	—	—	—	—	—	6Rx + 6Tx
1C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
2A	8Rx + 8Tx (7)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
2B	—	—	—	—	—	6Rx + 6Tx
2C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
3A (6)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
3B (6)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
3C (6)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
4A (6)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
4B (6)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
4C (6)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
5A	8Rx + 8Tx (7)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
5B	—	—	—	—	—	6Rx + 6Tx
5C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
6A	8Rx + 8Tx (7)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
6B	—	—	—	—	—	6Rx + 6Tx
6C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx

Table 3-14. LVDS Channels Supported In HardCopy IV E and Stratix IV E Companion Devices with Socket Replacement Flow (Note 1), (2) (Part 2 of 2)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25	EP4SE230 EP4SE360 (3)	HC4E35	EP4SE360 EP4SE530 (4) EP4SE820 (4)	HC4E35	EP4SE530 (5) EP4SE820
7A (6)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
7B (6)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
7C (6)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
8A (6)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
8B (6)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
8C (6)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx

Notes to Table 3-14:

- (1) Channel counts are preliminary.
- (2) Rx = true LVDS input buffers with OCT RD, Tx = true LVDS output buffers, and eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
- (3) The EP4SE360 FPGA is offered only in the H780 package.
- (4) The EP4SE530 and EP4SE820 FPGAs are offered only in the H1152 package.
- (5) The EP4SE530 FPGA is offered only in H1517 package.
- (6) Top and bottom I/O banks do not have DPA, synchronizer, data realignment, and differential termination support in Stratix IV E and HardCopy IV E devices. Use left and right I/O banks if these features and maximum performance is required.
- (7) When the HardCopy IV E devices mapped to use 780-pin FineLine BGA Wire Bond package, I/O banks 1A, 2A, 5A, and 6A can support 6 pairs of LVDS channel (6RX + 6Tx) only.

Table 3-15. LVDS Channels Supported In HardCopy IV E and Stratix IV E Companion Devices with Non-Socket Replacement Flow (Note 1), (2), (3) (Part 1 of 2)

Bank	484-Pin FineLine BGA	780-Pin FineLine BGA
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25	EP4SE230
1A	6Rx + 6Tx	8Rx + 8Tx
1B	—	—
1C	6Rx + 6Tx	6Rx + 6Tx
2A	6Rx + 6Tx	8Rx + 8Tx
2B	—	—
2C	6Rx + 6Tx	6Rx + 6Tx
3A (3)	—	10Rx + 10eTx or 20eTx
3B (3)	—	—
3C (3)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx
4A (3)	—	10Rx + 10eTx or 20eTx
4B (3)	—	—
4C (3)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx
5A	6Rx + 6Tx	8Rx + 8Tx
5B	—	—
5C	6Rx + 6Tx	6Rx + 6Tx
6A	6Rx + 6Tx	8Rx + 8Tx
6B	—	—
6C	6Rx + 6Tx	6Rx + 6Tx
7A (3)	—	10Rx + 10eTx or 20eTx
7B (3)	—	—
7C (3)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx

Table 3-15. LVDS Channels Supported In HardCopy IV E and Stratix IV E Companion Devices with Non-Socket Replacement Flow (Note 1), (2), (3) (Part 2 of 2)

Bank	484-Pin FineLine BGA	780-Pin FineLine BGA
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25	EP4SE230
8A (3)	—	10Rx + 10eTx or 20eTx
8B (3)	—	—
8C (3)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx

Notes to Table 3-15:

- (1) Channel counts are preliminary.
- (2) Rx = true LVDS input buffers with OCT RD, Tx = true LVDS output buffers, and eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
- (3) Top and bottom I/O banks do not have DPA, synchronizer, data realignment, and differential termination support in Stratix IV E and HardCopy IV E devices. Use left and right I/O banks if these features and maximum performance is required.

HardCopy IV PLL Planning and Utilization

HardCopy IV devices offer up to 12 PLLs that support the same features as Stratix IV PLLs. The same nomenclature is used for HardCopy IV and Stratix IV PLLs that follow their geographical location in the device floorplan. The PLLs that reside on the top and bottom sides of the device are named PLL_T1, PLL_T2, PLL_B1, and PLL_B2; the PLLs that reside on the left and right sides of the device are named PLL_L1, PLL_L2, PLL_L3, PLL_L4, PLL_R1, PLL_R2, PLL_R3, and PLL_R4, respectively.

Table 3-16 and Table 3-17 show the number of PLLs available in HardCopy IV devices and their companion Stratix IV devices.

Table 3-16. HardCopy IV GX and Stratix IV GX PLL Mapping Options (Note 1)

PLL	780-Pin FineLine BGA		780-Pin FineLine BGA		1152-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype	HardCopy IV GX ASIC	Stratix IV GX FPGA Prototype
	HC4GX15	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230 EP4SGX290 (2) EP4SGX360 (2)	HC4GX25	EP4SGX290 (2) EP4SGX360 (2)	HC4GX25	EP4SGX110 EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX230 EP4SGX360 EP4SGX530 (3)	HC4GX35	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530 (4)
PLL_L1	—	—	—	—	—	—	—	—	—	—
PLL_L2	✓ (5)	✓	✓	✓	✓	✓	✓	✓	✓	✓
PLL_L3	—	—	—	—	—	—	—	—	✓	✓
PLL_L4	—	—	—	—	—	—	—	—	—	—
PLL_T1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PLL_T2	—	—	✓	✓	✓	✓	✓	✓	✓	✓
PLL_B1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PLL_B2	—	—	✓	✓	✓	✓	✓	✓	✓	✓
PLL_R1	—	—	—	—	—	—	—	—	—	—
PLL_R2	—	—	✓	✓	✓	✓	✓	✓	✓	✓
PLL_R3	—	—	—	—	—	—	—	—	✓	✓
PLL_R4	—	—	—	—	—	—	—	—	—	—

Notes to Table 3-16:

- (1) The PLL availability table is preliminary. It is best to design with the Quartus II software to check if your design can use all available PLLs.
- (2) The EP4SGX290 and EP4SGX360 FPGAs are offered only in the H780 package.
- (3) The EP4SGX530 FPGA is offered only in the H1152 package.
- (4) The EP4SGX530 FPGA is offered only in the H1517 package.
- (5) The HC4GX15 does not have PLL_L2 if the FPGA EP4SGX290 or EP4SGX360 is selected.

Table 3-17. HardCopy IV E and Stratix IV E PLL Mapping Options *(Note 1)*

PLL	484-Pin FineLine BGA	780-Pin FineLine BGA	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype	HardCopy IV E ASIC	Stratix IV E FPGA Prototype
	HC4E25	EP4SE230	HC4E25	EP4SE230 EP4SE360 (2)	HC4E35	EP4SE360 EP4SE530 (3) EP4SE820 (3)	HC4E35	EP4SE530 (4) EP4SE820
PLL_L1	—	—	—	—	—	—	✓	✓
PLL_L2	✓	✓	✓	✓	✓	✓	✓	✓
PLL_L3	—	—	—	—	✓	✓	✓	✓
PLL_L4	—	—	—	—	—	—	✓	✓
PLL_T1	✓	✓	✓	✓	✓	✓	✓	✓
PLL_T2	—	—	—	—	✓	✓	✓	✓
PLL_B1	✓	✓	✓	✓	✓	✓	✓	✓
PLL_B2	—	—	—	—	✓	✓	✓	✓
PLL_R1	—	—	—	—	—	—	✓	✓
PLL_R2	✓	✓	✓	✓	✓	✓	✓	✓
PLL_R3	—	—	—	—	✓	✓	✓	✓
PLL_R4	—	—	—	—	—	—	✓	✓

Notes to Table 3-17:


- (1) The PLL availability table is preliminary. It is best to design with the Quartus II software to check if your design can use all available PLLs.
- (2) The EP4SE360 FPGA is offered only in the H780 package.
- (3) The EP4SE530 and EP4SE820 FPGAs are offered only in the H1152 package.
- (4) The EP4SE530 FPGA is offered only in the H1517 package.

 For more information about HardCopy IV PLLs, refer to the *Clock Networks and PLLs in HardCopy IV Devices* chapter.

HardCopy IV Memory Blocks

TriMatrix memory in HardCopy IV devices supports the same memory functions and features as Stratix IV devices. You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register using the MegaWizard™ Plug-In Manager in the Quartus II software.

HardCopy IV embedded memory consists of MLAB, M9K, and M144K memory blocks, and has one-to-one mapping from Stratix IV memory. However, the number of available memory blocks differs based on physical density, package, and Stratix IV device to HardCopy IV ASIC mapping paths. The Quartus II software may not allow all available Stratix IV memory types to fit into a selected HardCopy IV device if your design has a very high resource utilization and performance target.

 Altera recommends that you compile your design with the Quartus II software and verify the device resource guide to check for available resources in the HardCopy IV device.

 For information about using the HardCopy Device Resource Guide, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

Functionally, memory in HardCopy IV and Stratix IV devices is identical. Memory blocks can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO.




Violating the setup or hold-time on the memory block address registers could corrupt the memory contents. This applies to both read and write operations.

MLAB Implementation

In Stratix IV devices, MLABs are dedicated blocks and can be configured for regular logic functions or memory functions. In HardCopy IV devices, MLAB memory blocks are implemented using HCells. The Quartus II software maps the Stratix IV MLAB function to the appropriate memory HCell macro that preserves memory function. This allows you to use the HardCopy IV core fabric more efficiently, freeing up unused HCells for ALM or DSP functions.

MLAB, M9K, and M144K Utilization

HardCopy IV MLAB, M9K, and M144K block functionality is similar to Stratix IV memory blocks; however, you cannot pre-load HardCopy IV MLAB, M9K, and M144K blocks with a `.mif` file when using them as RAM. Ensure that your Stratix IV design does not require `.mif` files if the memory blocks are used as RAM. However, if memory blocks are used as ROM, they are mask-programmed to the design's ROM contents.

 You can use the `ALTMEM_INIT` megafunction to initialize a RAM block after power-up for Stratix IV and HardCopy IV devices. This megafunction reads from a ROM defined with the megafunction and writes to the RAM after power-up. This function allows you to have initialized contents on a RAM block. Refer to the Quartus II Help for implementation information about this function.

Unlike Stratix IV FPGAs, HardCopy IV MLAB, M9K, and M144K RAM contents are unknown after power-up. However, like Stratix IV devices, all HardCopy IV memory output registers power-up cleared, if used. When designing HardCopy IV memory blocks as RAM, Altera recommends a write-before-read of the memory block to avoid reading unknown initial power-up data conditions. If the HardCopy IV memory block is designated as ROM, it powers up with the ROM contents.

One advantage over Stratix IV RAM blocks is that unused M9K and M144K blocks are disconnected from the power rails and MLABs are only implemented as required by your design. These unused resources do not contribute to overall power consumption on HardCopy IV devices.

- For a list of supported features in HardCopy IV memory blocks, refer to the *TriMatrix Embedded Memory Blocks in HardCopy IV Devices* chapter.

Using JTAG Features in HardCopy IV Devices

HardCopy IV ASICs support the same boundary-scan test (BST) functionality as Stratix IV FPGAs. However, no reconfiguration is possible because HardCopy IV devices are mask-programmed. Therefore, HardCopy IV devices do not support instructions to reconfigure the device through the JTAG pins. HardCopy IV boundary scan lengths also differ from Stratix IV devices.

- For information about HardCopy IV JTAG functionality and support, refer to the *IEEE 1149.1 JTAG Boundary Scan Testing in HardCopy IV Devices* chapter.

Power-Up and Configuration Pin Compatibility with Stratix IV Devices

When designing a board for both HardCopy IV and Stratix IV devices, most configuration pins required by the Stratix IV device are not required by the HardCopy IV device. The functions of these Stratix IV configuration pins are not carried over to the HardCopy IV companion device because HardCopy IV devices are not programmable. To simplify the board connection for these configuration pins, Altera recommends minimizing the power-up and configuration pins that do not carry over from a Stratix IV device to a HardCopy IV device. You should ensure that the board can be used for both Stratix IV and HardCopy IV devices. Configuration pins for both devices must be properly connected. Otherwise, separate boards are required for the two devices.

Table 3–18 lists the main and optional functions on the configuration pins used by Stratix IV and HardCopy IV devices.

Table 3–18. Mapping Configuration Pins into HardCopy IV Devices (Part 1 of 2) (Note 1), (2), (3), (4)

Stratix IV FPGA Prototype		HardCopy IV ASIC		Board Connection
Main Function	Optional Function	Main Function	Optional Function	
MSEL [2..0]	—	—	—	Not required and no connection on board.
nCONFIG (5)	—	nCONFIG	—	Required connection.
I/O pin	DATA0	I/O pin	DATA0	DATA[0] retains both user I/O and optional EPCS access functions. DATA [7..1] retains user I/O functions only.
I/O pin	DATA [7..1]	I/O pin	—	
DCLK	—	DCLK	—	No Connection on Board, except when EPCS access is required in user mode.
I/O pin	INIT_DONE (6)	I/O pin	INIT_DONE	Retains the same I/O functions from Stratix IV.
I/O pin	CLKUSR	I/O pin	—	Retains the same I/O functions from Stratix IV except CLKUSR, because no device programming is required.
nSTATUS (5)	—	nSTATUS	—	Required connection.
CONF_DONE (5)	—	CONF_DONE	—	Required connection.
nCE	—	nCE	—	Required connection.

Table 3–18. Mapping Configuration Pins into HardCopy IV Devices (Part 2 of 2) (Note 1), (2), (3), (4)

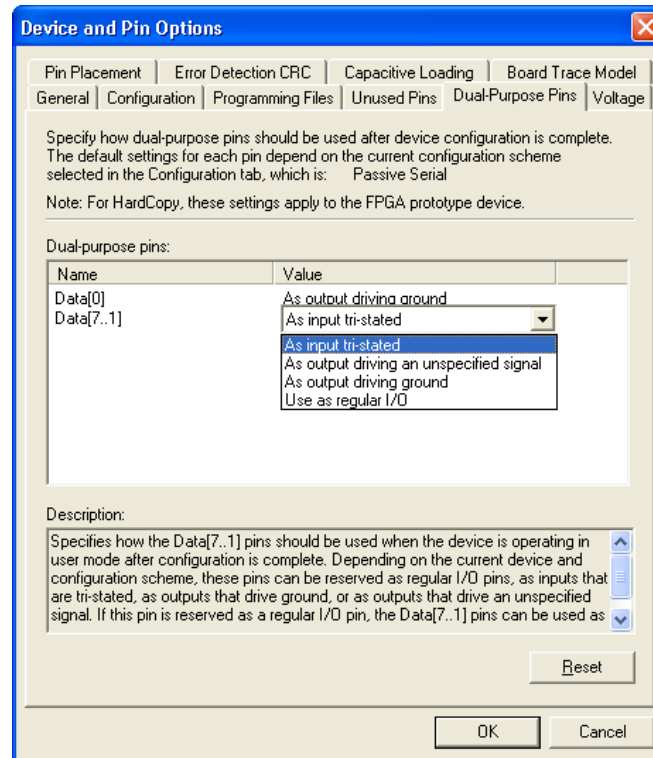
Stratix IV FPGA Prototype		HardCopy IV ASIC		Board Connection
Main Function	Optional Function	Main Function	Optional Function	
nCEO	—	nCEO	—	Not required and no connection on board.
PORSEL	—	PORSEL	—	Required connection.
I/O pin	ASDO	I/O pin	ASDO	No connection on board, except when EPCS access is required in user mode.
I/O pin	nCSO	I/O pin	nCSO	No connection on board, except when EPCS access is required in user mode.
nIO_PULLUP	—	nIO_PULLUP	—	Required connection.
I/O pin	CRC_ERROR (4)	I/O pin	—	Retains the same I/O functions from Stratix IV, but not CRC_ERROR, because no device programming is required.
I/O pin	DEV_CLRn	I/O pin	DEV_CLRn	Retains the same I/O functions from Stratix IV.
I/O pin	DEV_OE	I/O pin	DEV_OE	Retains the same I/O functions from Stratix IV.

Notes to Table 3–18:

- (1) For correct operation of a HardCopy IV device, pull the nSTATUS, nCONFIG, and CONF_DONE pins to V_{CCPGM}. In HardCopy IV devices, these pins are designed with weak internal resistors pulled up to V_{CCPGM}. Stratix IV configuration schemes require pull-up resistors on these I/O pins, so they may already be present on the board. You can remove these external pull-up resistors, if doing so does not affect other FPGAs on the board.
- (2) HardCopy IV devices have a maximum V_{CCIO} voltage of 3.0 V, but the input I/O pin can tolerate a 3.3 V level. This applies to V_{CCPGM} voltage and all dedicated and dual-purpose pins.
- (3) For HardCopy IV devices, there is weak pull-up on the nSTATUS, CONF_DONE, nCONFIG, and DCLK pins. Therefore, these pins can be left floating or remain connected to external pull-up resistors. If the EPCS is used in user mode as a boot-up RAM or data access for a Nios® II processor, DCLK, DATA[0], ASDO, and nCSO must be connected to the EPCS device.
- (4) In HardCopy IV devices, CRC_ERROR is hard-wired to logic 0 if the CRC feature is enabled in Stratix IV devices.
- (5) The PORSEL pin setting delays the POR sequence for both HardCopy IV and Stratix IV devices.
- (6) The INIT_DONE settings option is mask-programmed into the device. You must submit these settings to Altera with the final design prior to mapping to a HardCopy IV device. The use of the INIT_DONE option and other dual-purpose pins (for example, DEV_CLRn device-wide reset and DEV_OE device-wide output enable) are available in the **Fitter Device Options** section of the Quartus II report file.

For both the Stratix IV and HardCopy IV devices, the Quartus II software allows you to set the I/O pins listed in Table 3-18 as dual-purpose pins (as shown in Figure 3-2). As dual-purpose pins, they have I/O functionality when the device enters user mode (when INIT_DONE is asserted).

Figure 3-2. Device and Pin Options Dialog Box



If these dual-purpose pins are required to configure the Stratix IV device, but will be unused after configuration, these pins remain unused on the HardCopy IV device. It is important to consider the state of these pins after power-up and when the device is in user mode. For example, when replacing the Stratix IV device with a HardCopy IV device, these pins may be left floating when the configuration device is removed if you assign such pins as inputs. In this case, you will either require an external means to drive them to a stable level, or set the pins to output driving ground.

Revision History

Table 3-19 shows the revision history for this document.

Table 3-19. Document Revision History (Part 1 of 2)

Date	Version	Changes
January 2011	2.2	Minor text edits.
January 2010	2.1	Updated Table 3-2, Table 3-3, Table 3-6, Table 3-8, Table 3-9, Table 3-13, Table 3-18, Table 3-22, Table 3-23, Table 3-24, Table 3-28, and Table 3-29.

Table 3-19. Document Revision History (Part 2 of 2)

Date	Version	Changes
June 2009	2.0	<ul style="list-style-type: none">■ Added Table 3-13.■ Updated the following tables: Table 3-1, Table 3-5, Table 3-8, Table 3-12, Table 3-17, Table 3-18,■ Updated Figure 3-1.■ Updated “HardCopy IV and Stratix IV Mapping Options” and “Mapping HardCopy IV and Stratix IV I/Os and Modular I/O Banks.”■ Removed “Referenced Documents.”
December 2008	1.0	Initial release.

