

Introduction

Configuring an FPGA is the process of loading the design data into the device. Altera's SRAM-based Stratix® II, Stratix, APEX™ 20KC, and APEX 20KE FPGAs require configuration each time the device is powered up. After the device is powered down, the configuration data within the Stratix II, Stratix, or APEX device is lost and must be loaded again on power up.

There are several ways to configure these FPGAs. The details on the various configuration schemes available for these FPGAs are explained in the *Configuration Handbook*.

HardCopy® series devices are mask-programmed and cannot be configured. However, in addition to the capability of being instantly on upon power up (like a traditional ASIC device), these devices can mimic the behavior of the FPGA during the configuration process if necessary.

This chapter addresses various power-up options for HardCopy series devices. This chapter also discusses how configuration is emulated in HardCopy series devices while retaining the benefits of seamless migration and provides examples of how to replace the FPGAs in the system with HardCopy series devices.

HardCopy Power-Up Options

HardCopy series devices feature three variations of instant on power-up modes and a configuration emulation power-up mode. They are as follows:

- Instant on
- Instant on after 50 ms
- Configuration emulation of an FPGA configuration sequence



You must choose the power-up option when submitting the design database to Altera for migrating to a HardCopy series device. Once the HardCopy series devices are manufactured, the power-up option cannot be changed.



HardCopy II and some HardCopy Stratix devices do not support configuration emulation. Refer to [“Configuration Emulation of FPGA Configuration Sequence”](#) on page 12-9 for more information.



HardCopy II and HardCopy Stratix devices retain the functionality of VCCSEL and PORSEL pins from the prototyping Stratix and Stratix II FPGAs. The signals can affect the HardCopy series power-up behavior using any power up option. Refer to the *Stratix Device Handbook* or the *Stratix II Device Handbook* for proper use of these additional signals.

Instant On Options

Instant on is the traditional power-up scheme of most ASIC and non-volatile devices. The instant on mode is the fastest power-up option of a HardCopy series device and is used when the HardCopy series device powers up independently while other components on the board still require initialization and configuration. Therefore, you must verify all signals that propagate to and from the HardCopy series device (for example, reference clocks and other input pins) are stable or do not affect the HardCopy series device operation.

There are two variations of instant on power-up modes available on all HardCopy devices.

- Instant on (no added delay)
- Instant on after 50 ms (additional delay)

Instant On (No Added Delay)

In the instant on power-up mode, once the power supplies ramp up above the HardCopy series device's power-on reset (POR) trip point, the device initiates an internal POR sequence. When this sequence is complete, the HardCopy series device transitions to an initialization phase, which releases the CONF_DONE signal to be pulled high. Pulling the CONF_DONE signal high indicates that the HardCopy series device is ready for normal operation. Figures 12-1 to 12-3 show the instant on timing waveform relationships of the configuration signals, V_{CC}, and user I/O pins with respect to the HardCopy series device's normal operation mode.

During the power-up sequence, internal weak pull-up resistors can pull the user I/O pins high. Once POR and the initialization phase is complete, the I/O pins are released. Similar to the FPGA, if the nIO_pullup pin transitions high, the weak pull-up resistors are disabled. Refer to the table that provides recommended operating conditions in the handbook for the specific device.

The value of the internal weak pull-up resistors on the I/O pins is in the Operating Conditions table of the specific FPGA's device handbook.

Instant On After 50-ms Delay

The instant on after 50-ms delay power-up mode is similar to the instant on power-up mode. However, in this case, the device waits an additional 50 ms following the end of the internal POR sequence before releasing the CONF_DONE pin. This option is useful if other devices on the board (such as a microprocessor) must be initialized prior to the normal operation of the HardCopy series device.

An on-chip oscillator generates the 50-ms delay after the power-up sequence. During the POR sequence and delay period, all user I/O pins can be driven high by internal, weak pull-up resistors. Just like the instant on mode, these pull-up resistors are affected by the nIO_pullup pin.

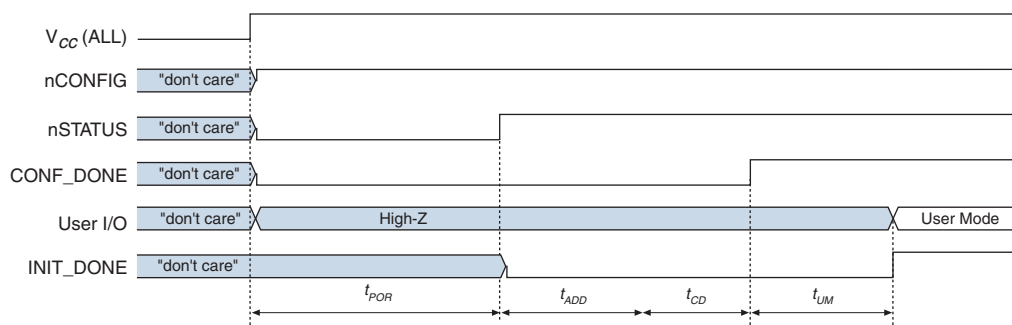


Similar to APEX 20K FPGAs, HardCopy APEX devices do not have an nIO_pullup function. Their internal, weak pull-up resistors are enabled during the power-up and initialization phase.

On the FPGA, an initialization phase occurs immediately after configuration where registers are reset, any PLLs used are initialized, and any I/O pins used are enabled as the device transitions into user mode. When the HardCopy series device uses instant on and instant on after 50-ms modes, a configuration sequence is not necessary, so the HardCopy series device transitions into the initialization phase after a power-up sequence immediately or after a 50-ms delay.

Figures 12-1 to 12-3 show instant on timing waveform relationships of the configuration signals, V_{CC}, and user I/O pins with respect to the HardCopy series device's normal operation mode. Tables 12-1 to 12-3 define the timing parameters for each of the HardCopy series device waveforms, and also show the effect of the PORSEL pin on power up. The nCE pin must be driven low externally for these waveforms to apply.

Figure 12-1 shows an instant on power-up waveform, where the HardCopy device is powered up, and the nCONFIG, nSTATUS, and CONF_DONE are not driven low externally.

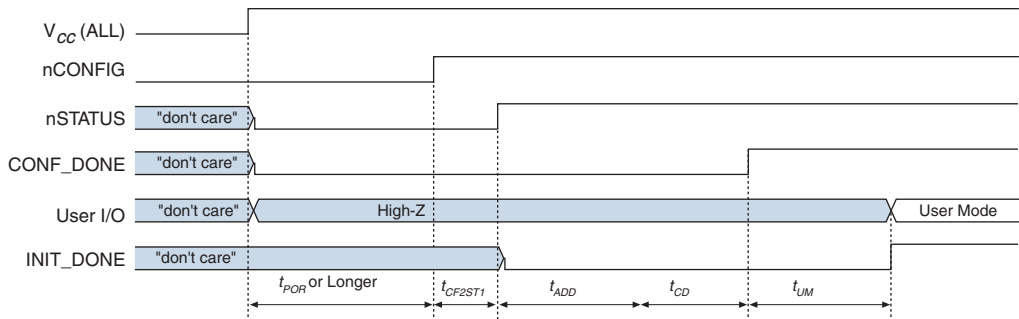
Figure 12–1. Timing Waveform for Instant On Option Notes (1), (2), (3), (4), (5)**Notes to Figure 12–1:**

- (1) V_{CC} (ALL) represents either all of the power pins or the last power pin powered up to specified operating conditions. All HardCopy power pins must be powered within specifications as described under *Hot Socketing* sections.
- (2) nCONFIG, nSTATUS, and CONF_DONE must not be driven low externally for this waveform to apply.
- (3) User I/O pins may be tri-stated or driven before and during power up. See the *Hot Socketing* sections for more details. The nIO_pullup pin can affect the state of the user I/O pins during the initialization phase.
- (4) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus II software. HardCopy series devices carry over the INIT_DONE functionality from the prototyped FPGA design.
- (5) The nCEO pin is asserted about the same time the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply.

An alternative to the power-up waveform in Figure 12–1 is if the nCONFIG pin is externally held low longer than the PORSEL delay. This delays the initialization sequence by a small amount as indicated in Figure 12–2.

In addition, Figure 12–2 is an instant on power-up waveform where nCONFIG is momentarily held low and nSTATUS and CONF_DONE are not driven low externally.

Figure 12–2. Timing Waveform for Instant On Option Where nCONFIG is Held Low After Power Up Notes (1), (2), (3), (4), (5), (6)



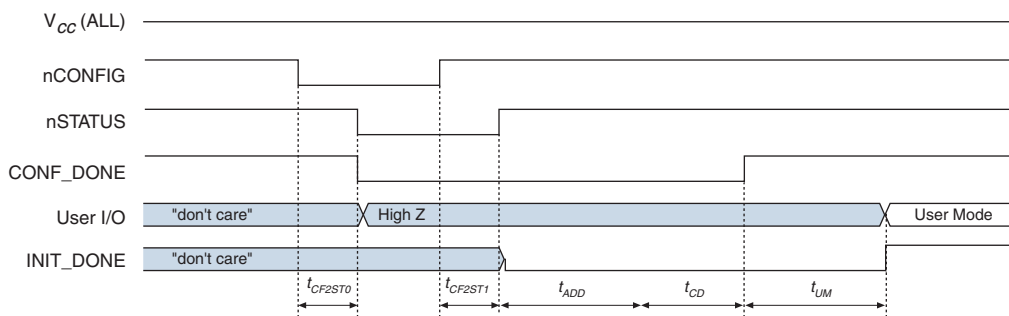
Notes to Figure 12–2:

- (1) This waveform applies if nCONFIG is held low longer than t_{POR} delay.
- (2) V_{CC} (ALL) represents either all of the power pins or the last power pin powered up to specified operating conditions. All HardCopy power pins must be powered within specifications as described under *Hot Socketing* sections.
- (3) nCONFIG, nSTATUS, and CONF_DONE must not be driven low externally for this waveform to apply.
- (4) User I/O pins may be tri-stated or driven before and during power up. See the *Hot Socketing* sections for more details. The nIO_pullup pin can affect the state of the user I/O pins during the initialization phase.
- (5) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus II software. HardCopy devices carry over the INIT_DONE functionality from the prototyped FPGA design.
- (6) The nCEO pin is also asserted about the same time the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply.

Pulsing the nCONFIG signal on an FPGA re-initializes the configuration sequence. The nCONFIG signal on a HardCopy series device also restarts the initialization sequence.

Figure 12–3 shows the instant on behavior of the configuration signals and user I/O pins if the nCONFIG pin is pulsed while the V_{CC} supplies are already powered up and stable.

Figure 12–3. Timing Waveform for Instant On Option When Pulsing NConfig Notes (1), (2), (3), (4), (5)



Notes to Figure 12–3:

- (1) V_{CC} (ALL) represents either all of the power pins or the last power pin powered up to specified operating conditions. All HardCopy power pins must be powered within specifications as described under *Hot Socketing* sections.
- (2) nSTATUS and CONF_DONE must not be driven low externally for this waveform to apply.
- (3) The nIO_pullup pin can affect the state of the user I/O pins during the initialization phase.
- (4) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus II software. HardCopy devices carry over the INIT_DONE functionality from the prototyped FPGA design.
- (5) The nCEO pin is also asserted about the same time the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply.



In the FPGA, the INIT_DONE signal remains high for several clock cycles after the nCONFIG signal is asserted, after which time INIT_DONE goes low. In the HardCopy series device, the INIT_DONE signal starts low, as shown in Figure 12–3, regardless of the logic state of the nCONFIG signal. The INIT_DONE signal transitions high only after the CONF_DONE signal transitions high.

Tables 12–1 through 12–3 show the timing parameters for the instant on mode. These tables also show the time taken for completing the instant on power-up sequence in Figure 12–1 on page 12–4 for HardCopy series devices. This option is typical of an ASIC’s functionality.

Table 12–1. Timing Parameters for Instant On Mode in HardCopy II Devices

Parameter	Description	Condition	Min	Typical	Max	Units
t_{POR}	PORSEL delay (1)	12		12		ms
		100		100		ms
t_{CF2ST0}	nCONFIG low to nSTATUS low (1)				800	ns
t_{CF2ST1}	nCONFIG high to nSTATUS high (1)				100	μ s
t_{ADD}	Additional delay	Instant on	33		60	μ s
		After 50 ms added delay	50		90	ms
t_{CD}	CONF_DONE delay		600		1100	ns
t_{UM}	User mode delay		25		55	μ s

Note to Table 12–1:

- (1) This parameter is similar to the Stratix II FPGA specifications. Refer to the *Configuration Handbook* for more information.

Table 12–2. Timing Parameters for Instant On Mode in HardCopy Stratix Devices

Parameter	Description	Condition	Min	Typical	Max	Units
t_{POR}	PORSEL delay	2	1	2		ms
		100	70	100		ms
t_{CF2ST0}	nCONFIG low to nSTATUS low (1)				800	ns
t_{CF2ST1}	nCONFIG high to nSTATUS high (1)				40	μ s
t_{ADD}	Additional delay	Instant on	4		8	ms
		After 50 ms added delay	25	50	75	ms
t_{CD}	CONF_DONE delay		0.5		3	μ s
t_{UM}	User mode delay		6.0		28	μ s

Note to Table 12–2

- (1) This parameter is similar to the Stratix FPGA specifications. Refer to the *Configuration Handbook* for more information.

Table 12–3. Timing Parameters for Instant On Mode in HardCopy APEX Devices

Parameter	Description	Condition	Min	Typical	Max	Units
t_{POR}	POR delay			5		μ s
t_{CF2ST0}	nCONFIG low to nSTATUS low (1)				200	ns
t_{CF2ST1}	nCONFIG high to nSTATUS high (1)				1	μ s
t_{ADD}	Additional delay	Instant on		0		μ s
		After 50 ms added delay		50		ms
t_{CD}	CONF_DONE delay		0.5		3	μ s
t_{UM}	User mode delay		2.5		8	μ s

Note to Table 12–3:

- (1) This parameter is similar to the APEX FPGA specifications. Refer to the *Configuration Handbook* for more information.

For correct operation of a HardCopy series device using the instant on option, pull the nSTATUS, nCONFIG, and CONF_DONE pins to V_{CC} . In the HardCopy series devices, these pins are designed with weak internal resistors pulled up to V_{CC} . Many FPGA configuration schemes require pull-up resistors on these I/O pins, so they may already be present on the board. In some HardCopy series device applications, you can remove these external pull-up resistors.

Altera recommends leaving external pull-up resistors on the board if one of the following conditions exists.



For more information, refer to the *Designing with 1.5-V Devices* chapter in the *Stratix Device Handbook*.

- There is more than one HardCopy series and/or FPGA on the board
- The HardCopy design uses configuration emulation
- The design uses MultiVolt I/O configurations

In the FPGA, you can enable the `INIT_DONE` pin in the Quartus II software. If you used the `INIT_DONE` pin on the FPGA prototype, the HardCopy series device retains its function.

- In HardCopy series devices, the `INIT_DONE` settings option is masked-programmed into the device. You must submit these settings to Altera with the final design prior to migrating to a HardCopy series device. The use of the `INIT_DONE` option and other option pins (for example, `DEV_CLRn` and `DEV_OE`) are available in the Fitter Device Options sections of the Quartus II report file.
- For HardCopy II and HardCopy Stratix devices, the `PORSEL` pin setting delays the `POR` sequence similar to the prototyping FPGA. For more information on `PORSEL` settings for the FPGA, refer to the *Configuration Handbook*.

In some FPGA configuration schemes, inputs `DCLK` and `DATA[7..0]` float if the configuration device is removed from the board. In the HardCopy series devices, these I/O pins are designed with weak, internal pull-up resistors, so the pins can be left unconnected on the board.

Configuration Emulation of FPGA Configuration Sequence

In configuration emulation mode, the HardCopy series device emulates the behavior of an APEX or Stratix FPGA during its configuration phase. When this mode is used, the HardCopy device uses a configuration emulation circuit to receive configuration bit streams. When all the configuration data is received, the HardCopy series device transitions into an initialization phase and releases the `CONF_DONE` pin to be pulled high. Pulling the `CONF_DONE` pin high signals that the HardCopy series device is ready for normal operation. If the optional open-drain `INIT_DONE` output is used, the normal operation is delayed until this signal is released by the HardCopy series device.



HardCopy II and some HardCopy Stratix devices do not support configuration emulation mode.

During the emulation sequence, the user I/O pins can be pulled high by internal, weak pull-up resistors. Once the configuration emulation and initialization phase is completed, the I/O pins are released. Similar to the FPGA, if the `nIO_pullup` pin is driven high, the weak pull-up resistors are disabled. The value of the internal weak pull-up resistors on the I/O pins can be found in the Operating Conditions table of the specific FPGA's device handbook.



Similar to APEX 20K FPGAs, HardCopy APEX devices do not have an `nIO_pullup` function. Their internal weak pull-up resistors are enabled during the power up and initialization phase.

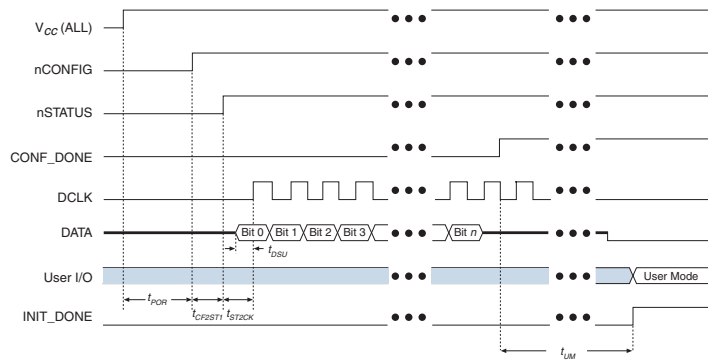


Similar to Stratix or APEX FPGAs, HardCopy Stratix or HardCopy APEX devices enter initialization phase immediately after a successful configuration sequence. At this time, registers are reset, any PLLs used are initialized, and any I/O pins used are enabled as the device transitions into user mode.

One application of the configuration emulation mode occurs when multiple programmable devices are cascaded in a configuration chain and only one device is replaced with a HardCopy series device. In this case, programming control signals and clock signals used to program the FPGA must also be used for the HardCopy series device. If this is not done, the HardCopy series device remains in the configuration emulation phase, the emulation sequence never ends, and the HardCopy `CONF_DONE` pin remains de-asserted. The proper configuration data stream and data clock is necessary so the HardCopy series device has the accurate emulation behavior.

Figure 12–4 shows a waveform of the configuration signals and the user I/O signals using configuration emulation mode.

Figure 12–4. Timing Waveform for Configuration Emulation Mode *Notes (1), (2), (3), (4), (5)*



Notes to Figures 12–4:

- (1) V_{CC} (ALL) represents either all of the power pins or the last power pin powered up to specified operating conditions. All HardCopy power pins must be powered within specifications as described under *Hot Socketing* sections.
- (2) nCONFIG, nSTATUS, and CONF_DONE must not be driven low externally for this waveform to apply.
- (3) User I/O pins may be tri-stated or driven before and during power up. See the *Hot Socketing* sections for more details. The nIO_pullup pin can affect the state of the user I/O pins during the initialization phase.
- (4) INIT_DONE is an optional pin that can be enabled on the FPGA using the Quartus II software. HardCopy devices will carry over the INIT_DONE functionality from the prototyped FPGA design.
- (5) The nCEO pin is also asserted about the same time the CONF_DONE pin is released. However, the nCE pin must be driven low externally for this waveform to apply.

Configuration Emulation Timing Parameters

Tables 12–4 and 12–5 provide the timing parameters for the configuration emulation mode.

Parameter	Description (2)	Condition	Min	Typ	Max	Units
t_{POR}	PORSEL delay	2	1	2		ms
		100	70	100		ms
t_{DSU}	Data setup time		7			ns
t_{CF2ST1}	nCONFIG high to nSTATUS				40	μ s
t_{ST2CK}	nSTATUS to DCLK		1			μ s
t_{UM}	User mode delay		6.0		28	μ s

Notes to Table 12–4:

- (1) HC1S80, HC1S60, and HC1S25 devices do not support emulation mode.
- (2) These parameters are similar to the Stratix FPGA specifications. Refer to the *Configuration Handbook* for more information.

Parameter	Description (1)	Min	Typical	Max	Units
t_{POR}	POR delay		5		μ s
t_{DSU}	Data setup time	10			ns
t_{CF2ST1}	nCONFIG high to nSTATUS			1	μ s
t_{ST2CK}	nSTATUS to DCLK	1		3	μ s
t_{UM}	User mode delay	2		8	μ s

Notes to Table 12–5:

- (1) These parameters are similar to the APEX FPGA specifications. Refer to the *Configuration Handbook* for more information.

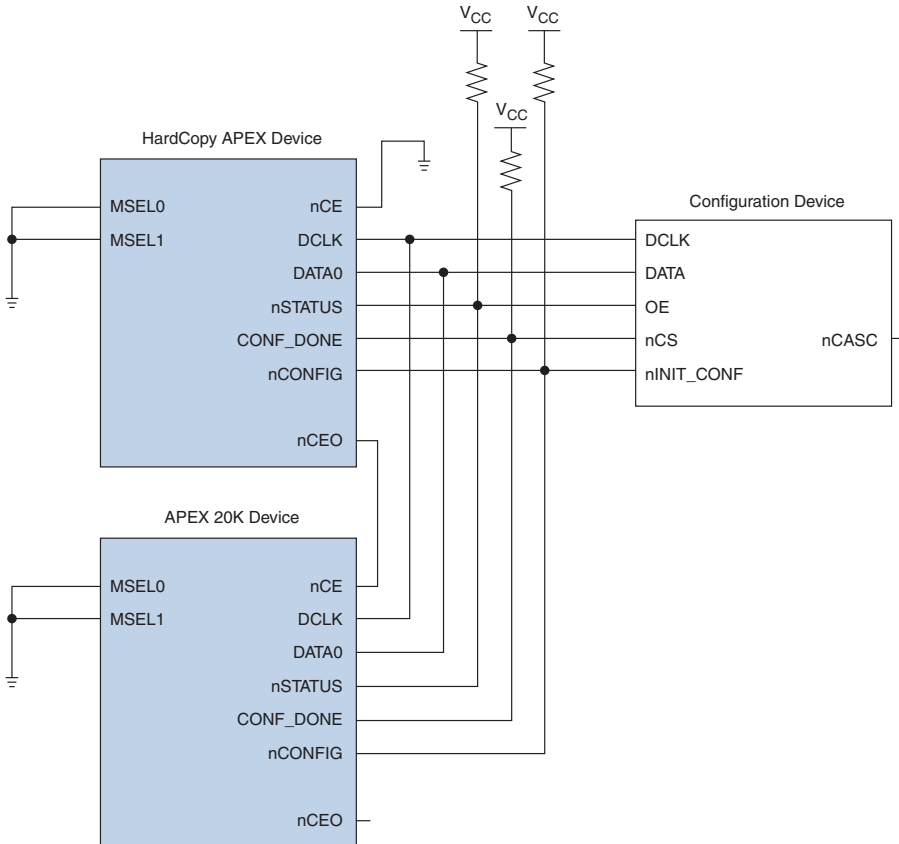
Benefits of Configuration Emulation

Configuration emulation in HardCopy series devices provides several advantages, including the following:

- Removes any necessity for changes to software, especially if the FPGA is configured using a microprocessor. Not having to change the software benefits the designer because microprocessor software changes demand significant system verification and qualification efforts, which also impact development time.
- Allows HardCopy series devices to co-exist with other FPGAs in a cascaded chain. None of the components need to be modified or added, and no design changes to the board are required. Additionally, no configuration software changes need to be made.
- Supports all configuration options available for the FPGA.

In this example, a single configuration device originally configured two APEX FPGAs. In [Figure 12-5](#), a HardCopy APEX device replaces an APEX FPGA.

Figure 12-5. Emulation of Configuration Sequence



A HardCopy series device in configuration emulation mode requires the same configuration control signals as the FPGA that was replaced. In configuration emulation mode, the HardCopy series device responds in exactly the same way as the FPGA. The CONF_DONE signal of the HardCopy series device is asserted at exactly the same time as the FPGA.

Power-Up Options Summary When Designing With HardCopy Series Devices

When designing a board for the prototyping FPGA with the intent of eventually replacing it with a HardCopy device, there are three power-up options that you should consider.

- Instant on
- Instant on after 50 ms
- Configuration emulation of an FPGA configuration sequence

You must choose the power-up option when submitting the design database to Altera for migrating to a HardCopy series device. Once the HardCopy series devices are manufactured, the power-up option cannot be changed.



HardCopy II and some HardCopy Stratix devices do not support configuration emulation mode.

HardCopy II and HardCopy Stratix devices retain the functionality of the `VCCSEL` and `PORSEL` pins from the prototyping Stratix II or Stratix FPGAs. For HardCopy II and HardCopy Stratix devices, the `PORSEL` pin setting delays the POR sequence similar to the prototyping FPGA.



For more information on `PORSEL` settings for the FPGA, refer to the *Configuration Handbook*.

The `nCE` and `nCEO` pins are functional in HardCopy series devices. The `nCE` pin must be held low for proper operation of the `nCEO` pin. If the `nCE` pin is driven low, the `nCEO` pin will be asserted after the initialization is completed and the `CONF_DONE` pin is released.

On the HardCopy II device, the `nCE` pin delays the initialization if it is not driven low. Like in the Stratix II device, `nCEO` and `TDO` of the HardCopy II device are powered by `VCCIO`.

If you used the `INIT_DONE` pin on the FPGA prototype, the HardCopy series device retains its function. In HardCopy series devices, the `INIT_DONE` settings option is masked-programmed into the device. These settings must be submitted to Altera with the final design prior to migrating to a HardCopy series device. The use of the `INIT_DONE` option and other option pins (for example, `DEV_CLRn` and `DEV_OE`) are available in the Fitter Device Options sections of the Quartus II report file.

HardCopy II devices do not support the user-supplied start-up clock option available for Stratix II devices. The HardCopy II device uses its own internal clock for power-up circuitry. The startup clock selection is an option for configuring the FPGA, which you can set in the Quartus II software under Device and Pin Options.

HardCopy devices support device-wide reset (`DEV_CLRn`) and device-wide output enable (`DEV_OE`). The HardCopy settings follow the prototyping FPGA setting, which you set in the Quartus II software under Device and Pin Options.

For correct operation of a HardCopy series device using the instant on option, pull the `nSTATUS`, `nCONFIG`, and `CONF_DONE` pins to V_{CC} . In the HardCopy series devices, these pins are designed with weak, internal resistors pulled up to V_{CC} . Many FPGA configuration schemes require pull-up resistors on these I/O pins, so they may already be present on the board. In some HardCopy series device applications, you can remove these external pullup resistors.

Altera recommends leaving external pull-up resistors on the board if one of the following conditions exists:

- There is more than one HardCopy series and/or FPGA on the board
- The HardCopy design uses configuration emulation
- The design uses MultiVolt™ I/O configurations



For more information, refer to the *Designing with 1.5-V Devices* chapter in the *Stratix Device Handbook*.

In some FPGA configuration schemes, inputs `DCLK` and `DATA[7..0]` float if the configuration device is removed from the board. In the HardCopy series devices, these I/O pins are designed with weak internal pull-up resistors, so the pins can be left unconnected on the board.

When designing a board with a Stratix II prototype device and its companion HardCopy II device, most configuration pins required by the Stratix II device are not required by the HardCopy II device. To maximize I/O pin counts with HardCopy II device utilization, Altera recommends minimizing power-up and configuration pins that do not carry over from a Stratix II device into a HardCopy II device. More information can be found on the *Migrating Stratix II Device Resources to HardCopy II Devices* chapter.

HardCopy devices support the MSEL settings used on the FPGA. You are not required to change these settings on the board when replacing the prototyping FPGA with the HardCopy series device.

HardCopy II devices do not use MSEL pins and these pin locations are not connected in the package. It is acceptable to drive these pins to V_{CC} or GND as required by the prototyping Stratix II device.

Pulsing the nCONFIG signal on an FPGA re-initializes the configuration sequence. The nCONFIG signal on a HardCopy series device also restarts the initialization sequence.

The HardCopy device JTAG pin locations match their corresponding FPGA prototypes. Like the FPGAs, the JTAG pins have internal weak pull ups or pull downs on the four input pins TMS, TCK, TDI, and TRST. There is no requirement to change the JTAG connections on the board when replacing the prototyping FPGA with the HardCopy series device. More information on JTAG pins is the corresponding *Boundary-Scan Support* chapter for each device.

Power-Up Option Selection and Examples

The HardCopy series device power-up option is mask-programmed. Therefore, it is important that the board design is verified to ensure that the HardCopy series device power-up option chosen will work properly. This section provides recommendations on selecting a power-up option and provides some examples.

Table 12–6 shows a comparison of applicable FPGA and HardCopy power up options.

Power Up Scheme	Device Family					
	Stratix II	Stratix	APEX 20K APEX 20KE APEX 20KC	HardCopy II (1)	HardCopy Stratix (2)	HardCopy APEX
Instant on				✓	✓	✓
Instant on after 50 ms				✓	✓	✓
Passive serial (PS)	✓	✓	✓		✓	✓
Active serial (AS)	✓					
Fast passive parallel (FPP)	✓	✓			✓	
Passive parallel synchronous (PPS)			✓			✓
Passive parallel asynchronous (PPA)	✓	✓	✓		✓	✓
Joint Test Action Group (JTAG)	✓	✓	✓		✓	✓
Remote local update FPP (3)	✓	✓				

Table 12–6. FPGA Configuration Modes and HardCopy Series Power-Up Schemes (Part 2 of 2)

Power Up Scheme	Device Family					
	Stratix II	Stratix	APEX 20K APEX 20KE APEX 20KC	HardCopy II (1)	HardCopy Stratix (2)	HardCopy APEX
Remote local update PPA (3)	✓	✓				
Remote local update PS (3)		✓				

Notes to Table 12–6:

- (1) HardCopy II devices do not support emulation mode.
- (2) HC1S80, HC1S60, and HC1S25 devices do not support emulation mode.
- (3) The remote/local update feature of Stratix devices is not supported in HardCopy Stratix devices.

Power-up option recommendations depend on the following board configurations:

- Single HardCopy series device replacing a single FPGA on the board
- One or more HardCopy series devices replacing one or more FPGA of a multiple-device configuration chain
- All HardCopy series devices replacing all FPGAs of a multiple-device configuration chain

In a multiple-device configuration chain, more than one FPGA on a board obtains configuration data from the same source.

Replacing One FPGA With One HardCopy Series Device

Altera recommends using the instant on or instant on after 50 ms mode when replacing an FPGA with a HardCopy series device regardless of the board configuration scheme. Table 12–7 gives a summary of HardCopy series device power-up options when a single HardCopy series device replaces a single FPGA on the board.



Table 12–7 does not include HardCopy II options because HardCopy II devices only support instant on and instant on after 50 ms modes.

Configuration Scheme	HardCopy APEX Options	HardCopy Stratix Options	Comments
PS with configuration device(s) or download cable (1)	<ul style="list-style-type: none"> ● Instant on ● Instant on after 50 ms 	<ul style="list-style-type: none"> ● Instant on ● Instant on after 50 ms 	The configuration device(s) must be removed from the board.
FPP with enhanced configuration devices	<ul style="list-style-type: none"> ● Not available 	<ul style="list-style-type: none"> ● Instant on ● Instant on after 50 ms 	The configuration device(s) must be removed from the board.
PS, PPA, PPS, FPP, with a microprocessor (2)	<ul style="list-style-type: none"> ● Emulation 	<ul style="list-style-type: none"> ● Emulation (3) 	If the microprocessor code can be changed, the design should use the instant on or instant on after 50 ms mode. However, the microprocessor still needs to drive a logic ‘1’ value on the HardCopy nCONFIG pin
JTAG configuration	<ul style="list-style-type: none"> ● Instant on after 50 ms ● Emulation 	<ul style="list-style-type: none"> ● Instant on after 50 ms ● Emulation (3) 	Configuration emulation mode can be used but delays the initialization of the board or device.

Notes to Table 12–7:

- (1) Download cable used may be either MasterBlaster™, USB Blaster, ByteBlaster™ II, or ByteBlasterMV™ hardware.
- (2) For parallel programming modes, DATA [7 . . 1] pins have weak pull up resistors on the HardCopy series device, which can be optionally enabled or disabled through metallization. DCLK and DATA [0] pins have internal weak pull-up resistors.
- (3) HC1S80, HC1S60, and HC1S25 devices do not support emulation mode.

Replacing One or More FPGAs With One or More HardCopy Series Devices in a Multiple-Device Configuration Chain

Altera recommends using the instant on or instant on after 50 ms mode when replacing an FPGA with a HardCopy series device, regardless of configuration scheme. Table 12–8 gives a summary of HardCopy series device power-up options when a single HardCopy series device replaces a single FPGA of a multiple-device configuration chain.



When using the instant on or instant on after 50 ms mode, the HardCopy series device could be in user-mode and ready before other configured devices on the board. It is important to verify that any signals that communicate to and from the HardCopy series device are stable or will not affect the HardCopy series device or other device operation while the devices are still in the power up or configuration stage. For example, if the HardCopy series design used a PLL reference clock that is not available until after other devices are fully powered up, the HardCopy series device PLL will not operate properly unless the PLLs are reset.



Table 12–8 does not include HardCopy II options because HardCopy II devices only support instant on and instant on after 50 ms modes.

Table 12–8. Power-Up Options for One or More HardCopy Series Devices Replacing FPGAs in a Multiple-Device Configuration Chain (Part 1 of 2)

Configuration Scheme	HardCopy APEX Options	HardCopy Stratix Options	Comments
PS with configuration device(s) or download cable (1) FPP with enhanced configuration device (4)	<ul style="list-style-type: none"> • Emulation • Instant on (3) • Instant on after 50 ms (3) 	<ul style="list-style-type: none"> • Emulation (2) • Instant on (3) • Instant on after 50 ms (3) 	Instant on or instant on after 50 ms modes can be used if the nCE pin of the following APEX or Stratix device can be tied to logic 0 on the board and the configuration data is modified to remove the HardCopy series device configuration data. The configuration sequence then skips the HardCopy series device.
PS, PPA, PPS, FPP, with a microprocessor (4)	<ul style="list-style-type: none"> • Emulation 	<ul style="list-style-type: none"> • Emulation (2) 	If the microprocessor code can be changed, the design should use the instant on or instant on after 50 ms mode. However, the microprocessor still needs to drive a logic '1' value on the HardCopy series device nCONFIG pin.

Table 12–8. Power-Up Options for One or More HardCopy Series Devices Replacing FPGAs in a Multiple-Device Configuration Chain (Part 2 of 2)

Configuration Scheme	HardCopy APEX Options	HardCopy Stratix Options	Comments
JTAG configuration	• Emulation	• Emulation (2)	If the HardCopy series device is put in BYPASS mode and the JTAG programming data is modified to remove the HardCopy configuration information, instant on or instant on after 50 ms modes can be used.

Notes to Table 12–8:

- (1) Download cable used may be either MasterBlaster, USB Blaster, ByteBlaster II, or ByteBlasterMV hardware.
- (2) HC1S80, HC1S60, and HC1S25 devices do not support emulation mode.
- (3) If the HardCopy series device is the last device in the configuration chain, Altera recommends using instant on modes.
- (4) For parallel programming modes, DATA [7 . . 1] pins have weak pull up resistors on the HardCopy series device, which can be optionally enabled or disabled through metallization. DCLK and DATA [0] pins also have weak pull-up resistors.

Replacing all FPGAs with HardCopy Series Devices in a Multiple-Device Configuration Chain

When all Stratix II, Stratix, and APEX FPGAs are replaced by HardCopy II, HardCopy Stratix, and HardCopy APEX devices, respectively, Altera recommends using the instant on or instant on after 50 ms mode, regardless of configuration scheme.

Once the HardCopy series devices replace the FPGAs, any configuration devices used to configure the FPGAs should be removed from the board. Microprocessor code, if applicable, should be changed to account for the HardCopy series device power-up scheme. You can use the JTAG chain to perform other JTAG operations except configuration.

FPGA to HardCopy Configuration Migration Examples

The following are examples of how HardCopy series devices replace FPGAs that use different FPGA configuration schemes.

HardCopy Series Device Replacing a Stand-Alone FPGA

In this example, the single HardCopy series device uses the instant on power-up option, as shown in Figure 12–7. The configuration device, now redundant, is removed, and no further board changes are necessary. The pull-up resistors on the nCONFIG, nSTATUS, and CONF_DONE pins can be removed, but should be left on the board if configuration emulation or multiple-voltage I/O standards are used. You could also use the instant on after 50 ms power-up mode in this example.

Figures 12-6 and 12-7 show how a HardCopy series device replaces an FPGA previously configured with an Altera configuration device.

Figure 12-6. Configuration of a Stand-Alone FPGA Note (1)

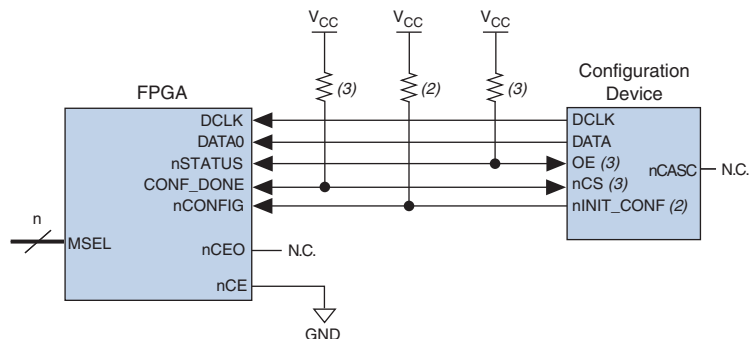
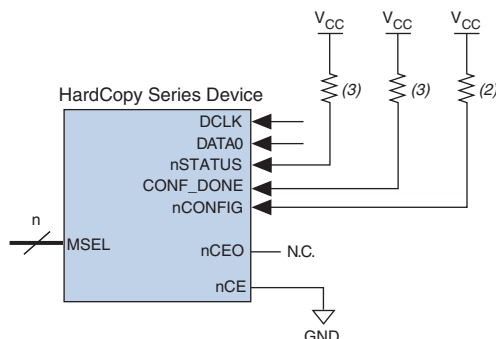


Figure 12-7. HardCopy Series Device Replacing Stand-Alone FPGA Note (1)



Notes to Figures 12-6 and 12-7:

- (1) For details on configuration interface connections, refer to the *Configuration Handbook*. The handbook includes information on MSEL pins set to PS mode.
- (2) The nINIT_CONF pin (available on enhanced configuration and EPC2 devices) has an internal pull-up resistor that is always active. Therefore, the nINIT_CONF/nCONFIG line does not require an external pull-up resistor. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used or not available, use a resistor to pull the nCONFIG pin to V_{CC}.
- (3) Enhanced configuration and EPC2 devices have internal programmable pull-up resistors on OE and nCS pins. Refer to the *Configuration Handbook* for more details of this application in FPGAs. HardCopy series devices have internal weak pull-up resistors on nSTATUS, nCONFIG, and CONF_DONE pins.

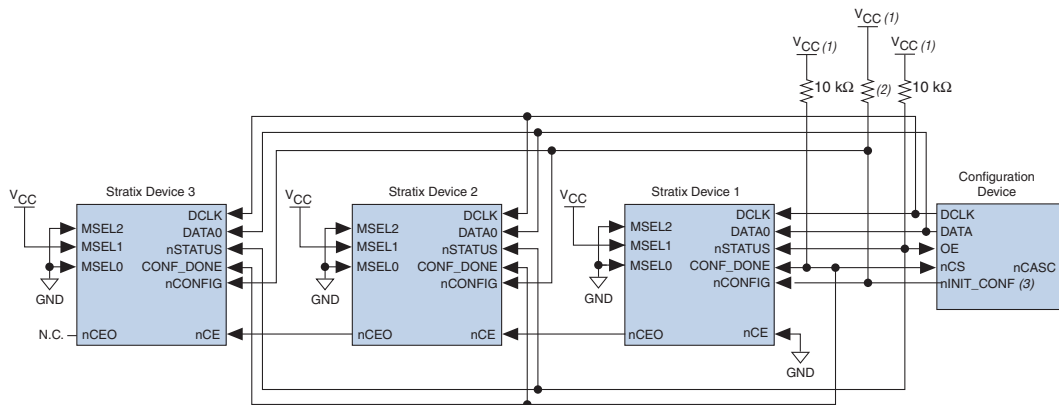
HardCopy Series Device Replacing an FPGA in a Cascaded Configuration Chain

Figure 12–8 shows a design where the configuration data for the Stratix devices is stored in a single configuration device, and the FPGAs are connected in a multiple-device configuration chain. The second device in the chain is replaced with a HardCopy Stratix device, as shown in Figure 12–9.



For more information on Stratix FPGA configuration schemes, refer to the *Configuration Handbook*.

Figure 12–8. Configuration of Multiple FPGAs in a Cascade Chain

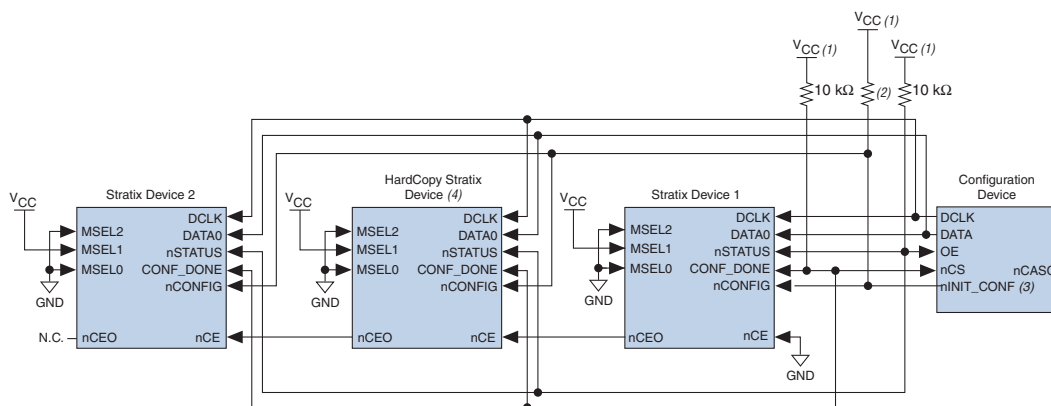


Notes to Figure 12–8:

- (1) The pull-up resistors are connected to the same supply voltage as the configuration device.
- (2) The enhanced configuration devices and EPC2 devices have internal programmable pull-up resistors on the OE and nCS pins. Refer to the *Configuration Handbook* for more details.
- (3) The nINIT_CONF pin is available on EPC16, EPC8, EPC4, and EPC2 devices. Refer to the *Configuration Handbook* for more details.

Configuration with the HardCopy Series Device in the Cascade Chain

Figure 12–9 shows the same cascade chain as Figure 12–8, but the second FPGA in the chain has been replaced with a HardCopy Stratix device.

Figure 12–9. Replacing an FPGA with a HardCopy Equivalent in the Cascade Chain**Notes to Figure 12–9:**

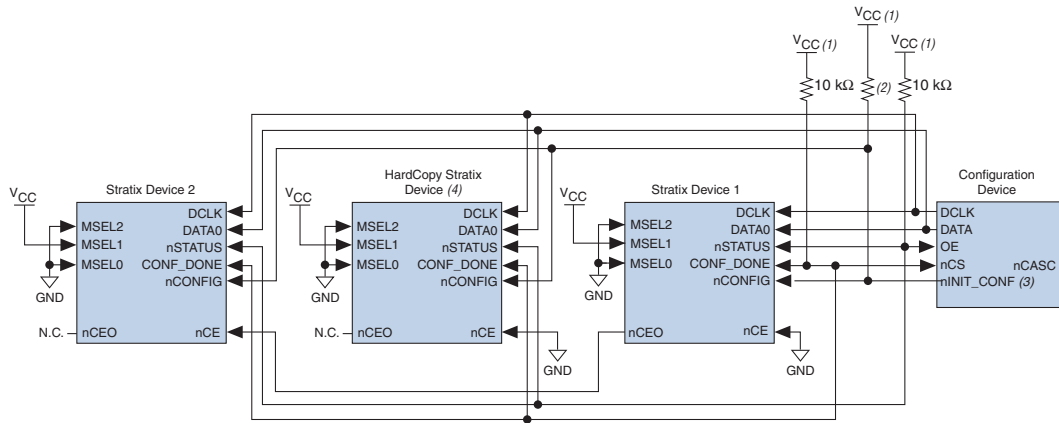
- (1) The pull-up resistors are connected to the same supply voltage as the configuration device.
- (2) The enhanced configuration devices and EPC2 devices have internal programmable pull-up resistors on the OE and nCS pins. Refer to the *Configuration Handbook* for more details.
- (3) The nINIT_CONF pin is available on EPC16, EPC8, EPC4, and EPC2 devices. Refer to the *Configuration Handbook* for more information.
- (4) HC1S80, HC1S60, and HC1S25 devices do not support emulation mode and cannot be used in this method.

In this example, the HardCopy Stratix device can only be configured using the configuration emulation mode. The configuration device cannot be removed, as it is still required by other Stratix devices in the chain. While the HardCopy Stratix device does not need the data stored in the configuration device, the data in the configuration device is not modified to reflect this. The emulation mode ensures that the HardCopy series device nCEO pin is asserted correctly after the emulation of the configuration sequence. The nCEO pin enables the next device in the chain to receive the correct configuration data from the configuration device. Additionally, with the configuration emulation mode, you do not need to make any changes to the board.

Configuration With the HardCopy Series Device Removed From the Cascade Chain

An alternative method to configure FPGAs on a board with both HardCopy series devices and FPGAs is to remove the HardCopy series device from the cascade chain. Figure 12–10 shows how the devices are connected with the HardCopy series device removed from the chain.

The data in the configuration device should be modified to exclude the HardCopy series device configuration options. The HardCopy series device can use any of the three power-up options.

Figure 12–10. Configuration With the HardCopy Series Device Removed From the Cascade Chain**Notes to Figure 12–10:**

- (1) The pull-up resistors are connected to the same supply voltage as the configuration device.
- (2) The enhanced configuration devices and EPC2 devices have internal programmable pull-up resistors on the OE and nCS pins. Refer to the *Configuration Handbook* for more details.
- (3) The nINIT_CONF pin is available on EPC16, EPC8, EPC4, and EPC2 devices. Refer to the *Configuration Handbook* for more information.
- (4) HC1S80, HC1S60, and HC1S25 devices do not support emulation mode and cannot be used in this method.

Eliminating the HardCopy series device from the configuration chain requires the following changes on the board:

- The nCE pin of the HardCopy series device must be tied to GND.
- The nCE pin of the FPGA that was driven by the HardCopy series nCEO pin must now be driven by the nCEO pin of the FPGA that precedes the HardCopy series device in the chain.

HardCopy Series Device Replacing an FPGA Configured Using a Microprocessor

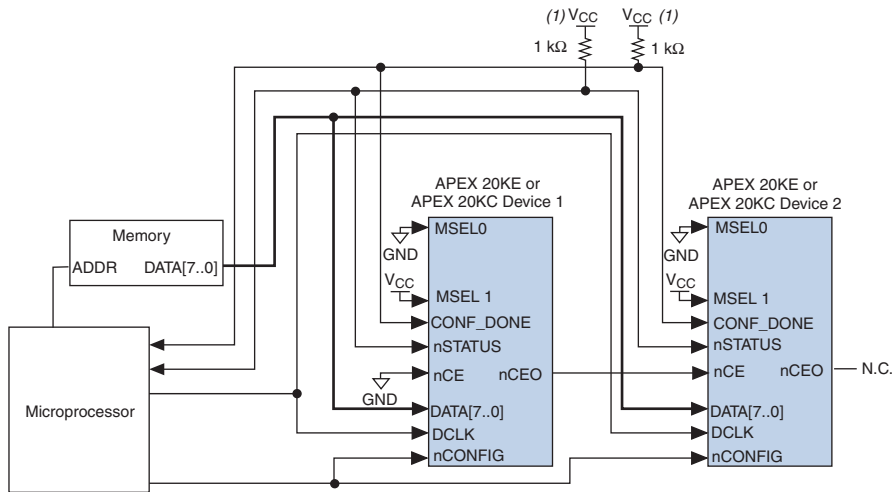
The HardCopy series device can replace FPGAs that are configured using a microprocessor, as shown in [Figures 12–12](#) and [12–13](#). While the instant on mode is the most efficient, designers can also use the instant on after 50 ms and configuration emulation mode.

[Figure 12–11](#) shows an application where APEX FPGAs are configured using a microprocessor in the PPS configuration scheme.



For more information on the PPS configuration scheme, refer to the *Configuration Handbook*.

Figure 12–11. Configuring FPGAs Using a Microprocessor



Note to Figure 12–11:

(1) Connect the pull-up resistors to a supply that provides an acceptable input signal for all devices in the chain.

When the HardCopy series device replaces the last FPGA of the configuration sequence (as shown in Figure 12–12), use the instant on or instant on after 50 ms mode. However, you must modify the microprocessor code to eliminate the configuration data for the last FPGA of the configuration chain.

Figures 12-12 and 12-13 show the HardCopy APEX device replacing APEX FPGAs either first or last in the configuration chain.

Figure 12-12. Replacement of Last FPGA in the Chain With a HardCopy Series Device

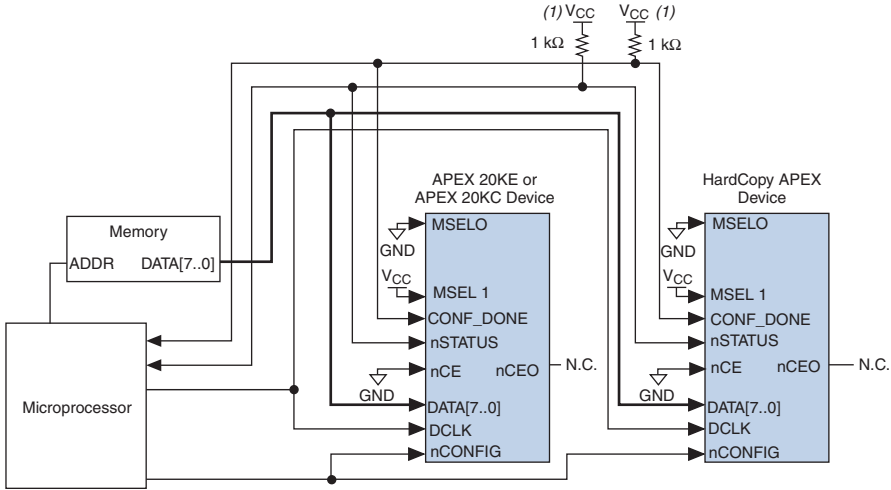
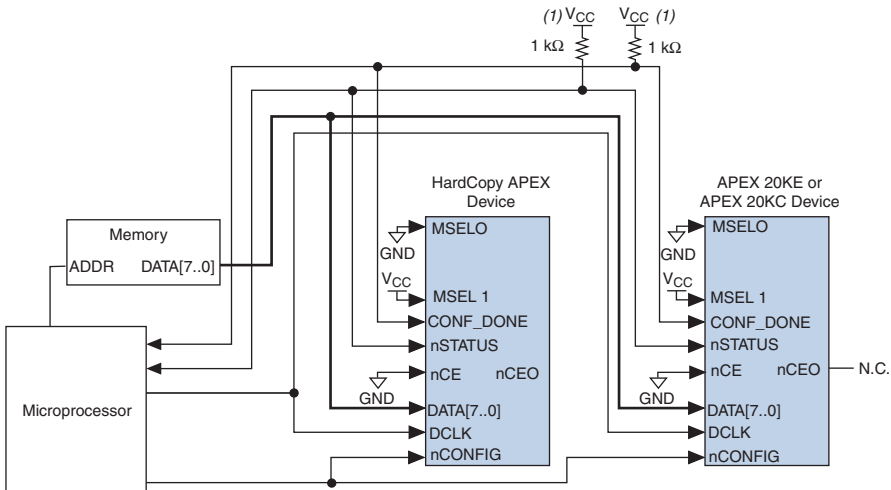


Figure 12-13. Replacement of First FPGA in the Chain With a HardCopy Series Device



Note to Figures 12-12 and 12-13:

- (1) Connect the pull-up resistors to a supply that provides an acceptable input signal for all devices in the chain.

If the HardCopy series device is the first device in the chain as opposed to the second (as shown in [Figure 12–13](#)), you must take the following into consideration, depending on the HardCopy power-up option used.

- Instant on mode—The microprocessor program code must be modified to remove the configuration code relevant to the HardCopy series device. The microprocessor must delay sending the first configuration data word to the FPGA until the `nCEO` pin on the HardCopy series device is asserted. The microprocessor then loads the first configuration data word into the FPGA.
- Instant on after 50 ms mode—The boot-up time of the microprocessor must be greater than 50 ms. The HardCopy series device asserts the `nCEO` pin after the 50-ms delay which, in turn, enables the following FPGA. The microprocessor can send the first configuration data word to the FPGA after the FPGA is enabled.
- Emulation mode—This option should be used if the microprocessor code pertaining to the configuration of the above devices cannot be modified.

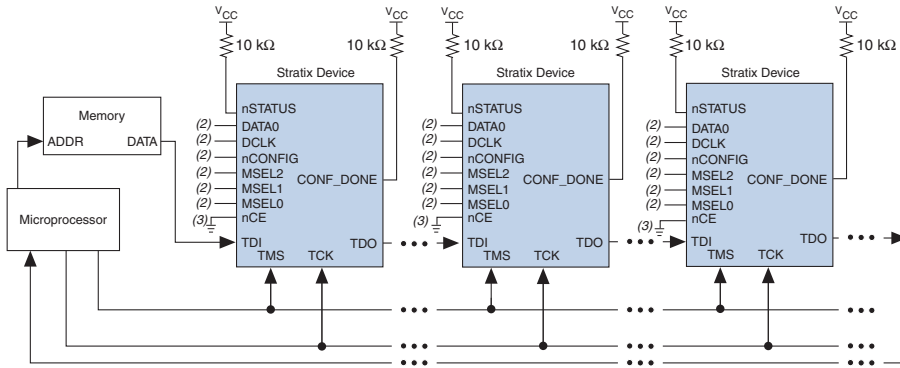
HardCopy Stratix Device Replacing FPGA Configured in a JTAG Chain

In this example, the circuit connectivity is maintained and there are no changes made to the board. The HardCopy series device can use either of the following power-up options when applicable.

- Instant on mode—Use the instant on power up mode if the microprocessor code can be modified so that it treats the HardCopy series device as a non-configurable device. The microprocessor can achieve this by issuing a `BYPASS` instruction to the HardCopy series device. With the HardCopy series device in `BYPASS` mode, the configuration data passes through it to the downstream FPGAs.
- Configuration emulation mode—Use the configuration emulation power up mode if the microprocessor code pertaining to the configuration of the above devices cannot be modified. HC1S80, HC1S60, and HC1S25 devices do not support this mode.

Figure 12–14 shows an example where there are multiple Stratix FPGAs. These devices are connected using the JTAG I/O pins for each device, and programmed using the JTAG port. An on-board microprocessor generates the configuration data.

Figure 12–14. Configuring FPGAs in a JTAG Chain Using a Microprocessor *Note (1)*

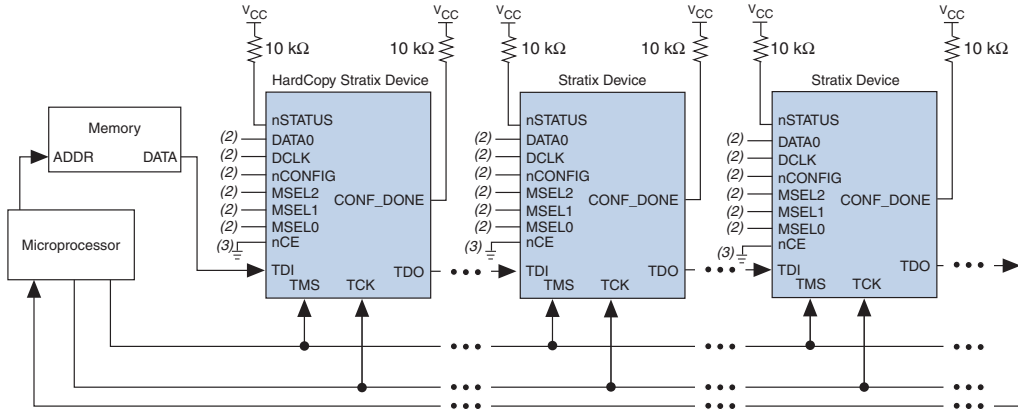


Notes to Figure 12–14:

- (1) Stratix II, Stratix, and APEX 20K devices can be placed within the same JTAG chain for device programming and configuration.
- (2) Connect the nCONFIG, MSEL0, MSEL1, and MSEL2 pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect nCONFIG to V_{CC}, and MSEL0, MSEL1, and MSEL2 to ground. Pull DATA0 and DCLK to either high or low.
- (3) nCE must be connected to GND or driven low for successful JTAG configuration.

Figure 12–15 shows an example where the first Stratix device in the JTAG chain is replaced by a HardCopy Stratix device.

Figure 12–15. Replacement of the First FPGA in the JTAG Chain With a HardCopy Series Device Note (1)



Notes to Figure 12–15:

- (1) Stratix II, Stratix, and APEX 20K devices can be placed within the same JTAG chain for device programming and configuration.
- (2) Connect the nCONFIG, MSEL0, MSEL1, and MSEL2 pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect nCONFIG to V_{CC}, and MSEL0, MSEL1, and MSEL2 to ground. Pull DATA0 and DCLK to either high or low.
- (3) nCE must be connected to GND or driven low for successful JTAG configuration.

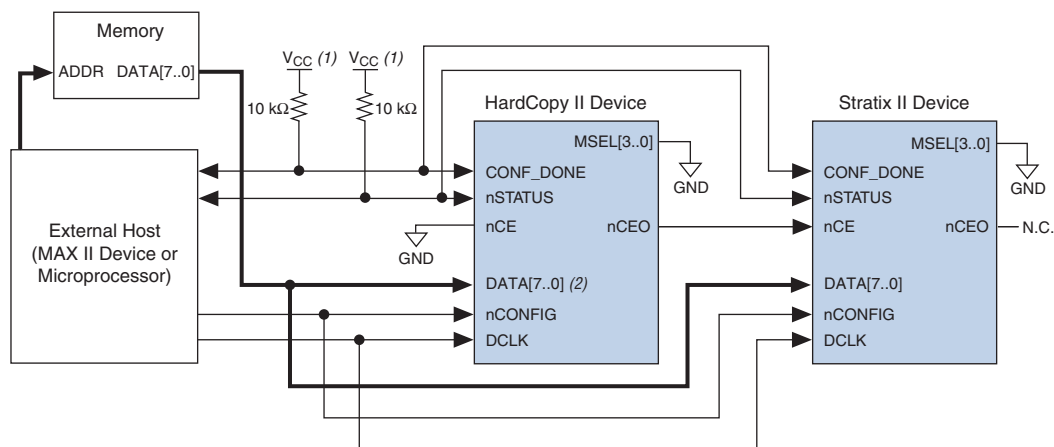
HardCopy II Device Replacing Stratix II Device Configured With a Microprocessor

When replacing a Stratix II FPGA with a HardCopy II device, the HardCopy II device can only use the instant on and instant on after 50 ms modes. This example does not require any changes to the board. However, the microprocessor code must be modified to treat the HardCopy II device as a non-configurable device.

Figure 12–16 shows an example with two Stratix II devices configured using a microprocessor or MAX® II device and the FPP configuration scheme.



For more information on Stratix II configuration, refer to the *Configuration Handbook*.

Figure 12–17. Replacement of the First FPGA in the FPP Configuration Chain With a HardCopy Series Device**Notes to Figure 12–17:**

- (1) Connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. The V_{CC} voltage meets the I/O standard's V_{IH} specification on the device and the external host.
- (2) The $DATA[7..0]$ pins are not used on the HardCopy II device, but they preserve the pin assignment and direction from the Stratix II device, allowing drop-in replacement.

Conclusion

HardCopy series devices can emulate a configuration sequence while maintaining the seamless migration benefits of the HardCopy methodology. Instant on mode, which is the simplest of the available options, provides ASIC-like operation at power on. This mode can be used in most cases without regard to the original FPGA configuration mode and without any hardware and/or software changes.

In some cases, however, a software revision and/or a board re-design may be necessary to guarantee that correct configuration data is sent to the remaining programmable devices. Such modifications are easily made in the early stages of the board design process if it is determined that one or more of the FPGAs will be replaced with an equivalent HardCopy series device. Board-design techniques like jumper connectors and 0- Ω resistors enable such modifications without the necessity to re-design the board.

The instant on after 50 ms mode is suitable in cases where a delay is necessary to accommodate the configuration device to become operational, or to allow one or more pre-determined events to be completed before the HardCopy series device asserts its `CONF_DONE` pin.

Finally, the emulation mode is the option to choose if software or hardware modifications are not possible. In such cases, the HardCopy series device co-exists with other FPGAs.

Document Revision History

Table 12–9 shows the revision history for this chapter.

<i>Table 12–9. Document Revision History (Part 1 of 2)</i>		
Date and Document Version	Changes Made	Summary of Changes
September 2008, v2.5	Updated chapter number and metadata.	—
June 2007, v2.4	Minor text edits.	—
December 2006 v2.3	Added revision history.	—
May 2006, v2.2	<ul style="list-style-type: none"> ● Updated Tables 20-1, 20-3, and 2-5. 	—
March 2006, v2.1	<ul style="list-style-type: none"> ● Formerly chapter 16. ● Re-organized <i>HardCopy Power-Up Options</i> section to eliminate redundancy. ● Updated Figures 20-1, 20-2, and 20-3. ● Updated Tables 20-1 to 20-5, and Table 20-7. ● Added <i>Power Up Options Summary When Designing With HardCopy Series Devices</i> section. 	—
October 2005, v2.0	Moved from Chapter 15 to Chapter 16 in Hardcopy Series Device Handbook 3.2	—

Table 12–9. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
January 2005, v2.0	<ul style="list-style-type: none"> ● Chapter title changed to <i>Power-Up Modes and Configuration Emulation in HardCopy Series Devices</i>. ● Added HardCopy II device information. ● Updated external resistor requirements depending on chip configuration. ● Added reference to some control and option pins that carry over functions from the FPGA design and affect the HardCopy power up. ● Updated information on which HardCopy devices do not support emulation mode. ● Added Table 15–9 which lists what power up options are supported by FPGAs and their HardCopy counterpart. ● Added “Replacing One FPGA With One HardCopy Series Device”, “Replacing One or More FPGAs With One or More HardCopy Series Devices in a Multiple-Device Configuration Chain”, and “Replacing all FPGAs with HardCopy Series Devices in a Multiple-Device Configuration Chain” sections, including Tables 15-10 and 15-11, highlighting power up recommendations for each HardCopy series family. 	—
June 2003, v1.0	Initial release of Chapter 15, Power-Up Modes and Configuration Emulation in HardCopy Series Devices.	—