

Introduction

System designers must consider the recommended DC and switching conditions discussed in this chapter to maintain the highest possible performance and reliability of the MAX[®] II devices. This chapter contains the following sections:

- “Operating Conditions” on page 5–1
- “Power Consumption” on page 5–8
- “Timing Model and Specifications” on page 5–8

Operating Conditions

Table 5–1 through Table 5–12 provide information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for MAX II devices.

Absolute Maximum Ratings

Table 5–1 shows the absolute maximum ratings for the MAX II device family.

Table 5–1. MAX II Device Absolute Maximum Ratings (Note 1), (2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Internal supply voltage (3)	With respect to ground	–0.5	4.6	V
V_{CCIO}	I/O supply voltage	—	–0.5	4.6	V
V_I	DC input voltage	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin (4)	—	–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias (5)	–65	135	°C
T_J	Junction temperature	TQFP and BGA packages under bias	—	135	°C

Notes to Table 5–1:

- (1) Refer to the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
- (3) Maximum V_{CCINT} for MAX II devices is 4.6 V. For MAX IIG and MAX IIZ devices, it is 2.4 V.
- (4) Refer to *AN 286: Implementing LED Drivers in MAX & MAX II Devices* for more information about the maximum source and sink current for MAX II devices.
- (5) Refer to Table 5–2 for information about “under bias” conditions.

Recommended Operating Conditions

Table 5-2 shows the MAX II device family recommended operating conditions.

Table 5-2. MAX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} (1)	3.3-V supply voltage for internal logic and ISP	MAX II devices	3.00	3.60	V
	2.5-V supply voltage for internal logic and ISP	MAX II devices	2.375	2.625	V
	1.8-V supply voltage for internal logic and ISP	MAX IIG and MAX IIZ devices	1.71	1.89	V
V_{CCIO} (1)	Supply voltage for I/O buffers, 3.3-V operation	—	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	—	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	—	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	—	1.425	1.575	V
V_I	Input voltage	(2), (3), (4)	-0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial range (5)	0	85	°C
		Industrial range	-40	100	°C
		Extended range (6)	-40	125	°C

Notes to Table 5-2:

- (1) MAX II device in-system programming and/or user flash memory (UFM) programming via JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, users are recommended to read back UFM contents and verify against the intended write data).
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) During transitions, the inputs may overshoot to the voltages shown in the following table based upon input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%
- (4) All pins, including clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (5) MAX IIZ devices are only available in the commercial temperature range.
- (6) For the extended temperature range of 100 to 125° C, MAX II UFM programming (erase/write) is only supported via the JTAG interface. UFM programming via the logic array interface is not guaranteed in this range.

Programming/Erasure Specifications

Table 5-3 shows the MAX II device family programming/erasure specifications.

Table 5-3. MAX II Device Programming/Erasure Specifications

Parameter	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	—	—	100 (1)	Cycles

Note to Table 5-3:

(1) This specification applies to the UFM and configuration flash memory (CFM) blocks.

DC Electrical Characteristics

Table 5-4 shows the MAX II device family DC electrical characteristics.

Table 5-4. MAX II Device DC Electrical Characteristics (Note 1) (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO,max}$ to 0 V (2)	-10	—	10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO,max}$ to 0 V (2)	-10	—	10	μA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) (3)	MAX II devices	—	12	—	mA
		MAX IIG devices	—	2	—	mA
		EPM240Z	—	29	150	μA
		EPM570Z	—	32	210	μA
$V_{SCHMITT}$ (4)	Hysteresis for Schmitt trigger input (5)	$V_{CCIO} = 3.3$ V	—	400	—	mV
		$V_{CCIO} = 2.5$ V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up (6)	MAX II devices	—	55	—	mA
		MAX IIG and MAX IIZ devices	—	40	—	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and in-system programming	$V_{CCIO} = 3.3$ V (7)	5	—	25	k Ω
		$V_{CCIO} = 2.5$ V (7)	10	—	40	k Ω
		$V_{CCIO} = 1.8$ V (7)	25	—	60	k Ω
		$V_{CCIO} = 1.5$ V (7)	45	—	95	k Ω

Table 5-4. MAX II Device DC Electrical Characteristics (Note 1) (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	μA
$C_{I/O}$	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

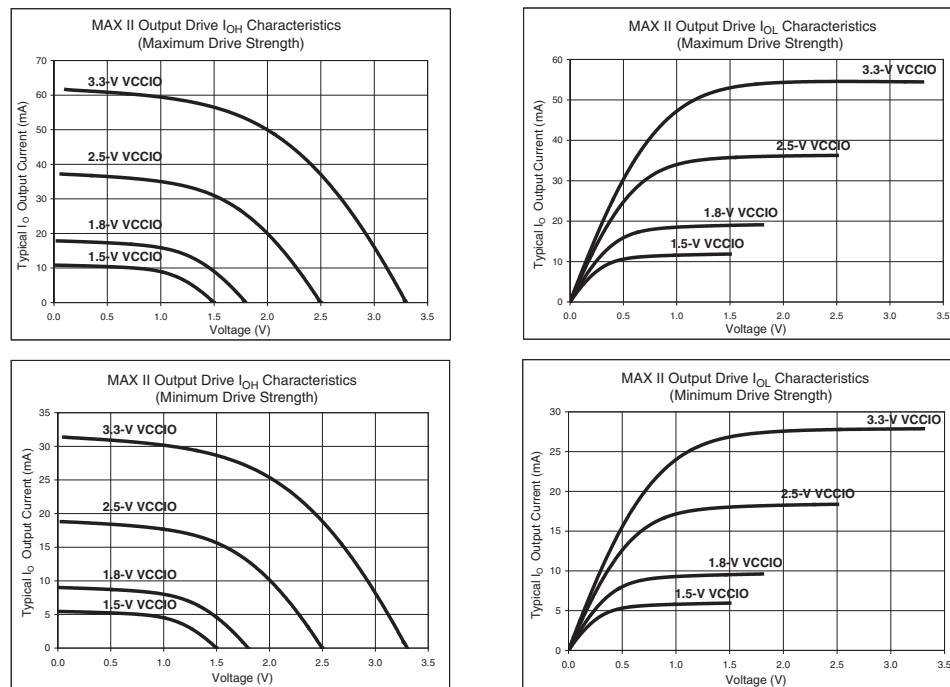
Notes to Table 5-4:

- (1) Typical values are for $T_A = 25\text{ }^\circ\text{C}$, $V_{CCINT} = 3.3$ or 2.5 V , and $V_{CCIO} = 1.5\text{ V}$, 1.8 V , 2.5 V , or 3.3 V .
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3 , 2.5 , 1.8 , and 1.5 V).
- (3) $V_i = \text{ground}$, no load, no toggling inputs.
- (4) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for $V_{CCIO} = 3.3\text{ V}$ and 120 mV for $V_{CCIO} = 2.5\text{ V}$.
- (5) The \overline{TCCK} input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.
- (6) This is a peak current value with a maximum duration of t_{CONFIG} time.
- (7) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO} .

Output Drive Characteristics

Figure 5-1 shows the typical drive strength characteristics of MAX II devices.

Figure 5-1. Output Drive Characteristics of MAX II Devices



Note to Figure 5-1:

- (1) The DC output current per pin is subject to the absolute maximum rating of Table 5-1.

I/O Standard Specifications

Table 5-5 through Table 5-10 show the MAX II device family I/O standard specifications.

Table 5-5. 3.3-V LVTTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	I/O supply voltage	—	3.0	3.6	V
V _{IH}	High-level input voltage	—	1.7	4.0	V
V _{IL}	Low-level input voltage	—	-0.5	0.8	V
V _{OH}	High-level output voltage	I _{OH} = -4 mA (1)	2.4	—	V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA (1)	—	0.45	V

Table 5-6. 3.3-V LVCMOS Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	I/O supply voltage	—	3.0	3.6	V
V _{IH}	High-level input voltage	—	1.7	4.0	V
V _{IL}	Low-level input voltage	—	-0.5	0.8	V

Table 5-6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0$, $I_{OH} = -0.1 \text{ mA}$ (1)	$V_{CCIO} - 0.2$	—	V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0$, $I_{OL} = 0.1 \text{ mA}$ (1)	—	0.2	V

Table 5-7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	-0.5	0.7	V
V_{OH}	High-level output voltage	$I_{OH} = -0.1 \text{ mA}$ (1)	2.1	—	V
		$I_{OH} = -1 \text{ mA}$ (1)	2.0	—	V
		$I_{OH} = -2 \text{ mA}$ (1)	1.7	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 0.1 \text{ mA}$ (1)	—	0.2	V
		$I_{OL} = 1 \text{ mA}$ (1)	—	0.4	V
		$I_{OL} = 2 \text{ mA}$ (1)	—	0.7	V

Table 5-8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	$0.65 \times V_{CCIO}$	2.25 (2)	V
V_{IL}	Low-level input voltage	—	-0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}$ (1)	$V_{CCIO} - 0.45$	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}$ (1)	—	0.45	V

Table 5-9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$ (2)	V
V_{IL}	Low-level input voltage	—	-0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}$ (1)	$0.75 \times V_{CCIO}$	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}$ (1)	—	$0.25 \times V_{CCIO}$	V

Notes to Table 5-5 through Table 5-9:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX II Architecture* chapter (*I/O Structure* section) in the *MAX II Device Handbook*.
- (2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 5-2.

Table 5-10. 3.3-V PCI Specifications (Note 1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	$0.5 \times V_{CCIO}$	—	$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage	—	-0.5	—	$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -500 \mu\text{A}$	$0.9 \times V_{CCIO}$	—	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 1.5 \text{ mA}$	—	—	$0.1 \times V_{CCIO}$	V

Note to Table 5-10:

(1) 3.3-V PCI I/O standard is only supported in Bank 3 of the EPM1270 and EPM2210 devices.

Bus Hold Specifications

Table 5-11 shows the MAX II device family bus hold specifications.

Table 5-11. Bus Hold Specifications

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	20	—	30	—	50	—	70	—	μA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	-20	—	-30	—	-50	—	-70	—	μA
Low overdrive current	$0 \text{ V} < V_{IN} < V_{CCIO}$	—	160	—	200	—	300	—	500	μA
High overdrive current	$0 \text{ V} < V_{IN} < V_{CCIO}$	—	-160	—	-200	—	-300	—	-500	μA

Power-Up Timing

Table 5–12 shows the power-up timing characteristics for MAX II devices.

Table 5–12. MAX II Power-Up Timing


Symbol	Parameter	Device	Min	Typ	Max	Unit
t_{CONFIG} (1)	The amount of time from when minimum V_{CCINT} is reached until the device enters user mode (2)	EPM240	—	—	200	μs
		EPM570	—	—	300	μs
		EPM1270	—	—	300	μs
		EPM2210	—	—	450	μs

Notes to Table 5–12:

- (1) Table 5–12 values apply to commercial and industrial range devices. For extended temperature range devices, the t_{CONFIG} maximum values are as follows:
- | Device | Maximum |
|---------|-------------------|
| EPM240 | 300 μs |
| EPM570 | 400 μs |
| EPM1270 | 400 μs |
| EPM2210 | 500 μs |
- (2) For more information about POR trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

Power Consumption

Designers can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

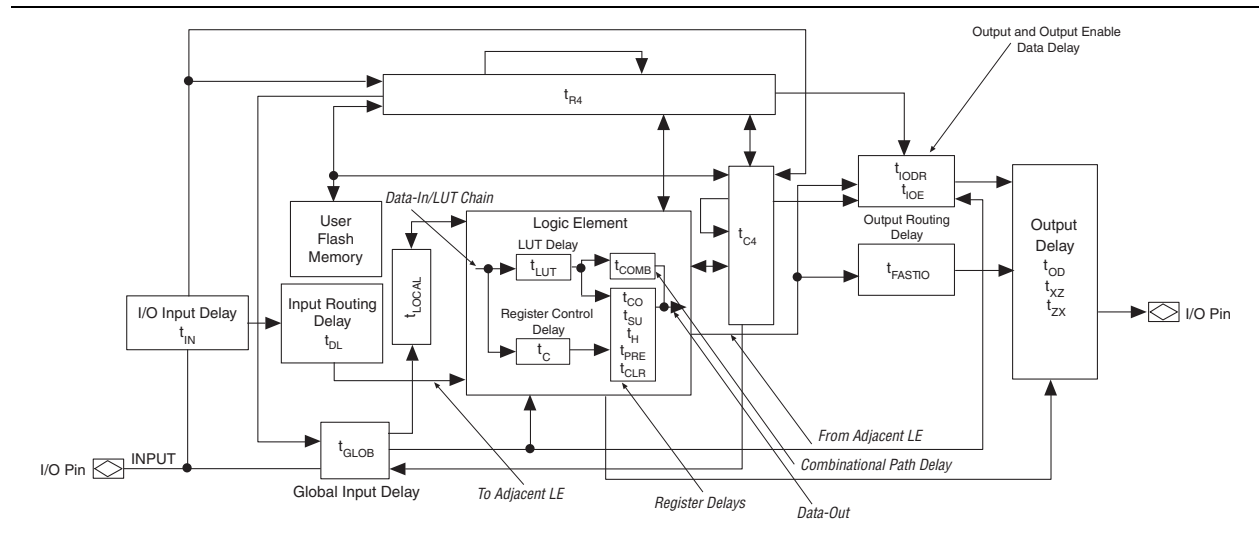
 For more information about these power analysis tools, refer to the *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Timing Model and Specifications

MAX II devices timing can be analyzed with the Altera Quartus® II software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5–2.

MAX II devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 5-2. MAX II Device Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters.

Refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook* for more information.

This section describes and specifies the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 5-13 shows the status of the MAX II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

Table 5-13. MAX II Device Timing Model Status

Device	Preliminary	Final
EPM240	—	✓
EPM240Z (1)	✓	—
EPM570	—	✓
EPM570Z (1)	✓	—

Table 5-13. MAX II Device Timing Model Status

Device	Preliminary	Final
EPM1270	—	✓
EPM2210	—	✓

Note to Table 5-13:

- (1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5-14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for -3, -4, and -5 speed grades are based on an EPM1270 device target while -6 and -7 speed grades are based on an EPM570Z device target.

Table 5-14. MAX II Device Performance

Resource Used	Design Size and Function	Resources Used			Performance					Unit
		Mode	LEs	UFM Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	
LE	16-bit counter (1)	—	16	0	304.0	247.5	201.1	184.1	123.5	MHz
	64-bit counter (1)	—	64	0	201.5	154.8	125.8	83.2	83.2	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	ns
	32-to-1 multiplexer	—	24	0	7.1	9.0	11.4	12.5	22.8	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	ns
	16-bit decoder with single address line	—	5	0	5.2	6.6	8.2	9.2	15.0	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI (2)	37	1	8.0	8.0	8.0	9.7	9.7	MHz
	512 × 8	Parallel (3)	73	1	(4)	(4)	(4)	(4)	(4)	MHz
	512 × 16	I ² C (3)	142	1	100 (5)	100 (5)	100 (5)	100 (5)	100 (5)	kHz

Notes to Table 5-14:

- (1) This design is a binary loadable up counter.
 (2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.
 (3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
 (4) This design is asynchronous.
 (5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 5-15 through Table 5-22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM structures, and MultiTrack interconnects. The timing values for -3, -4, and -5 speed grades shown in Table 5-15 through Table 5-22 are based on an EPM1270 device target, while -6 and -7 speed grade values are based on an EPM570Z device target.


 For more explanations and descriptions about each internal timing microparameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5-15. LE Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}	LE combinational LUT delay	—	571	—	742	—	914	—	1,215	—	2,247	ps
t_{COMB}	Combinational path delay	—	147	—	192	—	236	—	243	—	305	ps
t_{CLR}	LE register clear delay	238	—	309	—	381	—	401	—	541	—	ps
t_{PRE}	LE register preset delay	238	—	309	—	381	—	401	—	541	—	ps
t_{SU}	LE register setup time before clock	208	—	271	—	333	—	260	—	319	—	ps
t_H	LE register hold time after clock	0	—	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	235	—	305	—	376	—	380	—	489	ps
t_{CLKHL}	Minimum clock high or low time	166	—	216	—	266	—	253	—	335	—	ps
t_c	Register control delay	—	857	—	1,114	—	1,372	—	1,356	—	1,722	ps

Table 5-16. IOE Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	159	—	207	—	254	—	170	—	348	ps
t_{IN}	I/O input pad and buffer delay	—	708	—	920	—	1,132	—	907	—	970	ps
$t_{GLOB} (1)$	I/O input pad and buffer delay used as global signal pin	—	1,519	—	1,974	—	2,430	—	2,261	—	2,670	ps
t_{IOE}	Internally generated output enable delay	—	354	—	374	—	460	—	530	—	966	ps
t_{DL}	Input routing delay	—	224	—	291	—	358	—	318	—	410	ps
$t_{OD} (2)$	Output delay buffer and pad delay	—	1,064	—	1,383	—	1,702	—	1,319	—	1,526	ps

Table 5-16. IOE Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{zZ} (3)	Output buffer disable delay	—	756	—	982	—	1,209	—	1,045	—	1,264	ps
t_{zX} (4)	Output buffer enable delay	—	1,003	—	1,303	—	1,604	—	1,160	—	1,325	ps

Notes to Table 5-16:

- (1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB} , shown in Table 5-16, are based on an EPM240 device target.
- (2) Refer to Table 5-29 and 5-21 for delay adders associated with different I/O standards, drive strengths, and slew rates.
- (3) Refer to Table 5-19 and 5-13 for t_{zZ} delay adders associated with different I/O standards, drive strengths, and slew rates.
- (4) Refer to Table 5-17 and 5-12 for t_{zX} delay adders associated with different I/O standards, drive strengths, and slew rates.

Table 5-17 through Table 5-20 show the adder delays for t_{zX} and t_{zZ} microparameters when using an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength.

Table 5-17. t_{zX} IOE Microparameter Adders for Fast Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	28	—	37	—	45	—	72	—	71	ps
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	28	—	37	—	45	—	72	—	71	ps
2.5-V LVTTTL	14 mA	—	14	—	19	—	23	—	75	—	87	ps
	7 mA	—	314	—	409	—	503	—	162	—	174	ps
1.8-V LVTTTL	6 mA	—	450	—	585	—	720	—	279	—	289	ps
	3 mA	—	1,443	—	1,876	—	2,309	—	499	—	508	ps
1.5-V LVTTTL	4 mA	—	1,118	—	1,454	—	1,789	—	580	—	588	ps
	2 mA	—	2,410	—	3,133	—	3,856	—	915	—	923	ps
3.3-V PCI	20 mA	—	19	—	25	—	31	—	72	—	71	ps

Table 5-18. t_{zX} IOE Microparameter Adders for Slow Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	ps
	4 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	ps
3.3-V LVTTTL	16 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	ps
	8 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	ps

Table 5-18. t_{ZX} IOE Microparameter Adders for Slow Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
2.5-V LVTTTL	14 mA	—	10,412	—	10,112	—	9,811	—	9,110	—	9,105	ps
	7 mA	—	13,613	—	13,313	—	13,012	—	9,830	—	9,835	ps
3.3-V PCI	20 mA	—	-75	—	-97	—	-120	—	6,534	—	6,533	ps

Table 5-19. t_{XZ} IOE Microparameter Adders for Fast Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	-56	—	-72	—	-89	—	-69	—	-69	ps
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	-56	—	-72	—	-89	—	-69	—	-69	ps
2.5-V LVTTTL	14 mA	—	-3	—	-4	—	-5	—	-7	—	-11	ps
	7 mA	—	-47	—	-61	—	-75	—	-66	—	-70	ps
1.8-V LVTTTL	6 mA	—	119	—	155	—	191	—	45	—	34	ps
	3 mA	—	207	—	269	—	331	—	34	—	22	ps
1.5-V LVTTTL	4 mA	—	606	—	788	—	970	—	166	—	154	ps
	2 mA	—	673	—	875	—	1,077	—	190	—	177	ps
3.3-V PCI	20 mA	—	71	—	93	—	114	—	-69	—	-69	ps

Table 5-20. t_{XZ} IOE Microparameter Adders for Slow Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA	—	206	—	-20	—	-247	—	1,433	—	1,446	ps
	4 mA	—	891	—	665	—	438	—	1,332	—	1,345	ps
3.3-V LVTTTL	16 mA	—	206	—	-20	—	-247	—	1,433	—	1,446	ps
	8 mA	—	891	—	665	—	438	—	1,332	—	1,345	ps
2.5-V LVTTTL	14 mA	—	222	—	-4	—	-231	—	213	—	208	ps
	7 mA	—	943	—	717	—	490	—	166	—	161	ps
3.3-V PCI	20 mA	—	161	—	210	—	258	—	1,332	—	1,345	ps

 The default slew rate setting for MAX II device in the Quartus® II design software is “fast”.

Table 5-21. UFM Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACLK}	Address register clock period	100	—	100	—	100	—	100	—	100	—	ns
t_{ASU}	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{AH}	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{ADS}	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{ADH}	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{DCLK}	Data register clock period	100	—	100	—	100	—	100	—	100	—	ns
t_{DSS}	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	60	—	ns
t_{DSH}	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{DDS}	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{DDH}	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	20	—	ns
t_{DP}	Program signal to data clock hold time	0	—	0	—	0	—	0	—	0	—	ns
t_{PB}	Maximum delay between program rising edge to UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	ns
t_{BP}	Minimum delay allowed from UFM busy signal going low to program signal going low	20	—	20	—	20	—	20	—	20	—	ns
t_{PPMX}	Maximum length of busy pulse during a program	—	100	—	100	—	100	—	100	—	100	μ s
t_{AE}	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	0	—	ns
t_{EB}	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	ns
t_{BE}	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	20	—	ns
t_{EPMX}	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	—	500	ms
t_{DCO}	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	—	5	ns

Table 5-21. UFM Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OE}	Delay from data register clock to data register output	180	—	180	—	180	—	180	—	180	—	ns
t_{RA}	Maximum read access time	—	65	—	65	—	65	—	65	—	65	ns
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	250	—	ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	250	—	ns

Figure 5-3 through Figure 5-5 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5-21.

Figure 5-3. UFM Read Waveforms

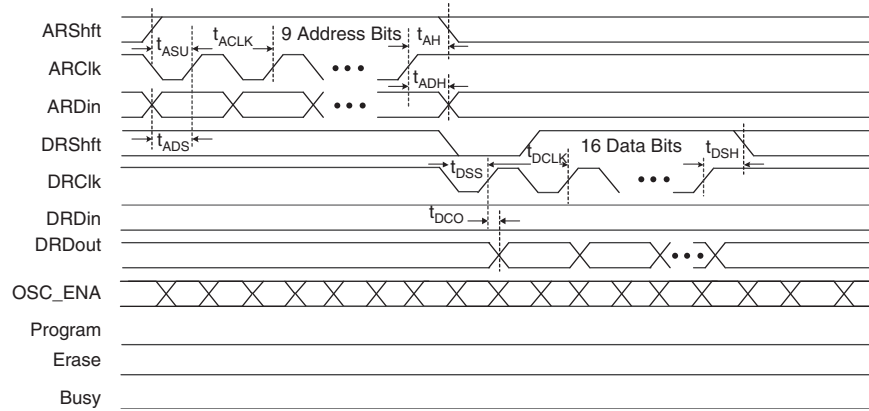


Figure 5-4. UFM Program Waveforms

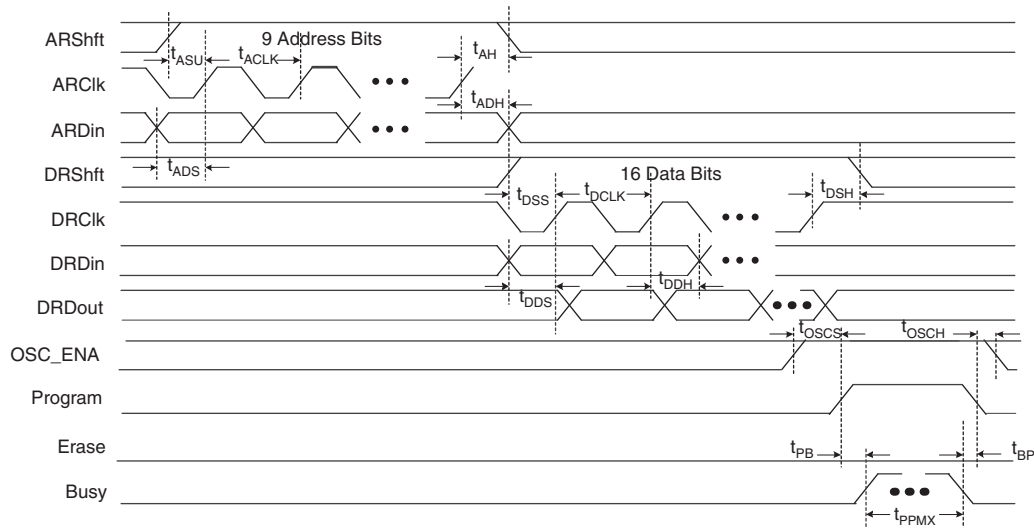


Figure 5-5. UFM Erase Waveform

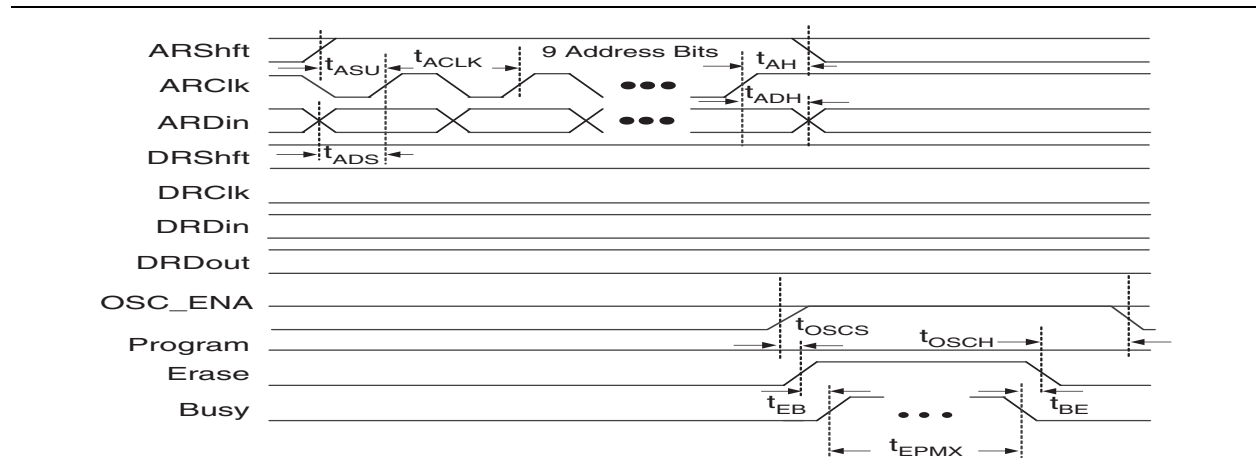


Table 5-22. Routing Delay Internal Timing Microparameters

Routing	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{C4}	—	429	—	556	—	687	—	(1)	—	(1)	ps
t_{R4}	—	326	—	423	—	521	—	(1)	—	(1)	ps
t_{LOCAL}	—	330	—	429	—	529	—	(1)	—	(1)	ps

Note to Table 5-22:

(1) The numbers will only be available in a later revision.

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTTL or for different drive strengths, use the I/O standard input and output delay adders in Table 5-27 through Table 5-28.

 For more information about each external timing parameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5-23 shows the external I/O timing parameters for EPM240 devices.

Table 5-23. EPM240 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	4.7	—	6.1	—	7.5	—	7.9	—	12.0	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.8	—	7.8	ns
t_{SU}	Global clock setup time	—	1.7	—	2.2	—	2.7	—	2.8	—	4.7	—	ns
t_H	Global clock hold time	—	0.0	—	0.0	—	0.0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.3	2.0	5.6	2.0	6.9	2.0	7.7	2.0	10.5	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	—	184.1	—	123.5	MHz

Note to Table 5-23:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-24 shows the external I/O timing parameters for EPM570 devices.

Table 5-24. EPM570 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	5.4	—	7.0	—	8.7	—	9.5	—	15.1	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.7	—	7.7	ns
t _{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	2.6	—	4.5	—	ns
t _H	Global clock hold time	—	0.0	—	0.0	—	0.0	—	0	—	0	—	ns
t _{CO}	Global clock to output delay	10 pF	2.0	4.5	2.0	5.8	2.0	7.1	2.0	6.1	2.0	7.6	ns
t _{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	ps
t _{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	ps
t _{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	ns
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	—	184.1	—	123.5	MHz

Note to Table 5-24:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-25 shows the external I/O timing parameters for EPM1270 devices.

Table 5-25. EPM1270 Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	6.2	—	8.1	—	10.0	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t _{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t _H	Global clock hold time	—	0.0	—	0.0	—	0.0	—	ns
t _{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns
t _{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t _{CL}	Global clock low time	—	166	—	216	—	266	—	ps

Table 5-25. EPM1270 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	MHz

Note to Table 5-25:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-26 shows the external I/O timing parameters for EPM2210 devices.

Table 5-26. EPM2210 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	7.0	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t_H	Global clock hold time	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	MHz

Note to Table 5-26:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

The I/O delay timing parameters for I/O standard input and output adders, and input delays are specified by speed grade independent of device density.

Table 5-27 through Table 5-28 show the adder delays associated with I/O pins for all packages. The delay numbers for -3, -4, and -5 speed grades shown in Table 5-27 through Table 5-30 are based on an EPM1270 device target, while -6 and -7 speed grade values are based on an EPM570Z device target. If an I/O standard other than 3.3-V LVTTTL is selected, add the input delay adder to the external t_{SU} timing parameters shown in Table 5-23 through Table 5-26. If an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength and fast slew rate is selected, add the output delay adder to the external t_{CO} and t_{PD} shown in Table 5-23 through Table 5-26.

Table 5-27. External Timing Input Delay Adders

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	ps
2.5-V LVTTTL	Without Schmitt Trigger	—	23	—	30	—	37	—	42	—	43	ps
	With Schmitt Trigger	—	339	—	441	—	543	—	429	—	476	ps
1.8-V LVTTTL	Without Schmitt Trigger	—	291	—	378	—	466	—	378	—	373	ps
1.5-V LVTTTL	Without Schmitt Trigger	—	681	—	885	—	1,090	—	681	—	622	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	ps

Table 5-28. MAX II IOE Programmable Delays

Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Delay from Pin to Internal Cells = 1	—	1,225	—	1,592	—	1,960	—	1,858	—	2,171	ps
Input Delay from Pin to Internal Cells = 0	—	89	—	115	—	142	—	569	—	609	ps

Maximum Input and Output Clock Rates

Table 5–29 and Table 5–30 show the maximum input and output clock rates for standard I/O pins in MAX II devices.

Table 5–29. MAX II Maximum Input Clock Rate for I/O

Standard		–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	Unit
3.3-V LVTTTL	Without Schmitt Trigger	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	MHz
2.5-V LVTTTL	Without Schmitt Trigger	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	MHz
2.5-V LVCMOS	Without Schmitt Trigger	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	MHz
1.8-V LVTTTL	Without Schmitt Trigger	200	200	200	200	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	200	200	200	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	150	150	150	150	MHz
3.3-V PCI	Without Schmitt Trigger	304	304	304	304	304	MHz

Table 5–30. MAX II Maximum Output Clock Rate for I/O

Standard	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	Unit
3.3-V LVTTTL	304	304	304	304	304	MHz
3.3-V LVCMOS	304	304	304	304	304	MHz
2.5-V LVTTTL	220	220	220	220	220	MHz
2.5-V LVCMOS	220	220	220	220	220	MHz
1.8-V LVTTTL	200	200	200	200	200	MHz
1.8-V LVCMOS	200	200	200	200	200	MHz
1.5-V LVCMOS	150	150	150	150	150	MHz
3.3-V PCI	304	304	304	304	304	MHz

JTAG Timing Specifications

Figure 5-6 shows the timing waveforms for the JTAG signals.

Figure 5-6. MAX II JTAG Timing Waveforms

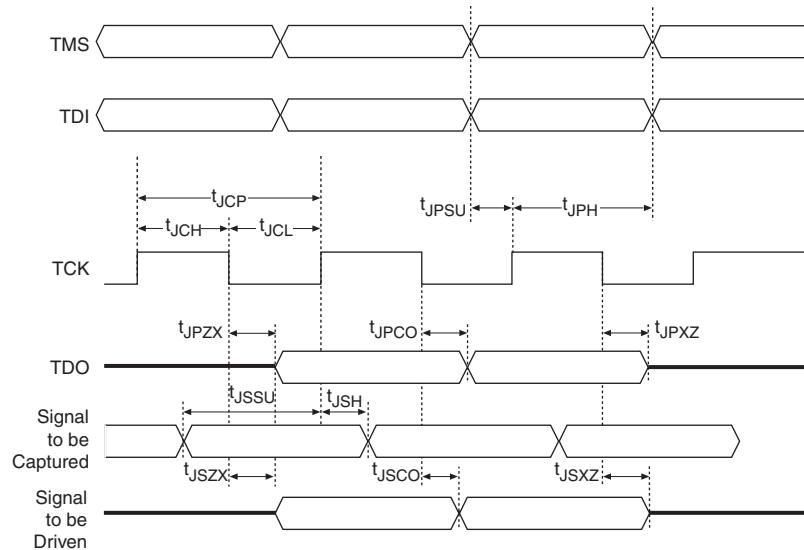


Table 5-31 shows the JTAG Timing parameters and values for MAX II devices.

Table 5-31. MAX II JTAG Timing Parameters (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JCP} (1)	TCK clock period for $V_{CCIO1} = 3.3\text{ V}$	55.5	—	ns
	TCK clock period for $V_{CCIO1} = 2.5\text{ V}$	62.5	—	ns
	TCK clock period for $V_{CCIO1} = 1.8\text{ V}$	100	—	ns
	TCK clock period for $V_{CCIO1} = 1.5\text{ V}$	143	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time (2)	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (2)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (2)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (2)	—	15	ns
t_{JSSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns

Table 5-31. MAX II JTAG Timing Parameters (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5-31:

- (1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.
- (2) This specification is shown for 3.3-V LVTTTL/LVCMOS and 2.5-V LVTTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVC MOS, the t_{JPSU} minimum is 6 ns and t_{JPC0} , t_{JPZX} , and t_{JPXZ} are maximum values at 35 ns.

Referenced Documents

This chapter references the following documents:

- *I/O Structure* section in the *MAX II Architecture* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*
- *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Document Revision History

Table 5-32 shows the revision history for this chapter.

Table 5-32. Document Revision History (Part 1 of 2)

Date and Revision	Changes Made	Summary of Changes
November 2008, version 2.4	<ul style="list-style-type: none"> ■ Updated Table 5-2. ■ Updated “Internal Timing Parameters” section. 	—
October 2008, version 2.3	<ul style="list-style-type: none"> ■ Updated New Document Format. ■ Updated Figure 5-1. 	—
July 2008, version 2.2	<ul style="list-style-type: none"> ■ Updated Table 5-14 , Table 5-23 , and Table 5-24. 	—
March 2008, version 2.1	<ul style="list-style-type: none"> ■ Added (Note 5) to Table 5-4. 	—
December 2007, version 2.0	<ul style="list-style-type: none"> ■ Updated (Note 3) and (4) to Table 5-1. ■ Updated Table 5-2 and added (Note 5). ■ Updated ICCSTANDBY and ICCPOWERUP information and added IPULLUP information in Table 5-4. ■ Added (Note 1) to Table 5-10. ■ Updated Figure 5-2. ■ Added (Note 1) to Table 5-13. ■ Updated Table 5-13 through Table 5-24, and Table 5-27 through Table 5-30. ■ Added tCOMB information to Table 5-15. ■ Updated Figure 5-6. ■ Added “Referenced Documents” section. 	Updated document with MAX IIZ information.
December 2006, version 1.8	<ul style="list-style-type: none"> ■ Added note to Table 5-1. ■ Added document revision history. 	—
July 2006, version 1.7	<ul style="list-style-type: none"> ■ Minor content and table updates. 	—
February 2006, version 1.6	<ul style="list-style-type: none"> ■ Updated “External Timing I/O Delay Adders” section. ■ Updated Table 5-29. ■ Updated Table 5-30. 	—
November 2005, version 1.5	<ul style="list-style-type: none"> ■ Updated Tables 5-2, 5-4, and 5-12. 	—
August 2005, version 1.4	<ul style="list-style-type: none"> ■ Updated Figure 5-1. ■ Updated Tables 5-13, 5-16, and 5-26. ■ Removed Note 1 from Table 5-12. 	—
June 2005, version 1.3	<ul style="list-style-type: none"> ■ Updated the R_{PULLUP} parameter in Table 5-4. ■ Added Note 2 to Tables 5-8 and 5-9. ■ Updated Table 5-13. ■ Added “Output Drive Characteristics” section. ■ Added I²C mode and Notes 5 and 6 to Table 5-14. ■ Updated timing values to Tables 5-14 through 5-33. 	—

Table 5-32. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
December 2004, version 1.2	<ul style="list-style-type: none">■ Updated timing Tables 5-2, 5-4, 5-12, and Tables 15-14 through 5-34.■ Table 5-31 is new.	—
June 2004, version 1.1	<ul style="list-style-type: none">■ Updated timing Tables 5-15 through 5-32.	—