

This section provides information for MAX<sup>®</sup> II design considerations.

This section includes the following chapters:

- [Chapter 16, Understanding Timing in MAX II Devices](#)
- [Chapter 17, Understanding and Evaluating Power in MAX II Devices](#)


### Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.




## Introduction

Altera® devices provide predictable device performance that is consistent from simulation to application. Before programming a device, you can determine the worst-case timing delays for any design. You can approximate propagation delays with either the Quartus® II Timing Analyzer or the timing models given in this chapter and the timing parameters listed in individual device data sheets.

 For the most precise timing results, you should use the Quartus II Timing Analyzer, which accounts for the effects of the secondary factors as mentioned later in this chapter.

This chapter defines external and internal timing parameters, and illustrates the timing models for the MAX® II device family.

 Familiarity with device architecture and characteristics is assumed. Refer to specific device or device family data sheets in this handbook for a complete description of the architecture, and for the specific values of the timing parameters listed in this chapter.

This chapter contains the following sections:

- “External Timing Parameters” on page 16–1
- “Internal Timing Parameters” on page 16–2
- “Internal Timing Parameters for MAX II UFM” on page 16–3
- “Timing Models” on page 16–4
- “Calculating Timing Delays” on page 16–5
- “Programmable Input Delay” on page 16–7
- “Timing Model versus Quartus II Timing Analyzer” on page 16–7

## External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. You can find the values of the external timing parameters in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by testing. All external timing parameters are shown in bold type. [Table 16–1](#) defines external timing parameters for the MAX II family.

**Table 16-1.** External Timing Parameters

Parameter	Description
$t_{PD1}$	Pin-to-pin delay for the worst case I/O placement with full a diagonal path across the device with combinational logic implemented in a single look-up table (LUT) in a logic array block (LAB) adjacent to output pin. Fast I/O Connection is used from the adjacent logic element (LE) to the output pin.
$t_{PD2}$	Pin-to-pin delay for the best case I/O placement with combinational logic (2-input AND gate) implemented in a single edge LE adjacent to the input pin. The longest pin path of the two inputs is shown. Fast I/O Connection is used from the adjacent LE to the output pin.
$t_{CLR}$	Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.
$t_{SU}$	Global clock setup time. The time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.
$t_H$	Global clock hold time. The time that data must be present at the input pin after the global clock signal is asserted at the clock pin.
$t_{CO}$	Global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.
$t_{CNT}$	Minimum global clock period. The minimum period maintained by a globally clocked counter.

## Internal Timing Parameters

Within a device, the timing delays contributed by individual architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal parameters are shown in italic type. [Table 16-2](#) defines the internal timing microparameters for the MAX II device family.

**Table 16-2.** Internal Timing Microparameters (Part 1 of 2)

Parameter	Description
$t_{LUT}$	LE combinational LUT delay for data-in to data-out.
$t_{COMB}$	Combinational path delay. The delay from the time when a combinational logic signal from the LUT bypasses the LE register to the time it becomes available at the LE output.
$t_{CLR}$	LE register clear delay. The delay from the assertion of the register's asynchronous clear input to the time the register output stabilizes at logical low.
$t_{PRE}$	LE register preset delay. The delay from the assertion of the register's asynchronous preset input to the time the register output stabilizes at logical high.
$t_{SU}$	LE register setup time before clock. The time required for a signal to be stable at the register's data and enable inputs before the register clock rising edge to ensure that the register correctly stores the input data.
$t_H$	LE register hold time after clock. The time required for a signal to be stable at the register's data and enable inputs after the register clock's rising edge to ensure that the register correctly stores the input data.
$t_{CO}$	LE register clock-to-output delay. The delay from the rising edge of the register's clock to the time the data appears at the register output.
$t_C$	Register control delay. The time required for a signal to be routed to the clock, preset, or clear input of an LE register.
$t_{FASTIO}$	Combinational output delay. $t_{FASTIO}$ is the time required for a combinational signal from the LE adjacent to the I/O block using the fast I/O connection.
$t_{IN}$	I/O input pad and buffer delay. The $t_{IN}$ applies to I/O pins used as inputs.
$t_{GLOB}$	$t_{GLOB}$ applies to $GCLK$ pins when used for global signals. $t_{GLOB}$ is the delay required for a global signal to be routed from the $GCLK$ pins to the LAB column clocks through the global clock network.

**Table 16–2.** Internal Timing Microparameters (Part 2 of 2)

Parameter	Description
$t_{IOE}$	Internal generated output enable delay. The delay from an internally generated signal on the interconnect to the output enable of the tri-state buffer.
$t_{DL}$	Input routing delay. The delay incurred from the row I/O pin used as input to the LE adjacent to it.
$t_{ODR}$	Output data delay for the row interconnect. The delay incurred by signals routed from an interconnect to an I/O cell.
$t_{OD}$	Output delay buffer and pad delay. Refer to <i>Timing Model and Specifications</i> section in the <i>DC and Switching Characteristics</i> chapter in the <i>MAX II Device Handbook</i> for delay adders associated with different I/O standards, drive strengths, and slew rates.
$t_{XZ}$	Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's enable control is disabled. Refer to <i>Timing Model and Specifications</i> section in the <i>DC and Switching Characteristics</i> chapter in the <i>MAX II Device Handbook</i> for delay adders associated with different I/O standards, drive strengths, and slew rates.
$t_{ZX}$	Output buffer enable delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. Refer to <i>Timing Model and Specifications</i> section in the <i>DC and Switching Characteristics</i> chapter in the <i>MAX II Device Handbook</i> for delay adders associated with different I/O standards, drive strengths, and slew rates.
$t_{C4}$	Delay for a column interconnect with average loading. The $t_{C4}$ covers a distance of four LAB rows.
$t_{R4}$	Delay for a row interconnect with average loading. The $t_{R4}$ covers a distance of four LAB columns.
$t_{LOCAL}$	Local interconnect delay.

## Internal Timing Parameters for MAX II UFM

Timing parameters for MAX II user flash memory (UFM) are the timing delays contributed by the UFM architectural elements, which cannot be measured explicitly. All timing parameters are shown in italic type. [Table 16–3](#) defines the timing microparameters for MAX II UFM.

**Table 16–3.** Internal Timing Microparameters for MAX II UFM (Part 1 of 2)

Parameter	Description
$t_{ASU}$	Address register shift signal setup to address register clock.
$t_{AH}$	Address register shift signal hold from address register clock.
$t_{ADS}$	Address register data in setup to address register clock.
$t_{ADH}$	Address register data in hold from address register clock.
$t_{DSS}$	Data register shift signal setup to data register clock.
$t_{DSH}$	Data register shift signal hold from data register clock.
$t_{DDS}$	Data register data in setup to data register clock.
$t_{DDH}$	Data register data in hold from data register clock.
$t_{DCO}$	Delay incurred from the data register clock to data register output when shifting the data out.
$t_{DP}$	PROGRAM signal to data clock hold time.
$t_{PB}$	Maximum delay between PROGRAM rising edge to UFM BUSY signal rising edge.
$t_{BP}$	Minimum delay allowed from UFM BUSY signal going low to PROGRAM signal going low.
$t_{PPMX}$	Maximum length of busy pulse during a program.
$t_{AE}$	Minimum ERASE signal to address clock hold time.

**Table 16-3.** Internal Timing Microparameters for MAX II UFM (Part 2 of 2)

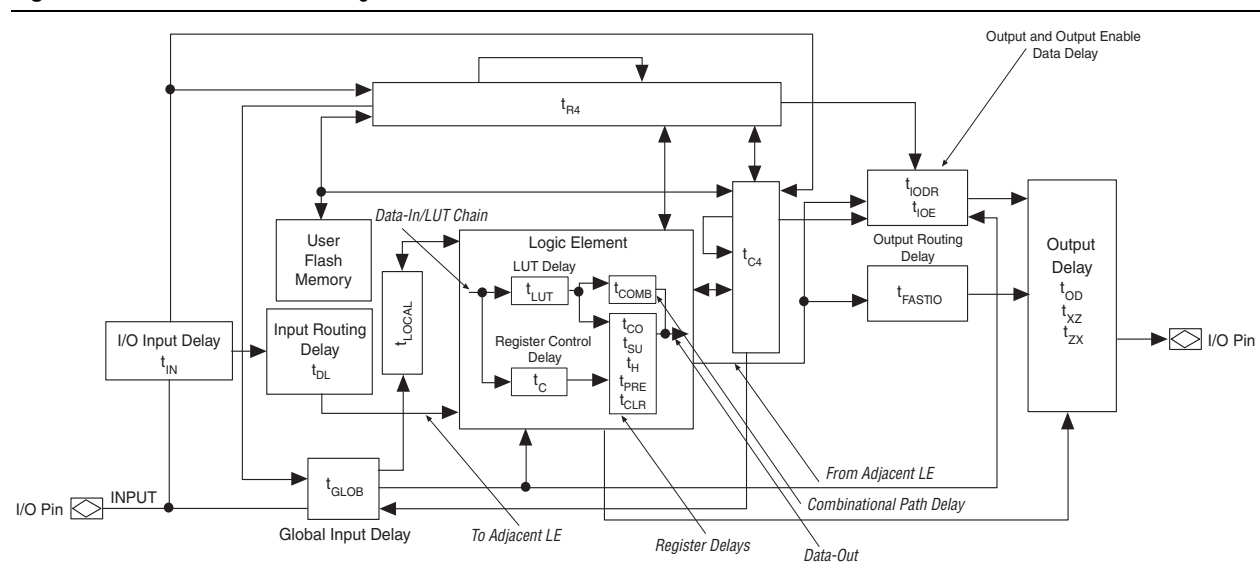
Parameter	Description
$t_{EB}$	Maximum delay between ERASE rising edge to UFM BUSY signal rising edge.
$t_{BE}$	Minimum delay allowed from UFM BUSY signal going low to ERASE signal going low.
$t_{EPMX}$	Maximum length of busy pulse during an erase.
$t_{RA}$	Maximum read access time. The delay incurred between the DRSHT signal going low to the first bit of data observed at the data register output.
$t_{OE}$	Delay from OSC_ENA signal reaching UFM to rising clock of OSC leaving the UFM.
$t_{OSCS}$	Maximum delay between the OSC_ENA rising edge to the ERASE/PROGRAM signal rising edge.
$t_{OSCH}$	Minimum delay allowed from the ERASE/PROGRAM signal going low to the OSC_ENA signal going low.

## Timing Models

Timing models are simplified block diagrams that illustrate the delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your design by examining the equations listed in the Quartus II Report File (.rpt) for the project. You can then add up the appropriate internal timing parameters to estimate the delays through the device.

The MAX II architecture has a globally routed clock. The MultiTrack interconnect ensures predictable performance, accurate simulation, and accurate timing analysis across all MAX II device densities and speed grades.

Figure 16-1 shows the timing model for MAX II devices. The timing model is the preliminary version which is subject to change. The final version of the timing model will be released once available.

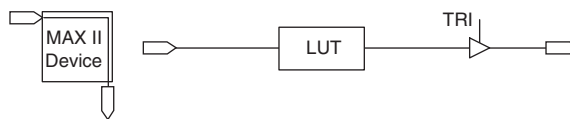
**Figure 16-1.** MAX II Device Timing Model

## Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for MAX II devices with the timing model shown in Figure 16-1 and by referring to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 16-2 through Figure 16-6 show the external timing parameters for the MAX II device family. To calculate the delay for a signal that follows a different path through the MAX II device, refer to the timing model to determine which internal timing parameters to add together.

For the most precise timing results, use the Quartus II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

**Figure 16-2.** External Timing Parameter ( $t_{PD1}$ ) *Note (1)*



**Note to Figure 16-2:**

$$(1) \quad t_{PD1} = t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT} + t_{COMB} + t_{FASTIO} + (t_{OD} + \Delta t_{OD})$$

Table 16-4 lists the numbers of LABs according to device density.

**Table 16-4.** Numbers of LABs According to Device Density

Device Density	N LAB Rows	M LAB Columns
EPM240	4	6
EPM570	7	12
EPM1270	10	16
EPM2210	13	20

$Dt_{OD}$  is the adder delay (see note to Figure 16-2) for the  $t_{OD}$  microparameter when using an I/O standard other than 3.3-V LVTTTL with 16 mA current strength.

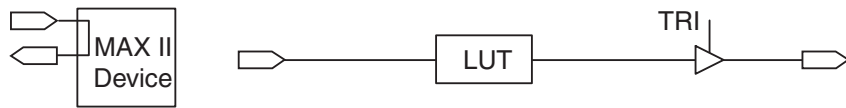
Refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* for adder delay values.

The following is an example:

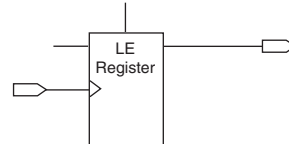
$t_{PD1}$  for the EPM240 device using an I/O standard of 3.3-V LVTTTL fast slew rate with a drive strength of 16 mA:

$$t_{PD1} = t_{IN} + 4 \times t_{R4}/4 + 6 \times t_{C4}/4 + t_{LUT} + t_{COMB} + t_{FASTIO} + t_{OD} \dots (a)$$

$t_{PD1}$  for the EPM240 device using an I/O standard of 2.5-V LVTTTL fast slew rate with a drive strength of 7 mA:  $t_{PD1} = (a) + (Dt_{OD} \text{ of 2.5-V LVTTTL fast slew 7 mA})$

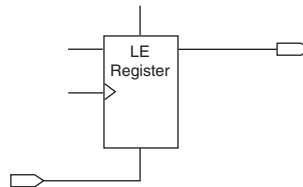
**Figure 16-3.** External Timing Parameter ( $t_{PD2}$ ) *Note (1)***Note to Figure 16-3:**

$$(1) \quad t_{PD2} = t_{IN} + t_{DL} + t_{LUT} + t_{COMB} + t_{FASTIO} + (t_{OD} + \Delta t_{OD})$$

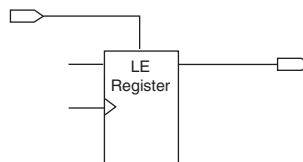
**Figure 16-4.** External Timing Parameter ( $t_{CO}$ ) *Note (1), (2)***Notes to Figure 16-4:**

$$(1) \quad t_{CO} = t_{GLOB} + t_C + t_{CO} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ OR } t_{IODR}) + (t_{OD} + \Delta t_{OD})$$

(2) The constants N and M are subject to change according to the position of the LAB in the entire device.

**Figure 16-5.** LE Register Clear and Preset Time ( $t_{CLR}$ ) *Note (1)***Note to Figure 16-5:**

$$(1) \quad t_{CLR} = t_{GLOB} + t_C + t_{CLR} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ OR } t_{IODR}) + (t_{OD} + \Delta t_{OD})$$

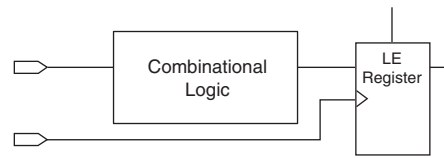
**Figure 16-6.** LE Register Clear and Preset Time ( $t_{PRE}$ ) *Note (1)***Note to Figure 16-6:**

$$(1) \quad t_{PRE} = t_{GLOB} + t_{LOCAL} + t_C + t_{PRE} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ OR } t_{IODR}) + (t_{OD} + \Delta t_{OD})$$

### Setup and Hold Time from an I/O Data and Clock Input

The Quartus II software might insert additional routing delays from the input pin to the register input to ensure a zero hold time for the LE register. Altera recommends that you use the Quartus II Timing Analyzer to obtain the setup time and hold time. See [Figure 16-7](#) and [Figure 16-8](#).

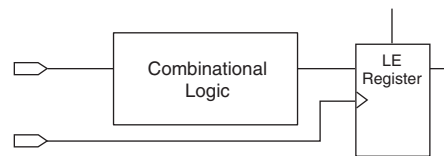
**Figure 16-7.** Setup and Hold Time ( $t_{SU}$ ) *Note (1)*



**Note to Figure 16-7:**

$$(1) t_{SU} = (t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT}) - (t_{GLOB} + t_C) + t_{SU}$$

**Figure 16-8.** Setup and Hold Time ( $t_H$ ) *Note (1)*



**Note to Figure 16-8:**

$$(1) t_H = (t_{GLOB} + t_C) - (t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT}) + t_H$$



For Figure 16-4 through Figure 16-8, the constants N and M are subject to change according to the position of LAB in the entire device for combinational logic implementation.

## Programmable Input Delay

The programmable input delay provides an option to add a delay to the input pin, guaranteeing a zero hold time. You can set this option in the Assignment Editor (Assignments menu) on a pin-by-pin basis. The following procedure shows how to turn on the input delay for the selected input pin in the Quartus II software:

1. Select input pin name in the design file.
2. Right-click and select **Locate** in the Assignment Editor.
3. Double-click the cell under Assignment Name and select **Input Delay from Pin to Internal Cells** in the pull-down list.
4. Double-click the **Value** cell to the right of the assignment name just made and enter 1.
5. On the File menu, click **Save**.

## Timing Model versus Quartus II Timing Analyzer

Hand calculations based on the timing model provide a good estimate of a design's performance. However, the Quartus II Timing Analyzer always provides the most accurate information on design performance because it takes into account secondary factors that influence the routing microparameters such as:

- Fan-out for each signal in the delay path
- Positions of other loads relative to the signal source and destination

- Distance between the signal source and destination
- Various interconnect lengths where some interconnects are truncated at the edge of the device

## Conclusion

The MAX II device architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. The Quartus II Timing Analyzer provides the most accurate timing information. However, you can use the timing model along with the timing parameters listed in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* to estimate a design's performance before compilation. Both methods enable you to accurately predict your design's in-system timing performance.

## Referenced Documents

This chapter references the following document:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*

## Document Revision History

Table 16-5 shows the revision history for this chapter.

**Table 16-5.** Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.1	<ul style="list-style-type: none"> <li>■ Updated New Document Format.</li> </ul>	—
December 2007, version 2.0	<ul style="list-style-type: none"> <li>■ Updated <math>t_{PD2}</math> information in Table 16-1.</li> <li>■ Added <math>t_{COMB}</math> information in Table 16-2.</li> <li>■ Updated Figure 16-1.</li> <li>■ Updated Note (1) to Figure 16-2.</li> <li>■ Updated "Calculating Timing Delays" section.</li> <li>■ Added "Referenced Documents" section.</li> </ul>	—
December 2006, version 1.4	<ul style="list-style-type: none"> <li>■ Added document revision history.</li> </ul>	—
January 2005, version 1.3	<ul style="list-style-type: none"> <li>■ Previously published as Chapter 17. No changes to content.</li> </ul>	—
December 2004, version 1.2	<ul style="list-style-type: none"> <li>■ Added section Programmable Input Delay.</li> </ul>	—
June 2004, version 1.1	<ul style="list-style-type: none"> <li>■ Updated Table 16-1. Various parameter naming updates.</li> </ul>	—

## Introduction

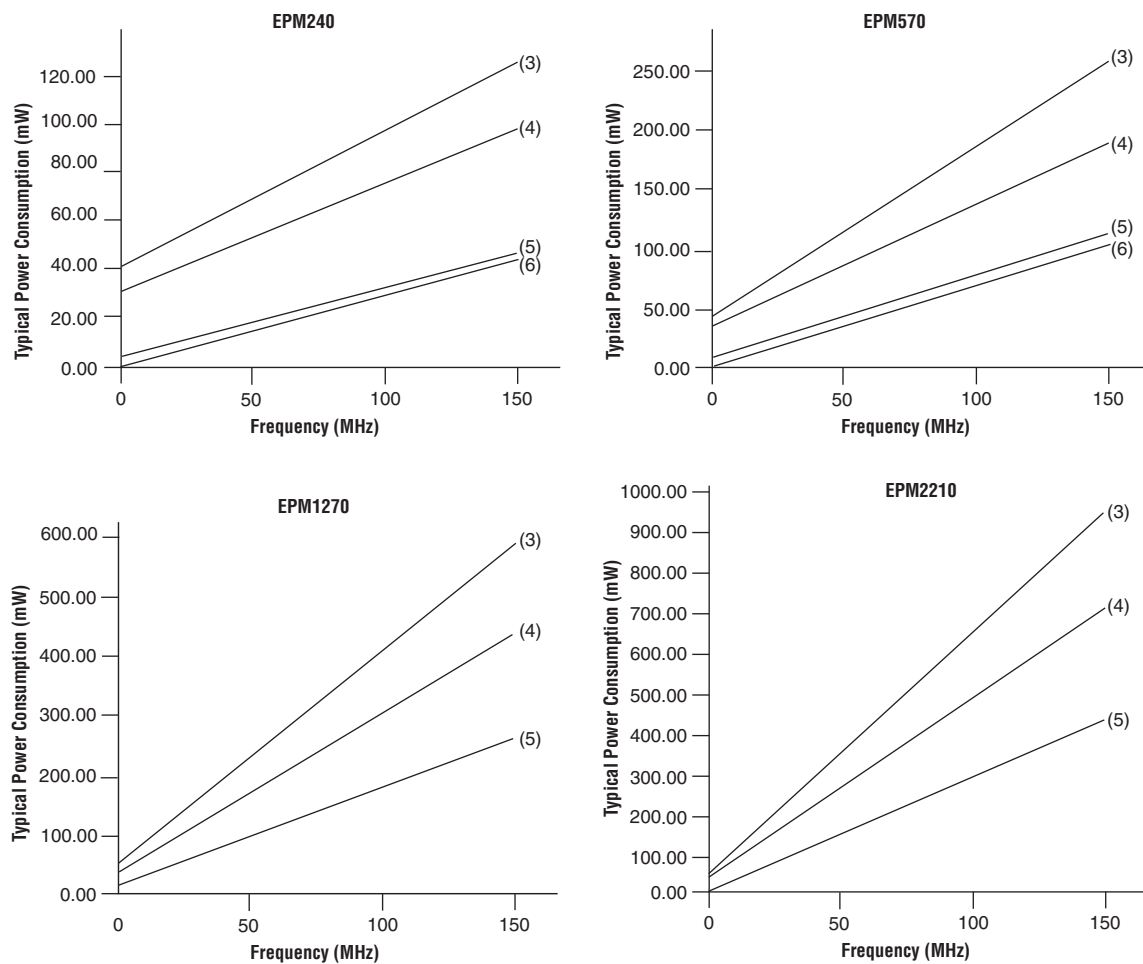
Power consumption has become an important factor for CPLD applications with the increased use of CPLDs in low power designs. Overall low standby (static) and dynamic power is becoming increasingly important to reduce system power, and can be achieved with MAX® II devices which have low stand-by and dynamic power.

This chapter contains the following sections:

- “Power in MAX II Devices” on page 17-1
- “MAX II Power Estimation Using the PowerPlay Early Power Estimator” on page 17-3
- “PowerPlay Early Power Estimator Inputs” on page 17-3
- “Power Estimation Summary” on page 17-13
- “Power Saving Techniques” on page 17-15

## Power in MAX II Devices

Different from previous CPLD architectures, MAX II logic does not use sense amplifiers that require bias currents to amplify signal voltages within the device. Additionally, with the Quartus® II software, efficient implementation of most interconnects with local routing in MAX II devices significantly lowers the dynamic power. [Figure 17-1](#) shows the typical power consumption versus frequency for MAX II devices. The power consumption (mWatts) provided is based on typical conditions using a pattern that fills a device with a 16-bit, loadable, enabled, up/down counter with no output load.

**Figure 17-1.** Power Consumption versus Frequency for MAX II Devices (Note 1), (2)**Notes to Figure 17-1:**

- (1) Every device is fully utilized with 16-bit counters for power estimation.
- (2) The MAX II and MAX IIG devices can operate up to 304 MHz.
- (3)  $V_{CCINT} = 3.3\text{ V}$
- (4)  $V_{CCINT} = 2.5\text{ V}$
- (5)  $V_{CCINT} = 1.8\text{ V}$  (MAX IIG)
- (6)  $V_{CCINT} = 1.8\text{ V}$  (MAX IIZ)

The power consumed in MAX II devices is dependent on the design. It is very important to complete a power evaluation early in the design process to ensure that the power dissipation by MAX II devices meets system requirements and specifications.

This chapter discusses how to evaluate and manage MAX II power using the MAX II PowerPlay Early Power Estimator spreadsheet, available at [www.altera.com](http://www.altera.com).

## MAX II Power Estimation Using the PowerPlay Early Power Estimator

The PowerPlay Early Power Estimator spreadsheet allows you to enter information into sections based on architectural features. The PowerPlay Early Power Estimator spreadsheet also provides a subtotal of power consumed by each architectural feature reported in each section in mWatts (mW). Figure 17-2 shows the overview of the MAX II PowerPlay Early Power Estimator summary worksheet.

Figure 17-2. MAX II PowerPlay Early Power Estimator

**PowerPlay Early Power Estimator**  
 MAX<sup>®</sup> II Family v7.2 [Release Notes](#)

Visit the Online [Power Management Resource Center](#)

Comments:


Input Parameters	Power (mW)	Thermal Analysis
Device: EPM240	Clocks: 0.00	Junction Temp, T <sub>J</sub> (°C): 27.0
Package: F100	Logic: 0.00	θ <sub>JA</sub> Junction-Ambient: 51.20
Temperature Grade: Commercial	UFM: 0.00	Maximum Allowed T <sub>A</sub> (°C): 82.9
Power Characteristics: Typical	I/O: 0.00	
V <sub>CCINT</sub> Supply Voltage: 3.3 V	Voltage Regulator: 0.00	
Ambient Temp, T <sub>A</sub> (°C): 25	P <sub>STANDBY</sub> : 39.63	
Airflow: Still Air	P <sub>TOTAL</sub> : 39.63	
		<b>Power Supply Current (mA)</b>
		I <sub>CCPOWERUP</sub> : 55.00
		I <sub>CCINT</sub> : 12.00
		I <sub>CCIO</sub> : 0.02
		Click 'I <sub>CCIO</sub> ' for I <sub>CCIO</sub> per Bank

Buttons: Set Toggle % | Reset | Import Quartus File | Import EPE v6.1

Errors:

Warnings:

Messages:  
 Quartus II Power Output File: <None>  
 File Load Date: <N/A>

 The power estimator results are based on estimated power data from device simulations and typical silicon measurements under nominal conditions. Results obtained should only be used as an estimation of power, not as a specification. The actual I<sub>CC</sub> must be verified during device operation, as this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

## PowerPlay Early Power Estimator Inputs

The following sections of the chapter explain what values you need to enter for the PowerPlay Early Power Estimator spreadsheet. The areas of entry in the PowerPlay Early Power Estimator spreadsheet include input parameters, clock, logic, UFM, and input/output (I/O) module.

## Input Parameters

Different MAX II devices consume different amounts of power for the same design. The larger the device, the more power it consumes because of a larger clock tree. In the Main section, you can enter the following parameters for the device and design:

- Device
- Package
- Temperature grade
- Power characteristics
- $V_{CCINT}$  supply
- Ambient temperature
- Airflow

Figure 17-3 shows the Input Parameter section in the PowerPlay Early Power Estimator spreadsheet.

**Figure 17-3.** Input Parameter Section

Table 17-1 describes the values that must be specified in the Input Parameter section of the PowerPlay Early Power Estimator spreadsheet.

**Table 17-1.** Input Parameter Section Information (Part 1 of 2)

Input Parameter	Description
Device	Select your MAX II device. Larger devices have slightly higher clock dynamic power. MAX IIZ devices have the lowest $I_{CCINT}$ compared to the MAX II and MAX IIG devices because MAX IIZ devices have optimized circuitry to reduce $I_{CCINT}$ . Compared to MAX II devices, MAX IIG devices use less power because they do not use the on-chip voltage regulator.
Package	Select the package that will be used. Larger packages provide a larger cooling surface and more contact points to the circuit board, leading to lower thermal resistance. Package selection does not affect power consumption.
Temperature Grade	Commercial devices have a maximum junction operating temperature of 85°C. Industrial devices offer 100°C operation while the MAX II automotive-grade devices can operate up to 125°C. This field affects the maximum junction temperature used in thermal calculations.
Power Characteristics	For MAX IIZ devices, you can select either typical or maximum power characteristics for the power estimation. The power characteristics are based on typical and theoretical worst-case silicon process. <i>Maximum</i> should be used for thermal design, while <i>Typical</i> gives you the estimation of the average use of the devices.

**Table 17-1.** Input Parameter Section Information (Part 2 of 2)

Input Parameter	Description
V <sub>CCINT</sub> Supply	The voltage of the V <sub>CCINT</sub> power supply. For MAX IIG and MAX IIZ devices, the supply voltage must be 1.8 V. For other devices, it can be either 2.5 V or 3.3 V. Devices with lower V <sub>CCINT</sub> have lower total standby power consumption.
Ambient Temperature	Enter the air temperature near the CPLD. This value can range from -40°C to 125°C, depending on the device temperature grade. This parameter is used to compute junction temperature based on power dissipation and thermal resistances through the top of the chip.
Airflow	Select an available ambient airflow in linear feet per minute (lfm) or meters per second (m/s). The options are still air, 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), or 400 lfm (2.0 m/s). Increased airflow results in a lower junction-to-air thermal resistance, and thus lower junction temperature.

## Clock Section

MAX II devices have four global clocks each. Each row in the Clock Domain subsection of the spreadsheet represents a clock network or a separate clock domain. You must enter the clock frequency (f<sub>MAX</sub>) in MHz, the total fan-out for each clock network used, and the local clock enable percentage. Figure 17-4 shows the Clock section in the PowerPlay Early Power Estimator spreadsheet.

**Figure 17-4.** Clock Section

Clock Domain	Clock Freq (MHz)	Total Fanout	Local Enable %	Total Power (mW)	User Comments
	0.0	0	50%	0.00	
	0.0	0	50%	0.00	
	0.0	0	50%	0.00	
	0.0	0	50%	0.00	

Table 17-2 describes the parameters in the Clock section of the PowerPlay Early Power Estimator spreadsheet.

**Table 17-2.** Clock Section Information

Column Heading	Description
Clock Domain	Enter a name for the clock network in this column (optional entry).
Clock Frequency (MHz)	Enter the frequency of the clock domain. The operating frequency for MAX II and MAX IIG is between 0 and 304 MHz. For MAX IIZ, the operating frequency is between 0 and 152 MHz.
Total Fanout	Enter the total number of logic element (LE) flipflops fed by this clock. The number of resources driven by every global clock is reported in the Fanout column of the Quartus II Compilation Report under Fitter > Resource Section > Global & Other Fast Signals > Fanout.
Local Enable %	Enter the average percentage of time that clock enable is high for destination flipflops. Local clock enables for flipflops in the LEs are promoted to logic array block (LAB)-wide signals. When a given flipflop is disabled, the LAB-wide clock is also disabled, cutting clock power in addition to power for downstream logic. This sheet models only the impact on clock tree power.
Total Power (mW)	Represents the total power dissipation due to clock distribution.
User Comments	Enter any comments (optional entry).

## Logic Section

A design is a combination of several design modules operating at different frequencies and toggle rates. Each design module can have a different amount of logic. For the most accurate power estimation, partition the design into different design modules. You can partition your design by grouping modules by clock frequency, location, hierarchy, or entities. Figure 17-5 shows the logic section in the PowerPlay Early Power Estimator spreadsheet.

**Figure 17-5.** Logic Section

Logic Module	Clock Freq (MHz)	# LEs	Toggle %	Power (mW)			User Comments
				Routing	Block	Total	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	

Each row in the Logic section represents a separate design module. Table 17-3 describes the parameters in the Logic section of the PowerPlay Early Power Estimator spreadsheet.

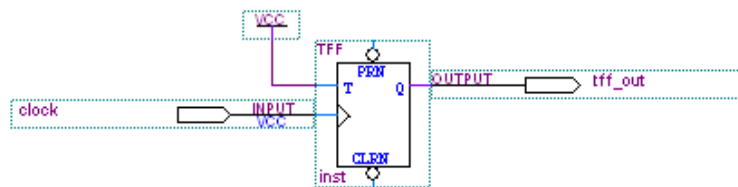
**Table 17-3.** Logic Section Information (Part 1 of 2)

Column Heading	Description
Logic Module	Enter a name for each module of the design (optional entry).
Clock Frequency (MHz)	Enter a clock frequency (MHz). The operating frequency for MAX II and MAX IIG is between 0 and 304 MHz. For MAX IIZ, the operating frequency is between 0 and 152 MHz. A 100 MHz input clock with a 12.5% toggle means that each look-up table (LUT) or flipflop output toggles 12.5 million times per second ( $100 \times 12.5\%$ ).
# LEs	Enter the number of LEs in this module.
Toggle %	<p>Enter the average percentage of logic toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To ensure you do not underestimate the toggle percentage, you can use a higher toggle percentage. Most logic toggles infrequently, and therefore toggle rates of &lt;50% are more realistic.</p> <p>For example, a TFF with its input tied to <math>V_{CC}</math> has a toggle rate of 100% because its output is changing logic states on every clock cycle (see Figure 17-6). Figure 17-7 shows an example of a 4-bit counter. The first TFF with least significant bit (LSB) output <math>cout_0</math> has a toggle rate of 100% because the signal toggles on every clock cycle. The toggle rate for the second TFF with output <math>cout_1</math> is 50% since the signal only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with output <math>cout_2</math> and fourth TFF with output <math>cout_3</math> are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is <math>(100 + 50 + 25 + 12.5)/4 = 46.875\%</math>.</p>

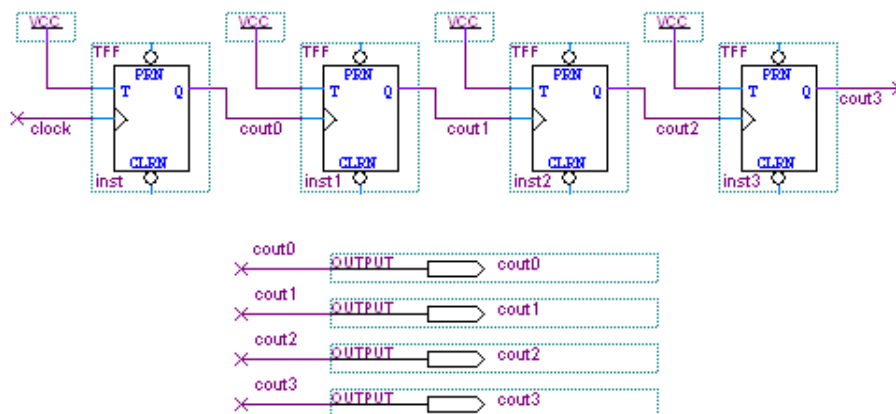
**Table 17-3.** Logic Section Information (Part 2 of 2)

Column Heading	Description
Routing	<p>Represents the power dissipation due to estimated routing.</p> <p>Routing power is highly dependent on placement and routing, which itself is a function of design complexity. The values shown are representative of routing power average based on experimentation on over 100 real-world designs.</p> <p>Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design.</p>
Block	<p>Represents the power dissipation due to internal toggling of the LEs.</p> <p>Logic block power is a function of the function implemented and relative toggle rates of the various inputs. The PowerPlay Early Power Estimator spreadsheet uses an estimate based on observed behavior across over 100 real-world designs.</p> <p>Use the Quartus II PowerPlay Power Analyzer for an accurate analysis based on the exact synthesis of your design.</p>
Total	Represents the total power dissipation. The total power dissipation is the sum of the routing and block power.
User Comments	Enter any comments (optional entry).

**Figure 17-6.** T-Flipflop



**Figure 17-7.** 4-Bit Counter



## UFM Section

When the design utilizes the UFM, the PowerPlay Early Power Estimator spreadsheet considers the time spent during read operations into the power estimation.

Figure 17-8 shows the UFM section in the PowerPlay Early Power Estimator spreadsheet.

**Figure 17-8.** UFM Section

UFM Module	Read %	Total Power (mW)	User Comments
	0.0%	0.00	

Table 17-4 describes the parameters in the UFM section of the PowerPlay Early Power Estimator spreadsheet.

**Table 17-4.** UFM Section Information

Column Heading	Description
UFM Module	Enter a name for the UFM module in this column (optional entry).
Read %	Enter the percentage of time the UFM spends in Read mode. It takes 16 clock cycles to shift the serial data out after an internal UFM read so the read operation occurs less than 1/17 (or about 6%) of the time. The clock in this calculation is the UFM block's DRCLK signal.
Total Power (mW)	Total power dissipation due to reading from the UFM block (mW). Programming and erasing can only be performed a limited number of times over the life of the device so they do not contribute to average power.
User Comments	Enter any comments (optional entry).

## I/O Section

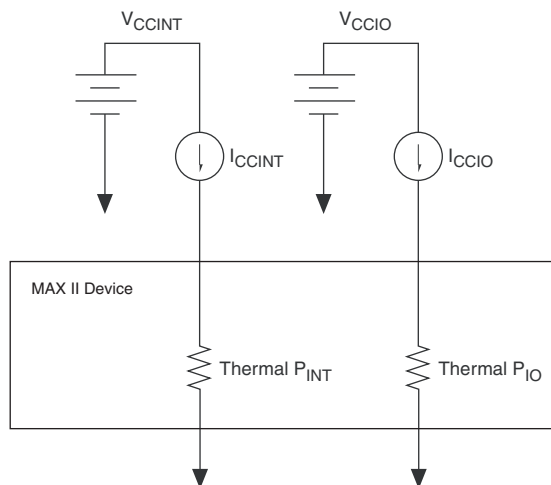
MAX II devices feature programmable I/O pins that support a wide range of industry I/O standards for increased design flexibility. The I/O section in the PowerPlay Early Power Estimator spreadsheet allows you to estimate the I/O pin power consumption based on the pin's I/O standards.

The total thermal power is the sum of the thermal power consumed by the device based on each power rail.

$$\text{Thermal Power} = \text{Thermal } P_{\text{INT}} + \text{Thermal } P_{\text{IO}}$$

Figure 17-9 shows a graphical representation of the thermal power consumption.

**Figure 17-9.** Thermal Power Representation



The PowerPlay Early Power Estimator spreadsheet estimates the current for each I/O bank based on the  $V_{CCIO}$  settings, if you specify the I/O bank for I/O pins in the I/O section. Figure 17-10 shows the I/O bank parameter settings.

**Figure 17-10.** I/O Bank Parameter Settings

	$V_{CCIO}$ (V)	$I_{CCIO}$ (mA)
I/O Bank 1	1.5	0.01
I/O Bank 2	1.5	0.01
N/A	1.5	0.00
N/A	1.5	0.00
Unassigned		0.00

Table 17-5 describes the I/O bank parameters in the I/O section of the PowerPlay Early Power Estimator spreadsheet.

**Table 17-5.** I/O Bank Information

Column Heading	Description
$V_{CCIO}$	Select the $V_{CCIO}$ voltage for each bank. Used to cross-check selected I/O standards in I/O section for warning purposes.
$I_{CCIO}$	Shows the total supply current due to the I/O pins in each I/O bank.
Unassigned	Represents the $I_{CCIO}$ of all I/O modules not assigned to an I/O bank.

Each row in the I/O section represents a design module where the I/O pins have the same frequency, toggle percentage, average capacitive load, I/O standard, and I/O bank. Figure 17-11 shows the I/O section of the PowerPlay Early Power Estimator spreadsheet and Table 17-6 describes the I/O module parameters.

Figure 17-11. I/O Section

Module	I/O Standard	Clock Freq (MHz)	# Output Pins	# Input Pins	# Bidir Pins	I/O Bank	Toggle %	OE %	Load (pF)	Bank I/O Std Check	Bank Voltage Check	Power (mW)			Supply Current (mA)		User Comments
												Routing	Block	Total	I <sub>CCINT</sub>	I <sub>CCIO</sub>	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
1.5 V 2mA	▼	0.0	0	0	0	?	12.5%	100%	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	

Table 17-6. I/O Section Information (Part 1 of 2)

Column Heading	Description
Module	Enter a name for the module in this column (optional entry).
I/O Standard	Select the I/O standard for the input, output, or bidirectional pins in this module from the pull-down list. The calculated I/O power varies based on the I/O standard.
Clock Freq (MHz)	Enter the clock frequency (MHz). The operating frequency for MAX II and MAX IIG is between 0 and 304 MHz. For MAX IIZ, the operating frequency is between 0 and 152 MHz. A 100 MHz input clock with a 12.5% toggle means that each I/O pin toggles 12.5 million times per second ( $100 \times 12.5\%$ ).
# Output Pins	Enter the number of output pins in this module.
# Input Pins	Enter the number of input pins in this module.
# Bidir Pins	Enter the number of bidirectional pins in this module.  An I/O pin configured as bidirectional but used only as an output consumes more power than one configured as an output-only, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin).
I/O Bank	Select the I/O bank for the module. If you do not know which I/O bank the pins will be assigned to, leave the value as "?". Assigning the I/O module to a bank checks whether your I/O voltage assignments are compatible or not, allowing per-bank I <sub>CCIO</sub> reporting.  The PowerPlay Early Power Estimator spreadsheet does not take any I/O placement constraints into consideration except for I/O standard and bank match, and I/O voltage.
Toggle %	Enter the average percentage of output, bidirectional, and input pins toggling on each clock cycle. The toggle percentage ranges from 0 to 100% for output pins and can be up to 200% for input pins used as clocks because clocks toggle at twice the clock frequency.  Typically, the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.

**Table 17-6.** I/O Section Information (Part 2 of 2)

Column Heading	Description
OE %	<p>Enter the average percentage of time that:</p> <ul style="list-style-type: none"> <li>■ The output I/O pins are enabled.</li> <li>■ Bidirectional I/O pins are outputs and enabled.</li> </ul> <p>During the remaining time:</p> <ul style="list-style-type: none"> <li>■ Output I/O pins are tri-stated.</li> <li>■ Bidirectional I/O pins are inputs.</li> </ul> <p>This number must be a percentage between 0% and 100%.</p>
Load (pF)	<p>Enter the pin loading external to the chip (pF). This parameter only applies to output and bidirectional pins.</p> <p>Pin and package capacitance is already included in the I/O model. Therefore, you only need to include off-chip capacitance in the Load parameter.</p>
Bank I/O Std Check	Indicates whether the selected I/O standard is available on the selected I/O bank or not. Not all I/O banks can implement every I/O standard.
Bank Voltage Check	Indicates whether the selected I/O bank has a voltage compatible with the selected I/O standard or not.
Routing	<p>Represents the power dissipation due to estimated routing.</p> <p>Routing power is highly dependent on placement and routing, which itself is a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 real-world designs.</p> <p>Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design.</p>
Block	<p>Represents the power dissipation due to internal and load toggling of the I/O.</p> <p>Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact I/O configuration of your design.</p>
Total	Represents the total power dissipation. The total power dissipation is the sum of the routing and block power.
$I_{CCINT}$	Represents the current drawn from the $I_{CCINT}$ rail. Powers internal digital circuitry and routing.
$I_{CCIO}$	Represents the current drawn from this bank's $V_{CCIO}$ rail.
User Comment	Enter any comments (optional entry).

## Other Input Information

There are three other buttons below the input parameters section: Set Toggle %, Reset, and Import Quartus File, as shown in [Figure 17-12](#).

**Figure 17-12.** The Three Buttons



### Set Toggle %

Sets the toggle rate for the Logic Module and I/O Module.

## Reset

Clears all input values in the PowerPlay Early Power Estimator spreadsheet.

## Importing the Quartus II Early Power Estimator File

If you have created the user design, you can use the Quartus II software to generate the PowerPlay Early Power Estimator file and then import this file into the PowerPlay Early Power Estimator spreadsheet. This power estimation report file contains the device resource information and importing this file saves you time and effort otherwise spent manually entering information into the PowerPlay Early Power Estimator spreadsheet. You can manually change any of the values after importing the file.

To generate the PowerPlay Early Power Estimator file, first compile your design in the Quartus II software. After that, on the Project menu, click **Generate PowerPlay Early Power Estimator File**. The Quartus II software creates a PowerPlay Early Power Estimator file with the name <revision name>\_early\_pwr.csv.



For more information about generating the PowerPlay Early Power Estimator file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

To import data into the PowerPlay Early Power Estimator spreadsheet, perform the following steps:

1. Click **Import Quartus File** in the PowerPlay Early Power Estimator spreadsheet.
2. Browse to a power estimation file generated from the Quartus II software. Click **OK**.

Clicking **OK** clears any user-entered values in the PowerPlay Early Power Estimator spreadsheet and populates the PowerPlay Early Power Estimator spreadsheet with device resource information from the specified power estimation file.

After importing a file, manually specify some of the input parameters in the main section. These input parameters include:

- $V_{CCINT}$  supply voltage
- Ambient temperature
- Airflow

The ambient temperature and airflow are used for thermal analysis only. Refer to the input parameters section for more information on these parameters.

The clock frequency values imported into PowerPlay Early Power Estimator Clock Domain, Logic, and I/O modules are the same as the  $f_{MAX}$  values of the design. You can manually edit the clock frequency and the toggle percentage in the PowerPlay Early Power Estimator spreadsheet to suit your system requirements.

## Power Estimation Summary

The main worksheet of the PowerPlay Early Power Estimator spreadsheet summarizes the power and current estimates for the design. It displays the total power, thermal analysis, and power supply current information. The accuracy of the information depends on the information entered. The power consumed can also vary greatly depending on the toggle rates entered. The following sections provide a description of the results of the PowerPlay Early Power Estimator spreadsheet.

### Power

This section shows the power dissipated in the MAX II device. The total thermal power is shown in mWatts and is a sum of the thermal power of all the resources being used in the device. The total thermal power includes the typical power from standby and dynamic power. Figure 17-13 shows the Power section.

Figure 17-13. Power Section

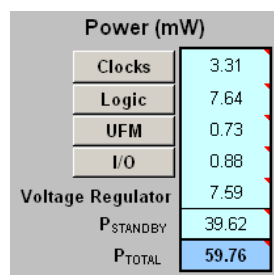


Table 17-7 describes the thermal power parameters in the PowerPlay Early Power Estimator spreadsheet.

Table 17-7. Power Information

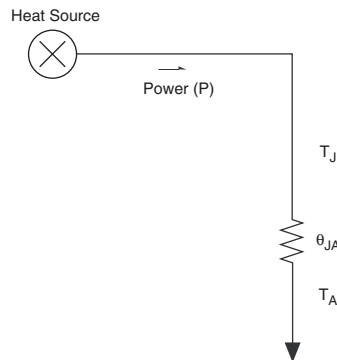
Column Heading	Description
Clock	Represents the dynamic power consumed by clock networks. Click <b>Clocks</b> for details.
Logic	Represents the dynamic power consumed by LEs and associated routing. Click <b>Logic</b> for details.
UFM	Represents the dynamic power consumed by the <b>UFM</b> block. Click <b>UFM</b> for details.
I/O	Represents the dynamic power consumed by I/O pins and associated routing. Click <b>I/O</b> for details.
Voltage Regulator	Represents the dynamic power consumed by the on-chip voltage regulator for a device that supports 2.5-V/3.3-V $V_{CCINT}$ .
P <sub>STANDBY</sub>	Represents the standby/static power consumed irrespective of clock frequency. The value includes static power consumed by the I/O banks and the voltage regulator. P <sub>STANDBY</sub> is dependent on the selected device and the $V_{CCINT}$ supply voltage.
P <sub>TOTAL</sub>	Represents the total power consumed by the CPLD. Refer to “Power Supply Current” on page 17-15 for the current draw from the CPLD supply rails.

## Thermal Analysis

In the Thermal Analysis part, the PowerPlay Early Power Estimator spreadsheet considers the device's ambient temperature and the airflow to determine the junction temperature ( $T_J$ ) of the device in °C.

The device can be considered a heat source and the junction temperature is the temperature at the device. The thermal resistance of the path is referred to as the junction-to-ambient thermal resistance ( $\theta_{JA}$ ). Figure 17-14 shows the thermal model for the PowerPlay Early Power Estimator spreadsheet.

**Figure 17-14.** Thermal Model for the PowerPlay Early Power Estimator



The PowerPlay Early Power Estimator spreadsheet determines the junction-to-ambient thermal resistance ( $\theta_{JA}$ ) based on the device, package, and airflow selected in the main input parameters.

The PowerPlay Early Power Estimator spreadsheet calculates the total power based on the device properties which provide  $\theta_{JA}$  and the ambient and junction temperature using the following equation:

**Equation 17-1.**

$$P = \frac{T_J - T_A}{\theta_{JA}}$$

Figure 17-15 shows the Thermal Analysis section and Table 17-8 describes the thermal analysis parameters in the PowerPlay Early Power Estimator spreadsheet.

**Figure 17-15.** Thermal Analysis Section

Thermal Analysis	
Junction Temp, $T_J$ (°C)	27.4
$\theta_{JA}$ Junction-Ambient	39.50
Maximum Allowed $T_A$ (°C)	82.6

**Table 17-8.** Thermal Analysis Information

Column Heading	Description
Junction Temp, $T_J$ (°C)	Represents the estimated device junction temperature.
$\theta_{JA}$ Junction-Ambient	Represents the junction-to-ambient thermal resistance through the top of the device (°C/W).
Maximum Allowed $T_A$ (°C)	Represents a guideline for the maximum ambient temperature (°C) that the device can be subjected to without violating maximum junction temperature.

## Power Supply Current

The power supply current provides the estimated current consumption for power supplies. The  $I_{CCPOWERUP}$  is only applicable during power up when the configuration flash memory (CFM) block downloads to the SRAM. The  $I_{CCINT}$  current is the supply current required from  $V_{CCINT}$ . The total  $I_{CCIO}$  current is the supply current required from  $V_{CCIO}$  for all I/O banks. For estimates of  $I_{CCIO}$  based on I/O banks, refer to the “I/O Section” on page 17-8 of the PowerPlay Early Power Estimator spreadsheet. Figure 17-16 shows the Power Supply Current section.

**Figure 17-16.** Power Supply Current



Table 17-9 describes the Power Supply Current parameters of the PowerPlay Early Power Estimator spreadsheet.

**Table 17-9.** Power Supply Current Information


Column Heading	Description
$I_{CCPOWERUP}$	Represents the maximum current drawn during power-up.
$I_{CCINT}$	Represents the total current drawn from the $I_{CCINT}$ supply.
$I_{CCIO}$	Represents the total current drawn from the $I_{CCIO}$ power rail(s). Refer to the “I/O Section” on page 17-8 for details about the current drawn from each I/O rail.

## Power Saving Techniques

The following guidelines reduce power consumption for an application:

- Slow the operation in portions of the circuit.  $I_{CC}$  is proportional to the frequency of operation. Slowing parts of a circuit lowers the  $I_{CC}$  and therefore reduces the power. MAX II devices provide global or array clock source for all registers. Signals that do not require high-speed operation can use a slower array clock that reduces the system power consumption.
- Reduce the number of outputs. Standby and dynamic current are required to support all I/O pins on the device. Reducing the number of I/O pins can reduce current necessary for the device, and thereby reduce the power.

- Reduce the loading and/or external capacitance on the outputs. Excessive loading and capacitance of printed circuit board (PCB) traces and other ICs on the output pins significantly increases the power. Keeping excess load and external capacitance to a minimum on the outputs pins whenever possible will significantly reduce the current necessary for the device.
- Reduce the amount of circuitry in the device. Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device and thus reduces the power.
- Modify the design to reduce power. Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant unnecessary signals.
- Modify I/O Locations. Grouping I/O pins from common logic blocks allows the Quartus II software to place the associated logic closer together. The more compact a logic block and I/O, the lower its dynamic power (especially true of low utilization designs with I/O spread around the device).
- Increase the performance requirements in the constraint file. Improving the performance that is beyond the need for operation reduces the power dissipation. The Quartus II software optimizes the design and places logic closer together, uses shorter routing and fewer logic levels, and lowers dynamic power and improves performance.

 MAX II devices offer a power-down capability that conserves battery life for portable applications. For more information about the power-down capability in MAX II devices and an application design example, refer to *AN 422: Power Management in Portable Systems Using MAX II CPLDs*.

## Conclusion

This chapter discusses how to evaluate and manage MAX II power by using the MAX II PowerPlay Early Power Estimator spreadsheet. This power estimation tool estimates the power consumption for your design based on typical conditions. The MAX II board-level designer can exploit the power calculator before board design and layout. The MAX II PowerPlay Early Power Estimator spreadsheet is available on the Altera website at [www.altera.com](http://www.altera.com).

## Referenced Documents

This chapter references the following documents:

- *AN 422: Power Management in Portable Systems Using MAX II CPLDs*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*

## Document Revision History

Table 17-10 shows the revision history for this chapter.

**Table 17-10.** Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.1	<ul style="list-style-type: none"> <li>■ Updated New Document Format.</li> </ul>	—
December 2007, version 2.0	<ul style="list-style-type: none"> <li>■ Updated Figure 17-1, Figure 17-2, and Figure 17-3.</li> <li>■ Updated Table 17-1 with information about power characteristics.</li> <li>■ Updated Table 17-2, Table 17-3, and Table 17-6.</li> <li>■ Added "Referenced Documents" section.</li> </ul>	Updated document with MAX IIZ information.
December 2006, version 1.5	<ul style="list-style-type: none"> <li>■ Added document revision history.</li> </ul>	—
July 2006, version 1.4	<ul style="list-style-type: none"> <li>■ Minor content update.</li> </ul>	—
August 2005, version 1.3	<ul style="list-style-type: none"> <li>■ Updated the entire <i>MAX II Power Estimation Using the PowerPlay Early Power Estimator</i> section.</li> </ul>	—
January 2005, version 1.2	<ul style="list-style-type: none"> <li>■ Previously published as Chapter 18. No changes to content.</li> </ul>	—
December 2004, version 1.1	<ul style="list-style-type: none"> <li>■ Added Excel Macro, General I/O AC Power, and General I/O DC Power sections.</li> <li>■ Updated figures.</li> <li>■ Updated Table 17-1.</li> </ul>	—