


## Core Overview

The Avalon® Streaming (Avalon-ST) Bytes to Packets and Packets to Bytes Converter cores allow an arbitrary stream of packets to be carried over a byte interface, by encoding packet-related control signals such as `startofpacket` and `endofpacket` into byte sequences. The Avalon-ST Packets to Bytes Converter core encodes packet control and payload as a stream of bytes. The Avalon-ST Bytes to Packets Converter core accepts an encoded stream of bytes, and converts it into a stream of packets.

 The SPI Slave to Avalon Master Bridge and JTAG to Avalon Master Bridge are examples of how the cores are used. For more information about the bridge, refer to the *SPI Slave/JTAG to Avalon Master Bridge Cores chapter* in volume 5 of the *Quartus II Handbook*.

Both of these cores are SOPC Builder-ready and integrate easily into any SOPC Builder-generated system.

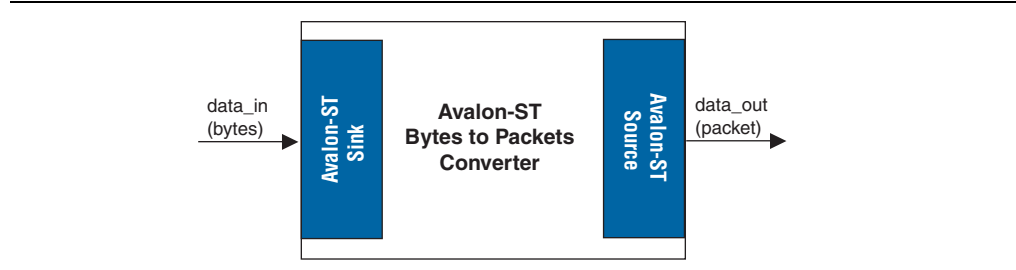
This chapter contains the following sections:

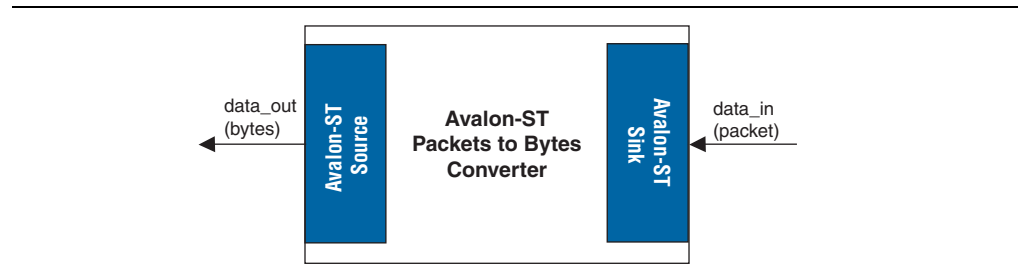
- “Functional Description”
- “Instantiating the Core in SOPC Builder” on page 18–3
- “Device Support” on page 18–4

## Functional Description

Figure 18–1 and Figure 18–2 show block diagrams of the Avalon-ST Bytes to Packets and Packets to Bytes Converter cores.

**Figure 18–1.** Avalon-ST Bytes to Packets Converter Core



**Figure 18-2.** Avalon-ST Packets to Bytes Converter Core

## Interfaces

Table 18-1 shows the properties of the Avalon-ST interfaces.

**Table 18-1.** Properties of Avalon-ST Interfaces

Feature	Property
Backpressure	Ready latency = 0.
Data Width	Data width = 8 bits; Bits per symbol = 8.
Channel	Supported, up to 255 channels.
Error	Not used.
Packet	Supported only on the Avalon-ST Bytes to Packet Converter core's source interface and the Avalon-ST Packet to Bytes Converter core's sink interface.



For more information about Avalon-ST interfaces, refer to the [Avalon Interface Specifications](#).

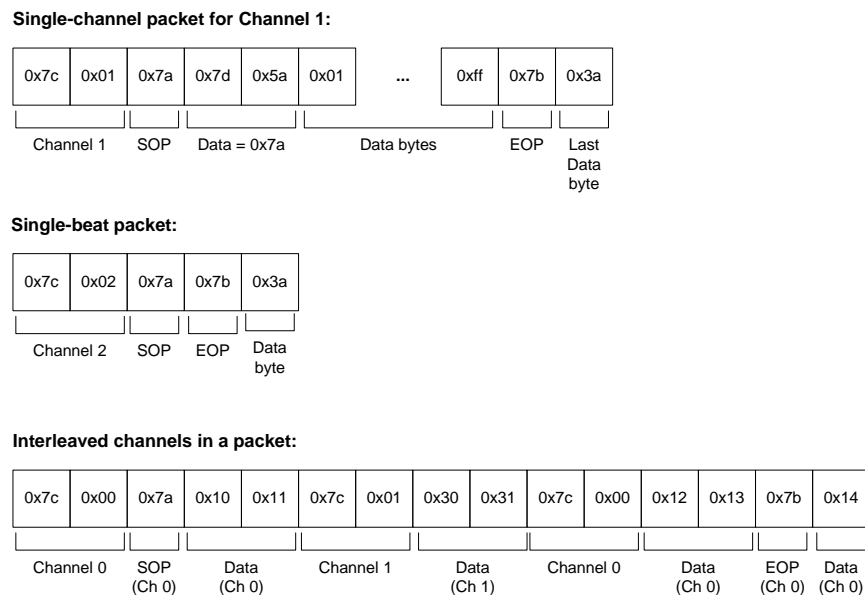
## Operation—Avalon-ST Bytes to Packets Converter Core

The Avalon-ST Bytes to Packets Converter core receives streams of bytes and transforms them into packets. When parsing incoming bytestreams, the core decodes special characters in the following manner, with higher priority operations listed first:

- Escape (0x7d)—The core drops the byte. The next byte is XORed with 0x20.
- Start of packet (0x7a)—The core drops the byte and marks the next payload byte as the start of a packet by asserting the `startofpacket` signal on the Avalon-ST source interface.
- End of packet (0x7b)—The core drops the byte and marks the following byte as the end of a packet by asserting the `endofpacket` signal on the Avalon-ST source interface. For single beat packets, both the `startofpacket` and `endofpacket` signals are asserted in the same clock cycle.
- Channel number indicator (0x7c)—The core drops the byte and takes the next non-special character as the channel number.

Figure 18-3 shows examples of bytestreams.

**Figure 18-3.** Examples of Bytestreams



## Operation—Avalon-ST Packets to Bytes Converter Core

The Avalon-ST Packets to Bytes Converter core receives packetized data and transforms the packets to bytestreams. The core constructs outgoing bytestreams by inserting appropriate special characters in the following manner and sequence:

- If the `startofpacket` signal on the core's source interface is asserted, the core inserts the following special characters:
  - Channel number indicator (0x7c).
  - Channel number, escaping it if required.
  - Start of packet (0x7a).
- If the `endofpacket` signal on the core's source interface is asserted, the core inserts an end of packet (0x7b) before the last byte of data.
- If the `channel` signal on the core's source interface changes to a new value within a packet, the core inserts a channel number indicator (0x7c) followed by the new channel number.
- If a data byte is a special character, the core inserts an escape (0x7d) followed by the data XORed with 0x20.

## Instantiating the Core in SOPC Builder

Use the MegaWizard™ interface for the Avalon-ST Bytes to Packets and Packets to Bytes Converter cores in SOPC Builder to add the core to a system. There are no user-configurable parameters for this core.

## Device Support

The Avalon-ST Bytes to Packets and Packets to Bytes Converter cores support all Altera device families.

## Referenced Documents

This chapter references *Avalon Interface Specifications*.

## Document Revision History

Table 18-2 shows the revision history for this chapter.

**Table 18-2.** Document Revision History

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
November 2009 v9.1.0	No change from previous release.	—
March 2009 v9.0.0	No change from previous release.	—
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size. No change to content.	—
May 2008 v8.0.0	Initial release.	—