

## Core Overview

Avalon® Streaming (Avalon-ST) components in SOPC Builder provide a channel interface to stream data from multiple channels into a single component. In a multi-channel Avalon-ST component that stores data, the component can store data either in the sequence that it comes in (FIFO) or in segments according to the channel. When data is stored in segments according to channels, a scheduler is needed to schedule the read operations from that particular component. The most basic of the schedulers is the Avalon-ST Round Robin Scheduler core.

The Avalon-ST Round Robin Scheduler core is SOPC Builder-ready and can integrate easily into any SOPC Builder-generated systems.

This chapter contains the following sections:

- “Performance and Resource Utilization”
- “Functional Description” on page 20–2
- “Instantiating the Core in SOPC Builder” on page 20–4
- “Device Support” on page 20–4

## Performance and Resource Utilization

This section lists the resource utilization and performance data for various Altera® device families. The estimates are obtained by compiling the core using the Quartus® II software.

Table 20–1 shows the resource utilization and performance data for a Stratix® II GX device (EP2SGX130GF1508I4).

**Table 20–1.** Resource Utilization and Performance Data for Stratix II GX Devices

Number of Channels	ALUTs	Logic Registers	Memory M512/M4K/M-RAM	f <sub>MAX</sub> (MHz)
4	7	7	0/0/0	> 125
12	25	17	0/0/0	> 125
24	62	30	0/0/0	> 125

Table 20–2 shows the resource utilization and performance data for a Stratix III device (EP3SL340F1760C3). The performance of the MegaCore® function in Stratix IV devices is similar to Stratix III devices.

**Table 20-2.** Resource Utilization and Performance Data for Stratix III Devices

Number of Channels	ALUTs	Logic Registers	Memory M9K/M144K/MLAB	f <sub>MAX</sub> (MHz)
4	7	7	0/0/0	> 125
12	25	17	0/0/0	> 125
24	67	30	0/0/0	> 125

Table 20-3 shows the resource utilization and performance data for a Cyclone® III device (EP3C120F780I7).

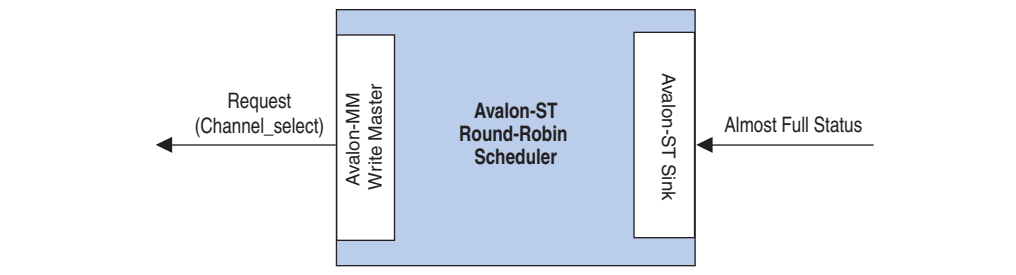
**Table 20-3.** Resource Utilization and Performance Data for Cyclone III Devices

Number of Channels	Total Logic Elements	Total Registers	Memory M9K	f <sub>MAX</sub> (MHz)
4	12	7	0	> 125
12	32	17	0	> 125
24	71	30	0	> 125

## Functional Description

The Avalon-ST Round Robin Scheduler core controls the read operations from a multi-channel Avalon-ST component that buffers data by channels. It reads the almost-full threshold values from the multiple channels in the multi-channel component and issues the read request to the Avalon-ST source according to a round-robin scheduling algorithm.

Figure 20-1 shows the block diagram of the Avalon-ST Round Robin Scheduler.

**Figure 20-1.** Avalon-ST Round Robin Scheduler Block Diagram

## Interfaces

The following interfaces are available in the Avalon-ST Round Robin Scheduler core:

- Almost-Full Status Interface
- Request Interface

### Almost-Full Status Interface

The Almost-Full Status interface is an Avalon-ST sink interface. Table 20-4 describes the almost-full interface.

**Table 20-4.** Avalon-ST Interface Feature Support

Feature	Property
Backpressure	Not supported
Data Width	Data width = 1; Bits per symbol = 1
Channel	Maximum channel = 32; Channel width = 5
Error	Not supported
Packet	Not supported

The interface collects the almost-full status from the sink components for all the channels in the sequence provided.

### Request Interface

The Request Interface is an Avalon Memory-Mapped (MM) Write Master interface. This interface requests data from a specific channel. The Avalon-ST Round Robin Scheduler core cycles through all of the channels it supports and schedules data to be read.

## Operations

If a particular channel is almost full, the Avalon-ST Round Robin Scheduler will not schedule data to be read from that channel in the source component.

The Avalon-ST Round Robin Scheduler only requests 1 beat of data from a channel at each transaction. To request 1 beat of data from channel  $n$ , the scheduler writes the value 1 to address  $(4 \times n)$ . For example, if the scheduler is requesting data from channel 3, the scheduler writes 1 to address  $0xC$ .

At every clock cycle, the Avalon-ST Round Robin Scheduler requests data from the next channel. Therefore, if the Avalon-ST Round Robin Scheduler starts requesting from channel 1, at the next clock cycle, it requests from channel 2. The Avalon-ST Round Robin Scheduler does not request data from a particular channel if the almost-full status for the channel is asserted. In this case, one clock cycle is used without a request transaction.

The Avalon-ST Round Robin Scheduler cannot determine if the requested component is able to service the request transaction. The component asserts `waitrequest` when it cannot accept new requests.

Table 20-5 shows the list of ports for the Avalon-ST Round Robin Scheduler core:

**Table 20-5.** Ports for the Avalon-ST Round Robin Scheduler (Part 1 of 2)

Signal	Direction	Description
<b>Clock and Reset</b>		
<code>clk</code>	In	Clock reference.
<code>reset_n</code>	In	Asynchronous active low reset.
<b>Avalon-MM Request Interface</b>		
<code>request_address</code> ( $\log_2$ Max_Channels-1:0)	Out	The write address used to signal the channel the request is for.
<code>request_write</code>	Out	Write enable signal.

**Table 20-5.** Ports for the Avalon-ST Round Robin Scheduler (Part 2 of 2)

Signal	Direction	Description
request_writedata	Out	The amount of data requested from the particular channel. This value is always fixed at 1.
request_waitrequest	In	Wait request signal, used to pause the scheduler when the slave cannot accept a new request.
<b>Avalon-ST Almost-Full Status Interface</b>		
almost_full_valid	In	Indicates that almost_full_channel and almost_full_data are valid.
almost_full_channel (Channel_Width-1:0)	In	Indicates the channel for the current status indication.
almost_full_data (log <sub>2</sub> Max_Channels-1:0)	In	A 1-bit signal that is asserted high to indicate that the channel indicated by almost_full_channel is almost full.

## Instantiating the Core in SOPC Builder

Use the MegaWizard™ interface for the Avalon-ST Round Robin Scheduler core in SOPC Builder to specify the core's configuration. [Table 20-6](#) describes the parameters that can be configured for the Avalon-ST Round Robin Scheduler component.

**Table 20-6.** Parameters for Avalon-ST Round Robin Scheduler Component

Parameters	Values	Description
<b>Number of channels</b>	2-32	Specifies the number of channels the Avalon-ST Round Robin Scheduler supports.
<b>Use almost-full status</b>	0-1	Specifies whether the almost-full interface is used. If the interface is not used, the core always requests data from the next channel at the next clock cycle.

## Device Support

The Avalon-ST Round Robin Scheduler core supports all Altera device families.

## Document Revision History

[Table 20-7](#) shows the revision history for this chapter.

**Table 20-7.** Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	No change from previous release.	—
March 2009 v9.0.0	No change from previous release.	—

**Table 20–7.** Document Revision History

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size. No change to content.	—
May 2008 v8.0.0	Initial release.	—

