

This chapter addresses how the Quartus® II software interacts with the Cadence Allegro Design Entry HDL software and the Cadence Allegro Design Entry CIS (Component Information System) software (also known as OrCAD Capture CIS) to provide a complete FPGA-to-board integration design workflow.

Introduction

With today's large, high-pin-count and high-speed FPGA devices, good PCB design practices are essential to ensure the correct operation of your system. The PCB design takes place concurrently with the design and programming of the FPGA. An FPGA or ASIC designer initially creates the signal and pin assignments and the board designer must correctly transfer these assignments to the symbols used in their system circuit schematics and board layout. As the board design progresses, pin reassignments are required to optimize the layout. Pin reassignments must be relayed to the FPGA designer to ensure the new assignments can be processed through the FPGA with updated placement and routing.


This chapter provides information about the following topics:


- Cadence tool description, history, and comparison.
- The general design flow between the Quartus II software and the Cadence Allegro Design Entry HDL software and the Cadence Allegro Design Entry CIS software.
- Generating schematic symbols from your FPGA design for use in the Cadence Allegro Design Entry HDL software.
- Updating Design Entry HDL symbols when signal and pin assignment changes are made in the Quartus II software.
- Creating schematic symbols in the Cadence Allegro Design Entry CIS software from your FPGA design.
- Updating symbols in the Cadence Allegro Design Entry CIS software when signal and pin assignment changes are made in the Quartus II software.
- Using Altera-provided device libraries in the Cadence Allegro Design Entry CIS software.

This chapter is intended for board design and layout engineers who want to begin the FPGA board integration process while the FPGA is still in the design phase. Part librarians can also benefit from this chapter by learning the method to use output from the Quartus II software to create new library parts and symbols.


The procedures in this chapter require the following software:

- The Quartus II software version 5.1 or later
- The Cadence Allegro Design Entry HDL software or the Cadence Allegro Design Entry CIS software version 15.2 or later
- The OrCAD Capture software with the optional CIS option version 10.3 or later (optional)

 Because the Cadence Allegro Design Entry CIS software is based on the OrCAD Capture software, these programs are very similar. This chapter refers to the Cadence Allegro Design Entry CIS software; however, any procedural information can also apply to the OrCAD Capture software unless otherwise noted.

 For more information about obtaining and licensing the Cadence tools and for product information, support, and training, refer to the Cadence website (www.cadence.com).

 For more information about the OrCAD Capture software and the CIS option, refer to the Cadence website (www.cadence.com).

 For more information about Cadence and OrCAD support and training, refer to the EMA Design Automation website (www.ema-eda.com).

Product Comparison

The Cadence and OrCAD design tools have similar functionality, but there are differences both in their function and location of product information. Table 9-1 lists the Cadence and OrCAD products described in this chapter and provides information about changes, product information, and support.

Table 9-1. Cadence and OrCAD Product Comparison

	Cadence Allegro Design Entry HDL	Cadence Allegro Design Entry CIS	OrCAD Capture CIS
Former Name	Concept HDL Expert	Capture CIS Studio	—
History	More commonly known by its former name, Cadence renamed all board design tools in 2004 under the Allegro name.	Based directly on OrCAD Capture CIS, the Cadence Allegro Design Entry CIS software is still developed by OrCAD but sold and marketed by Cadence. EMA provides support and training.	The basis for Design Entry CIS is still developed by OrCAD for continued use by existing OrCAD customers. EMA provides support and training for all OrCAD products.
Vendor Design Flow	Cadence Allegro 600 series, formerly known as the Expert Series, for high-end, high-speed design.	Cadence Allegro 200 series, formerly known as the Studio Series, for small- to medium-level design.	—
Information and Support	www.cadence.com www.ema-eda.com	www.cadence.com www.ema-eda.com	www.cadence.com www.ema-eda.com

FPGA-to-PCB Design Flow

You can create a design flow integrating an Altera FPGA design from the Quartus II software through a circuit schematic in the Cadence Allegro Design Entry HDL software or the Cadence Allegro Design Entry CIS software. Figure 9-1 shows the design flow with the Cadence Allegro Design Entry HDL software. Figure 9-2 shows the design flow with the Cadence Allegro Design Entry CIS software.

Figure 9-1. Design Flow with the Cadence Allegro Design Entry HDL Software

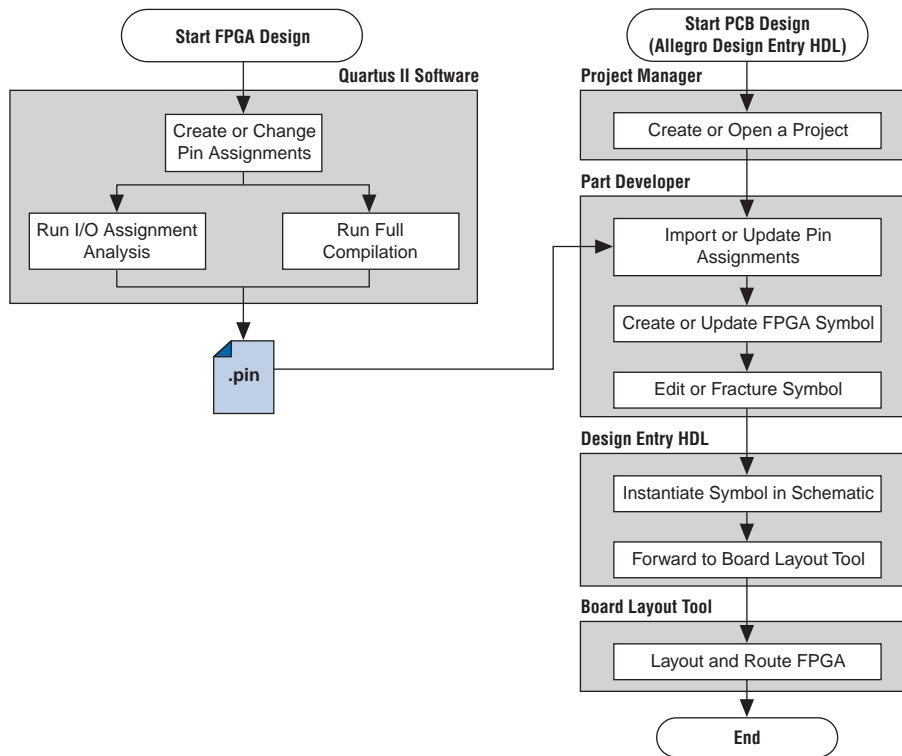


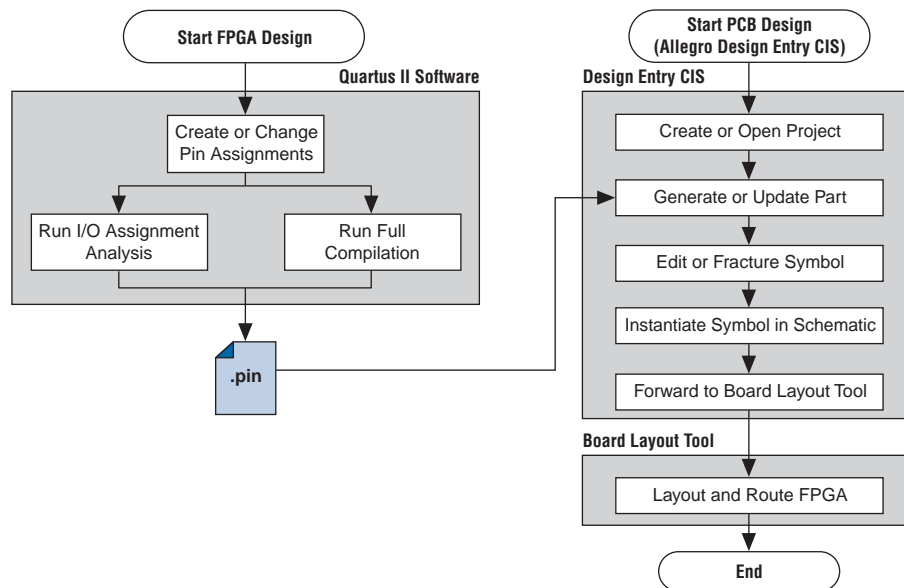
Figure 9-2. Design Flow with the Cadence Allegro Design Entry CIS Software

Figure 9-1 and Figure 9-2 show the possible design flows, depending on your tool choice. The Cadence PCB Librarian Expert license is required to use the Cadence Allegro PCB Librarian Part Developer tool to create FPGA symbols. You can update symbols with changes made to the FPGA design using any of these tools.

To integrate an Altera FPGA design starting in the Quartus II software through to a circuit schematic in the Cadence Allegro Design Entry HDL software or the Cadence Allegro Design Entry CIS software, perform the following steps:

1. In the Quartus II software, compile your design to generate a Pin-Out File (.pin) to transfer the assignments to the Cadence software.
2. If you are using the Cadence Allegro Design Entry HDL software for your schematic design, perform the following steps:
 - a. Open an existing project or create a new project in the Cadence Allegro Project Manager tool.
 - b. Construct a new symbol or update an existing symbol using the Cadence Allegro PCB Librarian Part Developer tool.
 - c. With the Cadence Allegro PCB Librarian Part Developer tool, edit your symbol or fracture it into smaller parts (optional).
 - d. Instantiate the symbol in your Cadence Allegro Design Entry HDL software schematic and transfer the design to your board layout tool.

–or

If you are using the Cadence Allegro Design Entry CIS software for your schematic design, perform the following steps:

- a. Generate a new part in a new or existing Cadence Allegro Design Entry CIS project, referencing the **.pin** output from the Quartus II software. You can also update an existing symbol with a new **.pin**.
- b. Split the symbol into smaller parts as necessary.
- c. Instantiate the symbol in your Cadence Allegro Design Entry CIS schematic and transfer the design to your board layout tool.

Performing Simultaneous Switching Noise (SSN) Analysis of Your FPGA

With the Quartus II software version 9.0 and later, you can extract pin assignment data and perform SSN analysis of your FPGA design for the designs that target Stratix III device family. You can perform SSN analysis to analyze SSN in your FPGA device early in the board layout stage as part of your overall pin planning process, however you do not have to perform SSN analysis to generate pin assignment data from the Quartus II software. You can use the SSN Analyzer tool in the Quartus II software to optimize the pin assignments for better SSN performance of your FPGA device.



To get the latest information on device support for the SSN Analyzer, refer to the Quartus II Help.

For more information about the SSN Analyzer, refer to the *Simultaneous Switching Noise (SSN) Analysis and Optimizations* chapter in volume 2 of the *Quartus II Handbook*.

Setting Up the Quartus II Software

You can transfer pin and signal assignments from the Quartus II software to the Cadence design tools by generating the Quartus II project **.pin**. The **.pin** is an output file generated by the Quartus II Fitter that contains pin assignment information. You can use the Quartus II Pin Planner to set and change the assignments contained in the **.pin** and then transfer the assignments to the Cadence design tools. You cannot, however, import pin assignment changes from the Cadence design tools into the Quartus II software with the **.pin**.

The **.pin** lists all used and unused pins on your selected Altera device. It also provides the following basic information fields for each assigned pin on the device:

- Pin signal name and usage
- Pin number
- Signal direction
- I/O standard
- Voltage
- I/O bank
- User or Fitter-assigned

- For more information about using the Quartus II Pin Planner to create or change pin assignment details, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.


Generating a .pin

The **.pin** is automatically generated by the Quartus II Fitter during a full compilation of your FPGA design, or when you run I/O assignment analysis on the design. The **.pin** is located in your Quartus II project directory with the name *<project name>.pin*.

- For more information about pin and signal assignment transfer and the files that the Quartus II software can import and export, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

FPGA-to-Board Integration with the Cadence Allegro Design Entry HDL Software

The Cadence Allegro Design Entry HDL software is a high-end schematic capture tool that is part of the Cadence 600 series design flow. Use the Cadence Allegro Design Entry HDL software to create flat circuit schematics for all types of PCB design. The Cadence Allegro Design Entry HDL software can also create hierarchical schematics to facilitate design reuse and team-based design. With the Cadence Allegro Design Entry HDL software, the design flow from FPGA-to-board is one-way, using only the **.pin** generated by the Quartus II software. Signal and pin assignment changes can only be made in the Quartus II software and are reflected in updated symbols in a Cadence Allegro Design Entry HDL project. For more information about the design flow with the Cadence Allegro Design Entry HDL software, refer to [Figure 9-1 on page 9-3](#).


-  Routing or pin assignment changes made in a board layout tool or a Cadence Allegro Design Entry HDL software symbol cannot be back-annotated to the Quartus II software.
- For more information about the Cadence Allegro Design Entry HDL software and the Cadence Allegro PCB Librarian Part Developer tool, including licensing, support, usage, training, and product updates, refer to the Help in the software or to the Cadence website (www.cadence.com).

Symbol Creation

In addition to circuit simulation, circuit board schematic creation is one of the first tasks required in the design of a new PCB. Schematics are required to understand how the PCB works, and to generate a netlist that is passed on to a board layout tool for board design and routing. The Cadence Allegro PCB Librarian Part Developer tool allows you to create schematic symbols based on FPGA designs exported from the Quartus II software.

You can create symbols for the Cadence Allegro Design Entry HDL project with the Cadence Allegro PCB Librarian Part Developer tool, which is available in the Cadence Allegro Project Manager tool. Altera recommends using the Cadence Allegro PCB Librarian Part Developer tool to import FPGA designs into the Cadence Allegro Design Entry HDL software.

You must have a PCB Librarian Expert license from Cadence to run the Cadence Allegro PCB Librarian Part Developer tool. The Cadence Allegro PCB Librarian Part Developer tool provides a GUI with many options for creating, editing, fracturing, and updating symbols. If you do not use the Cadence Allegro PCB Librarian Part Developer tool, you must create and edit symbols manually in the Symbol Schematic View in the Cadence Allegro Design Entry HDL software.

 If you do not have a PCB Librarian Expert license, you can automatically create FPGA symbols using the programmable IC (PIC) design flow found in the Cadence Allegro Project Manager tool. For more information about using the PIC design flow, refer to the Help in the Cadence design tools, or go to the Cadence website (www.cadence.com).

Before you can create a symbol from an FPGA design, you must first open a Cadence Allegro Design Entry HDL project with the Cadence Allegro Project Manager tool. If you do not have an existing Cadence Allegro Design Entry HDL project, you can create one with the Cadence Allegro Design Entry HDL software. Cadence Allegro Design Entry HDL projects are stored in your Cadence Allegro Design Entry HDL project directory with the name *<project name>.cpm*.

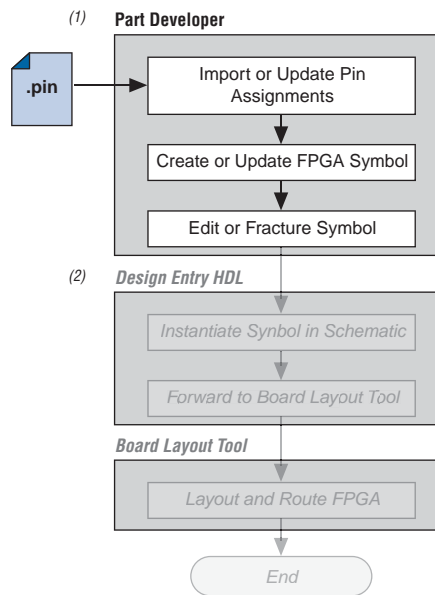
While the Cadence Allegro PCB Librarian Part Developer tool refers to symbol fractures as slots, the other tools described in this chapter use different names to refer to symbol fractures. Table 9-2 lists the symbol fracture naming conventions for each of the tools addressed in this chapter.

Table 9-2. Symbol Fracture Naming

	Cadence Allegro PCB Librarian Part Developer Tool	Cadence Allegro Design Entry HDL Software	Cadence Allegro Design Entry CIS Software
During symbol generation	Slots	—	Sections
During symbol schematic instantiation	—	Versions	Parts

Cadence Allegro PCB Librarian Part Developer Tool

You can create, fracture, and edit schematic symbols for your designs using the Cadence Allegro PCB Librarian Part Developer tool. Most devices are physically large with hundreds of pins, requiring large schematic symbols that might not fit on a single schematic page. Symbols designed in the Cadence Allegro PCB Librarian Part Developer tool can be split or fractured into several functional blocks called slots, allowing multiple smaller part fractures to exist on the same schematic page or across multiple pages. Figure 9-3 shows how the Cadence Allegro PCB Librarian Part Developer tool fits into the design flow.

Figure 9-3. Cadence Allegro PCB Librarian Part Developer Tool in the Design Flow**Notes to Figure 9-3:**

- (1) For more information about the full design flow flowchart, refer to [Figure 9-1 on page 9-3](#).
- (2) Grayed out steps are not part of the FPGA symbol creation or update process.

To run the Cadence Allegro PCB Librarian Part Developer tool, you must have a Cadence Allegro Design Entry HDL project open in the Cadence Allegro Project Manager tool. To open the Cadence Allegro PCB Librarian Part Developer tool, on the Flows menu, click **Library Management**, and then click **Part Developer**.

Import and Export Wizard

After starting the Cadence Allegro PCB Librarian Part Developer tool, use the **Import and Export** wizard to import your pin assignments from the Quartus II software. To access the Import and Export wizard, perform the following steps:

1. On the File menu, click **Import and Export**.



You will receive an error message from the Cadence Allegro PCB Librarian Part Developer tool when you open the **Import and Export** wizard if you are not using your PCB Librarian Expert license file. To point to your PCB Librarian Expert license file, on the File menu, click **Change Product** and then select the correct product license.

2. Select **Import ECO-FPGA**, and then click **Next**.

3. In the **Select Source** page of the **Import and Export** wizard, make the following settings:
 - a. In the **Vendor** list, select **Altera**.
 - b. In the **PnR Tool** list, select **quartusII**.
 - c. In the **PR File** box, browse to select the **.pin** in your Quartus II project directory.
 - d. Click **Simulation Options** to select simulation input files.
 - e. Click **Next**.
4. In the **Select Destination** dialog box, make the following settings:
 - a. Under **Select Component**, click **Generate Custom Component** to create a new component in a library,
–or
 - b. Click **Use standard component** to base your symbol on an existing component.



Altera recommends creating a new component if you previously created generic component for an FPGA device. Generic components can cause some problem with your design. When you create a new component you can place your pin and signal assignments from the Quartus II software on this component and reuse the component as a base when you have a new FPGA design.

- c. In the **Library** list, select an existing library. You can select from the cells contained in the selected library. Each cell represents all the symbol versions and part fractures for that particular part. In the **Cell** list, select the existing cell to use as a base for your part.
- d. In the **Destination Library** list, select a destination library for the component. Click **Next**.
- e. Review and edit the assignments you are importing into the Cadence Allegro PCB Librarian Part Developer tool based on the data in the **.pin** and then click **Finish**. The location of each pin is not included in the **Preview of Import Data** page of the **Import and Export** wizard, but input pins are placed on the left side of the created symbol, output pins on the right, power pins on the top, and ground pins on the bottom.

Edit and Fracture Symbol

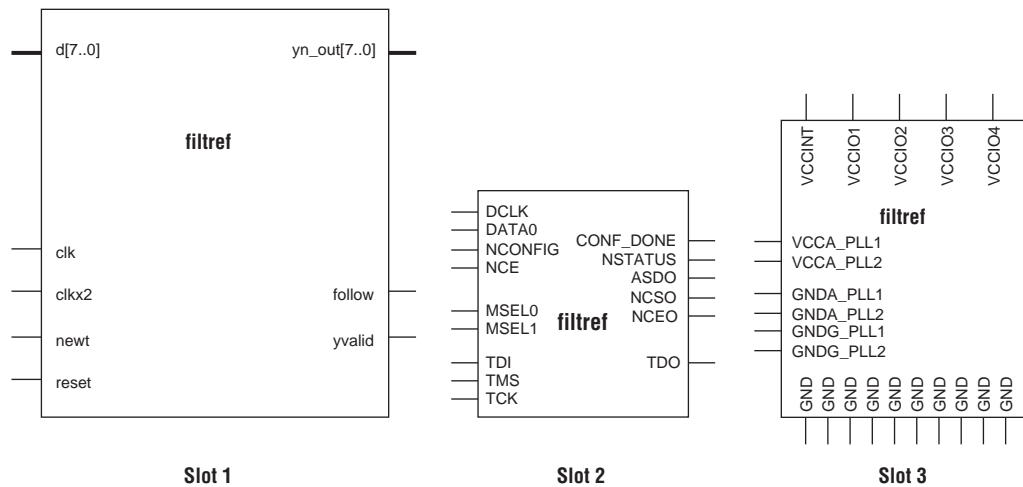
After creating your new symbol in the Cadence Allegro PCB Librarian Part Developer tool, you can edit the symbol graphics, fracture the symbol into multiple slots, and add or change package or symbol properties.

The Part Developer Symbol Editor contains many graphical tools to edit the graphics of a particular symbol. To edit the symbol graphics, select the symbol in the cell hierarchy. The **Symbol Pins** tab appears. You can edit the preview graphic of the symbol in the **Symbol Pins** tab.

Fracturing a Cadence Allegro PCB Librarian Part Developer package into separate symbol slots is useful for FPGA designs. A single symbol for most FPGA packages might be too large for a single schematic page. Splitting the part into separate slots allows you to organize parts of the symbol by function, creating cleaner circuit schematics. For example, you can create one slot for an I/O symbol, a second slot for a JTAG symbol, and a third slot for a power/ground symbol.

Figure 9-4 shows a part fractured into separate slots.

Figure 9-4. Splitting a Symbol into Multiple Slots (Notes 1), (2)



Notes to Figure 9-4:

- (1) Figure 9-4 represents a Cyclone device with JTAG or passive serial (PS) mode configuration option settings. Symbols created for other devices or other configuration modes may have different sets of configuration pins, but can be fractured in a similar manner.
- (2) The power/ground slot shows only a representation of power and ground pins. Because the device contains a large number of power and ground pins.

To fracture a part into separate slots, or to modify the slot locations of pins on parts that are already fractured in the Cadence Allegro PCB Librarian Part Developer tool, perform the following steps:

1. Start the Cadence Allegro Design Project Manager.
2. On the Flows menu, click **Library Management**.
3. Click **Part Developer**.
4. Click the name of the package you want to change in the cell hierarchy.
5. Click **Functions/Slots**. If you are not creating new slots but want to change the slot location of some pins, proceed to Step 6. If you are creating new slots, click **Add**. A dialog box appears, allowing you to add extra symbol slots. Set the number of extra slots you want to add to the existing symbol, not the total number of desired slots for the part. Click **OK**.
6. Click **Distribute Pins**. Specify the slot location for each pin. Use the checkboxes in each column to move pins from one slot to another. Click **OK**.
7. After distributing the pins, click the **Package Pin** tab and click **Generate Symbol(s)**.

8. Select whether to create a new symbol or modify an existing symbol in each slot. Click **OK**.

The newly generated or modified slot symbols display as separate symbols in the cell hierarchy. Each of these symbols can be edited individually.



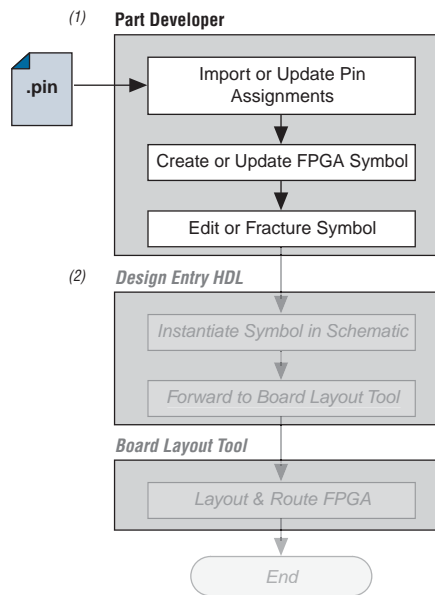
The Cadence Allegro PCB Librarian Part Developer tool allows you to remap pin assignments in the **Package Pin** tab of the main Cadence Allegro PCB Librarian Part Developer window. If signals are remapped to different pins in the Cadence Allegro PCB Librarian Part Developer tool, the changes are reflected only in regenerated symbols for use in your schematics. You cannot transfer pin assignment changes to the Quartus II software from the Cadence Allegro PCB Librarian Part Developer tool, which creates a potential mismatch of the schematic symbols and assignments in the FPGA design. If pin assignment changes are necessary, make the changes in the Quartus II Pin Planner instead of the Cadence Allegro PCB Librarian Part Developer tool, and update the symbol as described in the following sections.



For more information about creating, editing, and organizing component symbols with the Cadence Allegro PCB Librarian Part Developer tool, refer to the Part Developer Help.

Update FPGA Symbol


As the design process continues, you must make changes to the logic design in the Quartus II software, placing signals on different pins after the design is recompiled, or use the Quartus II Pin Planner to make changes manually. The board designer can request such changes to improve the board routing and layout. These types of changes must be carried forward to the circuit schematic and board layout tools to ensure signals are connected to the correct pins on the FPGA. Updating the **.pin** in the Quartus II software facilitates this flow. [Figure 9-5](#) shows this part of the design flow.

Figure 9-5. Updating the FPGA Symbol in the Design Flow**Notes to Figure 9-5:**

- (1) For more information about the full design flow flowchart, refer to [Figure 9-1 on page 9-3](#).
- (2) Grayed out steps are not part of the FPGA symbol update process.

To update the symbol using the Cadence Allegro PCB Librarian Part Developer tool after the **.pin** is updated, perform the following steps:

1. On the File menu, click **Import and Export**. The Import and Export wizard appears.
2. In the list of actions to perform, select **Import ECO - FPGA**. Click **Next**. The **Select Source** dialog box appears.
3. Select the updated source of the FPGA assignment information. In the **Vendor** list, select **Altera**. In the **PnR Tool** list, select **quartusII**. In the **PR File** field, click **browse** to specify the updated **.pin** in your Quartus II project directory. Click **Next**. The Select Destination window appears.
4. Select the source component and a destination cell for the updated symbol. To create a new component based on the updated pin assignment data, select **Generate Custom Component**. This replaces the cell listed under the **Specify Library and Cell** name header with a new, non-fractured cell. Any symbol edits or fractures are lost. You can preserve these edits by selecting **Use standard component and select the existing library and cell**. Select the destination library for the component and click **Next**. The **Preview of Import Data** dialog box appears.
5. Make any additional changes to your symbol. Click **Next**. A list of ECO messages displays summarizing what changes will be made to the cell. To accept the changes and update the cell, click **Finish**.
6. The main Cadence Allegro PCB Librarian Part Developer window appears. You can edit, fracture, and generate the updated symbols as usual from the main Cadence Allegro PCB Librarian Part Developer window.


 If the Cadence Allegro PCB Librarian Part Developer tool is not set up to point to your PCB Librarian Expert license file, an error message displays in red at the bottom of the message text window of the Part Developer when you select the **Import and Export** command. To point to your PCB Librarian Expert license, on the File menu, click **Change Product**, and select the correct product license.

Instantiating the Symbol in the Cadence Allegro Design Entry HDL Software

To instantiate the symbol in your Cadence Allegro Design Entry HDL schematic after the new symbol is saved in the Cadence Allegro PCB Librarian Part Developer tool, perform the following steps:


1. In the Cadence Allegro Project Manager tool, switch to the board design flow.
2. On the Flows menu, click **Board Design**.
3. To start the Cadence Allegro Design Entry HDL software, click **Design Entry**.
4. To add the newly created symbol to your schematic, on the Component menu, click **Add**. The **Add Component** dialog box appears.
5. Select the new symbol library location, and select the name of the cell you created from the list of cells.


The symbol is now “attached” to your cursor for placement in the schematic. If you fractured the symbol into slots, right-click the symbol and choose **Version** to select one of the slots for placement in the schematic.

 For more information about the Cadence Allegro Design Entry HDL software, including licensing, support, usage, training, and product updates, refer to the Help in the software or go to the Cadence website (www.cadence.com).

FPGA-to-Board Integration with Cadence Allegro Design Entry CIS Software

The Cadence Allegro Design Entry CIS software is a mid-level schematic capture tool (part of the Cadence 200 series design flow based on OrCAD Capture CIS). Use the Cadence Allegro Design Entry CIS software to create flat circuit schematics for all types of PCB design. You can also create hierarchical schematics to facilitate design reuse and team-based design using the Cadence Allegro Design Entry CIS software. With the Cadence Allegro Design Entry CIS software, the design flow from FPGA-to-board is unidirectional using only the **.pin** generated by the Quartus II software. Signal and pin assignment changes can only be made in the Quartus II software and are reflected in updated symbols in a Cadence Allegro Design Entry CIS schematic project. [Figure 9-2 on page 9-4](#) shows the design flow with the Cadence Allegro Design Entry CIS software.

 Routing or pin assignment changes made in a board layout tool or a Cadence Allegro Design Entry CIS symbol cannot be back-annotated to the Quartus II software.

 For more information about the Cadence Allegro Design Entry CIS software, including licensing, support, usage, training, and product updates, refer to the Help in the software, go to the Cadence (www.cadence.com) or go to the EMA Design Automation website (www.ema-eda.com).

Cadence Allegro Design Entry CIS Project Creation

The Cadence Allegro Design Entry CIS software has built-in support for creating schematic symbols using pin assignment information imported from the Quartus II software.

To create a new project in the Cadence Allegro Design Entry CIS software, perform the following steps:

1. On the File menu, point to **New** and click **Project**. The New Project wizard starts.

When you create a new project, you can select the PC Board wizard, the Programmable Logic wizard, or a blank schematic.

2. Select the PC Board wizard to create a project where you can select which part libraries to use, or select a blank schematic.

The Programmable Logic wizard is used only to build an FPGA logic design in the Cadence Allegro Design Entry CIS software.

Your new project is created in the specified location and consists of the following files:

- OrCAD Capture Project File (**.opj**)
- Schematic Design File (**.dsn**)

Generate Part

After you create a new project or open an existing project in the Cadence Allegro Design Entry CIS software, you can generate a new schematic symbol based on your Quartus II FPGA design. You can also update an existing symbol if your **.pin** is updated in the Quartus II software. The Cadence Allegro Design Entry CIS software stores component symbols in OrCAD Library File (**.olb**). When a symbol is placed in a library attached to a project, it is immediately available for instantiation in the project schematic.

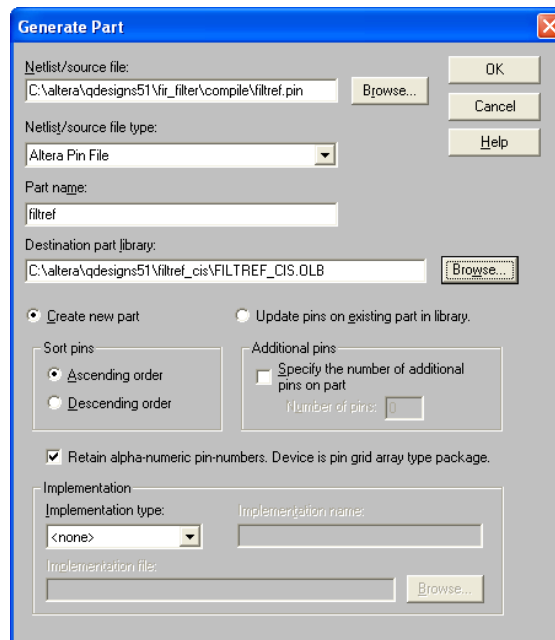
You can add symbols to an existing library or you can create a new library specifically for the symbols generated from your FPGA designs. To create a new library, perform the following steps:

1. On the File menu, point to **New** and click **Library** in the Cadence Allegro Design Entry CIS software to create a default library named **library1.olb**. This library appears in the **Library** folder in the Project Manager window of the Cadence Allegro Design Entry CIS software.
2. To specify a desired name and location for the library, right-click the new library and select **Save As**. The library file is not created until you save the new library.

You can now create a new symbol to represent your FPGA design in your schematic. To generate a schematic symbol, perform the following steps:

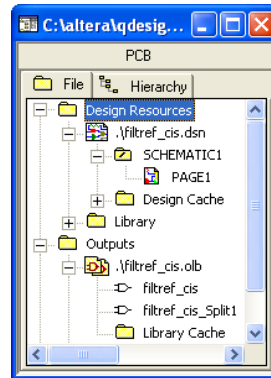
1. Start the Cadence Allegro Design Entry CIS software.
2. On the Tools menu, click **Generate Part**. The **Generate Part** dialog box appears (Figure 9-6).

Figure 9-6. Generate Part Dialog Box



3. To specify the **.pin** from your Quartus II design, in the **Netlist/source file type** field, click **Browse**.
4. In the **Netlist/source file type** list, select **Altera Pin File**.
5. Enter the new part name.
6. Specify the **Destination part library** for the symbol. If you do not select an existing library for the part, a new library is created with a default name that matches the name of your Cadence Allegro Design Entry CIS project.
7. To create a brand new symbol for this design, select **Create new part**. If you updated your **.pin** in the Quartus II software and want to transfer any assignment changes to an existing symbol, select **Update pins on existing part in library**.
8. Select any other desired options and set **Implementation type** to **<none>**. The symbol is for a primitive library part based only on the **.pin** and does not require special implementation. Click **OK**.
9. Review the Undo warning and click **Yes** to complete the symbol generation.

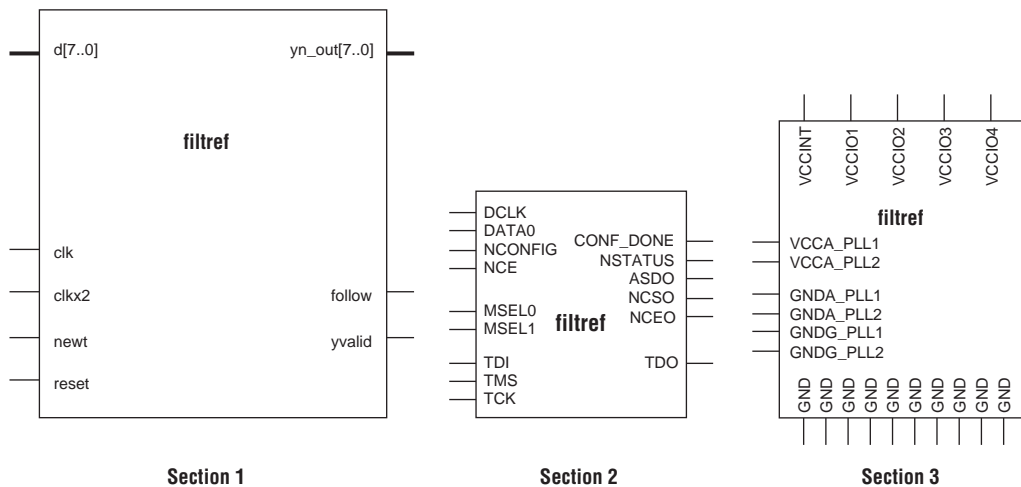
The symbol is generated and placed in the selected library or in a new library found in the **Outputs** folder of the design in the Project Manager window (Figure 9-7). Double-click the name of the new symbol to see its graphical representation and edit it manually using the tools available in the Cadence Allegro Design Entry CIS software.

Figure 9-7. Project Manager Window

For more information about creating and editing symbols in the Cadence Allegro Design Entry CIS software, refer to the Help in the software.


Split Part

After a new symbol is saved in a project library, you can fracture the symbol into multiple parts called sections. Fracturing a part into separate sections is useful for FPGA designs. A single symbol for most FPGA packages might be too large for a single schematic page. Splitting the part into separate sections allows you to organize parts of the symbol by function, creating cleaner circuit schematics. For example, you can create one slot for an I/O symbol, a second slot for a JTAG symbol, and a third slot for a power/ground symbol. [Figure 9-8](#) shows a part fractured into separate sections.

Figure 9-8. Splitting a Symbol into Multiple Sections (Notes 1), (2)

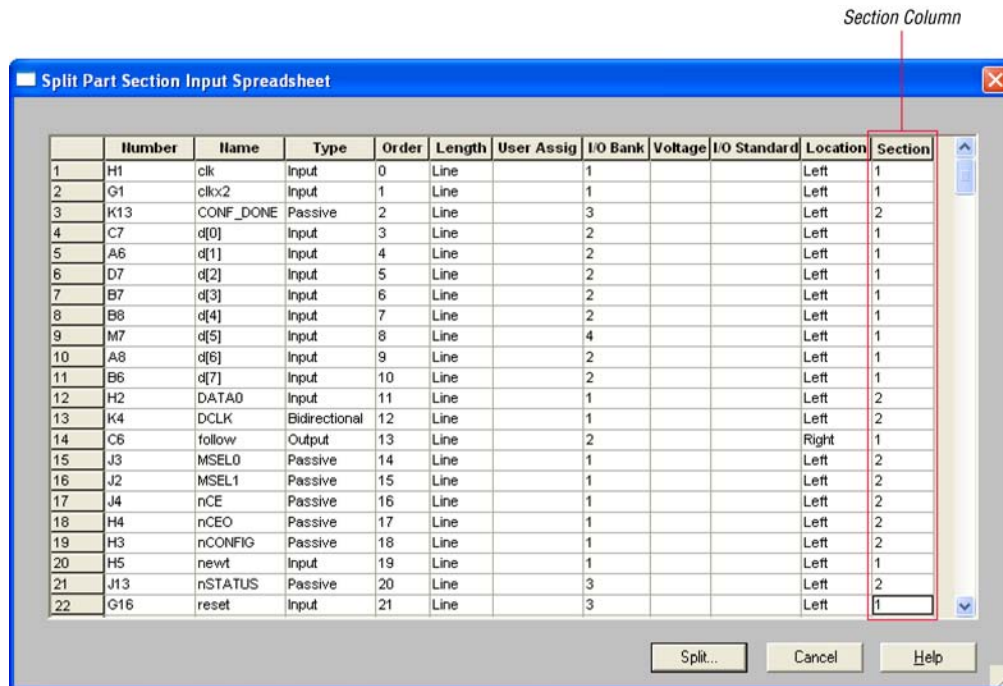
Notes to Figure 9-8:

- (1) [Figure 9-8](#) represents a Cyclone device with JTAG or passive serial (PS) mode configuration option settings. Symbols created for other devices or other configuration modes might have different sets of configuration pins, but can be fractured in a similar manner.
- (2) The power/ground section shows only a representation of power and ground pins. In actuality, the device contains a high number of power and ground pins.

 While symbol generation in the Design Entry CIS software refers to symbol fractures as sections, the other tools described in this chapter use different names to refer to symbol fractures.

To split a part into sections, select the part in its library in the Project Manager window of the Cadence Allegro Design Entry CIS software. On the Tools menu, click **Split Part** or right-click the part and choose **Split Part**. The **Split Part Section Input Spreadsheet** appears (Figure 9-9).


Figure 9-9. Split Part Section Input Spreadsheet



	Number	Name	Type	Order	Length	User Assig	I/O Bank	Voltage	I/O Standard	Location	Section
1	H1	clk	Input	0	Line		1			Left	1
2	G1	clkx2	Input	1	Line		1			Left	1
3	K13	CONF_DONE	Passive	2	Line		3			Left	2
4	C7	d[0]	Input	3	Line		2			Left	1
5	A6	d[1]	Input	4	Line		2			Left	1
6	D7	d[2]	Input	5	Line		2			Left	1
7	B7	d[3]	Input	6	Line		2			Left	1
8	B8	d[4]	Input	7	Line		2			Left	1
9	M7	d[5]	Input	8	Line		4			Left	1
10	A8	d[6]	Input	9	Line		2			Left	1
11	B6	d[7]	Input	10	Line		2			Left	1
12	H2	DATA0	Input	11	Line		1			Left	2
13	K4	DCLK	Bidirectional	12	Line		1			Left	2
14	C6	follow	Output	13	Line		2			Right	1
15	J3	MSEL0	Passive	14	Line		1			Left	2
16	J2	MSEL1	Passive	15	Line		1			Left	2
17	J4	nCE	Passive	16	Line		1			Left	2
18	H4	nCEO	Passive	17	Line		1			Left	2
19	H3	nCONFIG	Passive	18	Line		1			Left	2
20	H5	newt	Input	19	Line		1			Left	1
21	J13	nSTATUS	Passive	20	Line		3			Left	2
22	G16	reset	Input	21	Line		3			Left	1

Each row in the spreadsheet represents a pin in the symbol. The spreadsheet column labeled **Section** indicates the section of the symbol to which each pin is assigned. By default, all pins in a new symbol are located in section 1. Change the values in the **Section** column to assign pins to different, new sections of the symbol. You can also specify the side of a section on which the pin will reside by changing the values in the **Location** column. When you are finished, click **Split**. A new symbol appears in the same library as the original with the name *<original part name>_Split1*.

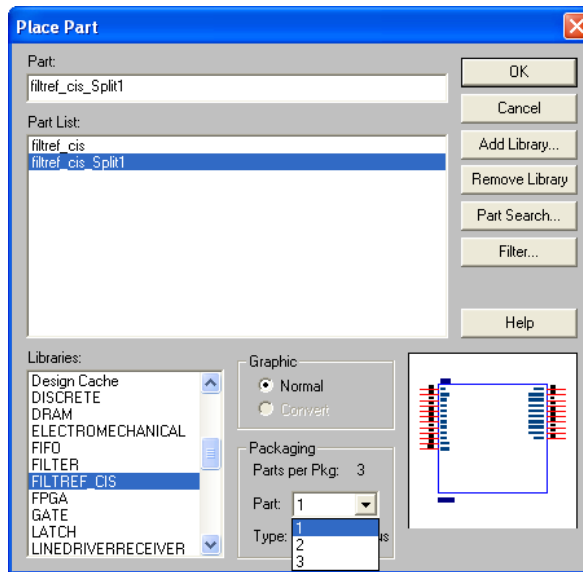
View and edit each section individually. To view the new sections of the part, double-click the part. The Part Symbol Editor window appears. The first section of the part is displayed for editing. On the View menu, click **Package** to view thumbnails of all the part sections. To edit the section of the symbol, double-click the thumbnail.

 For more information about splitting parts into sections and editing symbol sections in the Cadence Allegro Design Entry CIS software, refer to the Help in the software.

Instantiate Symbol in Design Entry CIS Schematic

After a new symbol is saved in a library in your Cadence Allegro Design Entry CIS project, you can instantiate it on a page in your schematic. Open a schematic page in the Project Manager window of the Cadence Allegro Design Entry CIS software. To add the newly created symbol to your schematic on the schematic page, on the Place menu, click **Part**. The **Place Part** dialog box appears (Figure 9-10).

Figure 9-10. Place Part Dialog Box



Select the new symbol library location and the newly created part name. If you select a part that is split into sections, you can select the section to place from the **Part** pop-up menu. Click **OK**. The symbol is now attached to your cursor for placement in the schematic. To place the symbol, click on the schematic page.



For more information about using the Cadence Allegro Design Entry CIS software, refer to the Help in the software.

Altera Libraries for the Cadence Allegro Design Entry CIS Software

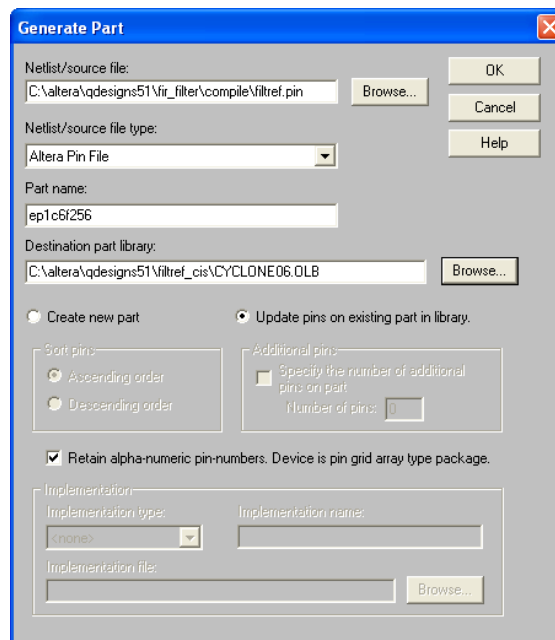
Altera provides downloadable **.olb** for many of its device packages. You can add these libraries to your Cadence Allegro Design Entry CIS project and update the symbols with the pin assignments contained in the **.pin** generated by the Quartus II software. This allows you to use the downloaded library symbols as a base for creating custom schematic symbols with your pin assignments that you can edit or fracture as desired. This can increase productivity by reducing the amount of time it takes to create and edit a new symbol.

To use the Altera-provided libraries with your Cadence Allegro Design Entry CIS project, perform the following steps:

1. Download the library of your target device from the Download Center page found through the Support page on the Altera website (www.altera.com).

2. Create a copy of the appropriate **.olb** to ensure that the original symbols are not altered. Place the copy in a convenient location, such as your Cadence Allegro Design Entry CIS project directory.
3. In the Project Manager window of the Cadence Allegro Design Entry CIS software, click once on the **Library** folder to select it. On the Edit menu, click **Project** or right-click the **Library** folder and choose **Add File** to select the copy of the downloaded **.olb** and add it to your project. The new library is added to the list of part libraries for your project.
4. On the Tools menu, click **Generate Part**. The **Generate Part** dialog box appears (Figure 9-11).

Figure 9-11. Generate Part Dialog Box



5. In the **Netlist/source file** field, click **Browse** to specify the **.pin** in your Quartus II design.
6. From the **Netlist/source file type** list, select **Altera Pin File**.
7. For **Part name**, enter the name of the target device the same as it appears in the downloaded library file. For example, if you are using a device from the **CYCLONE06.OLB** library, enter the part name to match one of the devices in this library such as **ep1c6f256**. You can rename the symbol later in the Project Manager window after the part is updated.
8. Set the **Destination part library** to the copy of the downloaded library you added to the project.
9. Select **Update pins on existing part in library**. Click **OK**.
10. Click **Yes**.

The symbol is updated with your pin assignments. Double-click the symbol in the Project Manager window to view and edit the symbol. On the View menu, click **Package** if you want to view and edit other sections of the symbol. If the symbol in the downloaded library is already fractured into sections, as some of the larger packages are, you can edit each section but you cannot further fracture the part. Generate a new part without using the downloaded part library if you require additional sections.



For more information about creating, editing, and fracturing symbols in the Cadence Allegro Design Entry CIS software, refer to the Help in the software.

Conclusion

Transferring a complex, high-pin-count FPGA design to a PCB for prototyping or manufacturing is a daunting process that can lead to errors in the PCB netlist or design, especially when different engineers are working on different parts of the project. The design workflow available when the Quartus II software is used with tools from Cadence assists the FPGA designer and the board designer in preventing such errors and focusing all attention on the design.

Referenced Document

This chapter references to the following documents:

- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.
- *Simultaneous Switching Noise (SSN) Analysis and Optimizations* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 9-3 shows the revision history for this chapter.

Table 9-3. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	<ul style="list-style-type: none"> ■ Added “Performing Simultaneous Switching Noise (SSN) Analysis of Your FPGA” on page 9-5. ■ General style editing. ■ Edited Figure 9-4 on page 9-10 and Figure 9-8 on page 9-16. 	Updated for the Quartus II software version 9.1 release.
March 2009 v9.0.0	<ul style="list-style-type: none"> ■ Chapter 9 was previously Chapter 7 in the 8.1 software release. ■ No change to content. 	Updated for the Quartus II software version 9.0 release.
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size.	Updated for the Quartus II software version 8.1 release.
May 2008 v8.0.0	Updated references.	Updated for the Quartus II software version 8.0.



For previous versions of the *Quartus II Handbook*, refer to the [Quartus II Handbook Archive](#).