13. PowerPlay Power Analysis

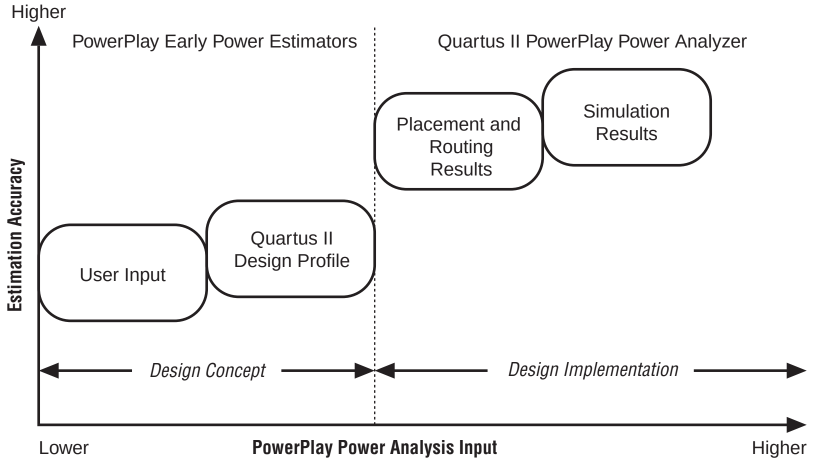
QII53013-9.1.0

This chapter describes how to use the Altera® Quartus® II PowerPlay Power Analysis tools to accurately estimate device power consumption.

Introduction

As designs grow larger and process technology continues to shrink, power becomes an increasingly important design consideration. When designing a PCB, the power consumed by a device must be accurately estimated to develop an appropriate power budget and to design the power supplies, voltage regulators, heat sink, and cooling system. As shown in Figure 13–1, the PowerPlay Power Analysis tools provide the ability to estimate power consumption from early design concept through design implementation.

Figure 13–1. PowerPlay Power Analysis



Early in your design cycle, you can use Microsoft Excel-based PowerPlay Early Power Estimation (EPE) spreadsheets to provide preliminary power consumption and heat dissipation estimates for Arria® GX, Cyclone®, HardCopy®, MAX® II, and Stratix® series devices. To calculate the estimates, you must enter information about environmental conditions and the number of device resources (such as clocks, DSP blocks) that you expect to use in your design. When your design is partially complete, you can generate a PowerPlay Early Power Estimator file with the Quartus II software to provide the EPE spreadsheets with the design's device resource profile. You can use the Quartus II software to generate a PowerPlay EPE file for Arria GX, Cyclone, MAX II, and Stratix series devices. Late in your design cycle, you can use the PowerPlay Power Analyzer in the Quartus II software to provide the most accurate estimate of device power consumption and heat dissipation.

The PowerPlay Power Analyzer is available for Arria GX, Cyclone, HardCopy, MAX II, and Stratix series devices.

For more information about acquiring the PowerPlay EPE spreadsheet, refer to PowerPlay Early Power Estimators (EPE) and Power Analyzer on the Altera website.

This chapter discusses the following topics:

Creating PowerPlay EPE Spreadsheets

You can use PowerPlay EPE spreadsheets to perform a preliminary thermal analysis and power consumption estimate for your design. You can enter the data manually, or you can use the tools in the Quartus II software to assist you in generating the device resources usage information for your design.

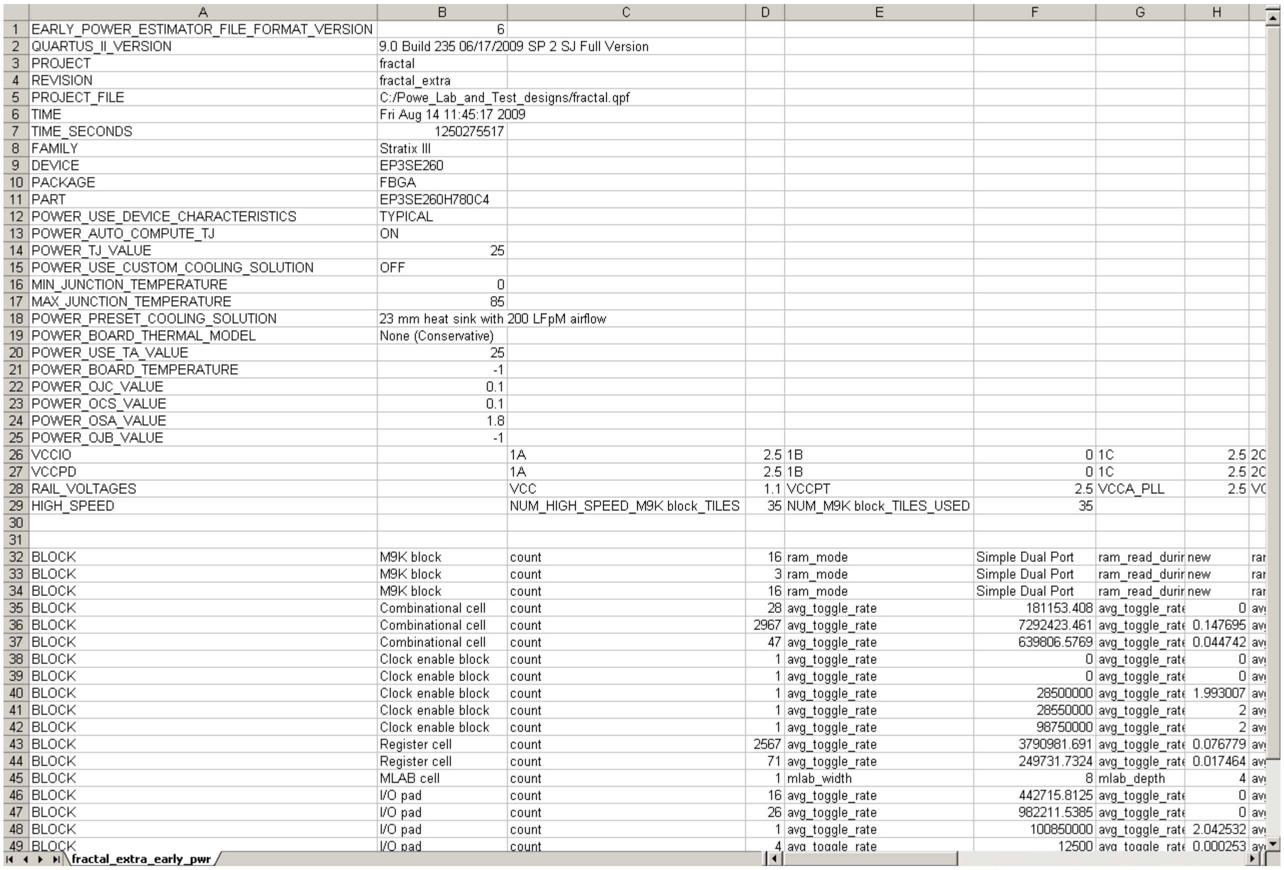
If you manually enter data into the EPE spreadsheet, you must enter the device resources, operating frequency, toggle rates, and other parameters for your design. If you do not have an existing design, you must estimate the number of device resources used in your design and enter them manually.

If you have an existing design or a partially completed design, you can use the Quartus II software to generate the PowerPlay EPE file to assist you in completing the PowerPlay EPE spreadsheet.

To generate the power estimation file, you must first compile your design in the Quartus II software. After compilation is complete, on the Project menu, click **Generate PowerPlay Early Power Estimator File**. The PowerPlay Early Power Estimator file is a Comma-Separated Value File (**.csv**) named ***<name of Quartus II project>*****_early_power.csv**. If your design targets a Cyclone, Stratix, or Stratix GX devices, the PowerPlay Early Power Estimator file is in Tab-Separated Value File (**.txt**) named ***<name of Quartus II project>*****_early_power.txt.**

Figure 13–2 shows an example of the contents of a power estimation file generated for a design that targets a Stratix II device.

Figure 13–2. Example of a PowerPlay Power Estimation File



	A	B	C	D	E	F	G	H	
1	EARLY_POWER_ESTIMATOR_FILE_FORMAT_VERSION	6							
2	QUARTUS_II_VERSION	9.0 Build 235 06/17/2009 SP 2 SJ Full Version							
3	PROJECT	fractal							
4	REVISION	fractal_extra							
5	PROJECT_FILE	C:/Powe_Lab_and_Test_designs/fractal.qpf							
6	TIME	Fri Aug 14 11:45:17 2009							
7	TIME_SECONDS	1250275517							
8	FAMILY	Stratix III							
9	DEVICE	EP3SE260							
10	PACKAGE	FBGA							
11	PART	EP3SE260H780C4							
12	POWER_USE_DEVICE_CHARACTERISTICS	TYPICAL							
13	POWER_AUTO_COMPUTE_TJ	ON							
14	POWER_TJ_VALUE	25							
15	POWER_USE_CUSTOM_COOLING_SOLUTION	OFF							
16	MIN_JUNCTION_TEMPERATURE	0							
17	MAX_JUNCTION_TEMPERATURE	85							
18	POWER_PRESET_COOLING_SOLUTION	23 mm heat sink with 200 LFpM airflow							
19	POWER_BOARD_THERMAL_MODEL	None (Conservative)							
20	POWER_USE_TA_VALUE	25							
21	POWER_BOARD_TEMPERATURE	-1							
22	POWER_OJC_VALUE	0.1							
23	POWER_OCS_VALUE	0.1							
24	POWER_OSA_VALUE	1.8							
25	POWER_OJB_VALUE	-1							
26	VCCIO		1A	2.5	1B	0	1C	2.5	2C
27	VCCPD		1A	2.5	1B	0	1C	2.5	2C
28	RAIL_VOLTAGES		VCC	1.1	VCCPT	2.5	VCCA_PLL	2.5	VC
29	HIGH_SPEED		NUM_HIGH_SPEED_M9K block_TILES	35	NUM_M9K block_TILES_USED	35			
30									
31									
32	BLOCK	M9K block	count	16	ram_mode	Simple Dual Port	ram_read_durir	new	rar
33	BLOCK	M9K block	count	3	ram_mode	Simple Dual Port	ram_read_durir	new	rar
34	BLOCK	M9K block	count	16	ram_mode	Simple Dual Port	ram_read_durir	new	rar
35	BLOCK	Combinational cell	count	28	avg_toggle_rate	181153.408	avg_toggle_rat	0	av
36	BLOCK	Combinational cell	count	2967	avg_toggle_rate	7292423.461	avg_toggle_rat	0.147695	av
37	BLOCK	Combinational cell	count	47	avg_toggle_rate	639806.5769	avg_toggle_rat	0.044742	av
38	BLOCK	Clock enable block	count	1	avg_toggle_rate	0	avg_toggle_rat	0	av
39	BLOCK	Clock enable block	count	1	avg_toggle_rate	0	avg_toggle_rat	0	av
40	BLOCK	Clock enable block	count	1	avg_toggle_rate	28500000	avg_toggle_rat	1.993007	av
41	BLOCK	Clock enable block	count	1	avg_toggle_rate	28550000	avg_toggle_rat	2	av
42	BLOCK	Clock enable block	count	1	avg_toggle_rate	98750000	avg_toggle_rat	2	av
43	BLOCK	Register cell	count	2567	avg_toggle_rate	3790981.691	avg_toggle_rat	0.076779	av
44	BLOCK	Register cell	count	71	avg_toggle_rate	249731.7324	avg_toggle_rat	0.017464	av
45	BLOCK	MLAB cell	count	1	mlab_width	8	mlab_depth	4	av
46	BLOCK	I/O pad	count	16	avg_toggle_rate	442715.8125	avg_toggle_rat	0	av
47	BLOCK	I/O pad	count	26	avg_toggle_rate	982211.5385	avg_toggle_rat	0	av
48	BLOCK	I/O pad	count	1	avg_toggle_rate	100850000	avg_toggle_rat	2.042532	av
49	BLOCK	I/O pad	count	4	avg_toggle_rate	12500	avg_toggle_rat	0.000253	av

The PowerPlay EPE spreadsheet includes the Import Data macro that parses the information in the power estimation file and transfers it into the spreadsheet. If you do not want to use the macro, you can manually transfer the data into the EPE spreadsheet.

For example, after importing the PowerPlay EPE file information into the PowerPlay EPE spreadsheet, you can add additional devices resource information at any time. If the existing Quartus II project represents only a portion of your full design, you must manually enter the additional device resources used in the final design.

PowerPlay EPE File Generator Compilation Report

After successfully generating the power estimation file, a PowerPlay EPE File Generator report is created under the **Compilation Report** section. This report is divided into different sections, such as Summary, Settings, Generated Files, Confidence Metric Details, and Signal Activities. For more information about the PowerPlay EPE File Generator report, refer to "PowerPlay Power Analyzer Compilation Report" on page 13–26.

Table 13–1 lists the main differences between the PowerPlay EPE and the Quartus II PowerPlay Power Analyzer.

Table 13–1. Comparison of the PowerPlay EPE and Quartus II PowerPlay Power Analyzer

Characteristic	PowerPlay EPE	Quartus II PowerPlay Power Analyzer
Phase in the design cycle	Any time	After fitting
Tool requirements	Spreadsheet program or the Quartus II software	The Quartus II software
Accuracy	Medium	Medium to very high
Data inputs	■ Resource usage estimates ■ Clock requirements ■ Environmental conditions ■ Toggle rate	■ Design after fitting ■ Clock requirements ■ Register transfer level (RTL) simulation results (optional) ■ Post-fitting simulation results (optional) ■ Signal activities per node or entity (optional) ■ Signal activity defaults ■ Environmental conditions
Data outputs *(1)*	■ Total thermal power dissipation ■ Thermal static power ■ Thermal dynamic power ■ Off-chip power dissipation ■ Current drawn from voltage supplies *(2)*	■ Total thermal power ■ Thermal static power ■ Thermal dynamic power ■ Thermal I/O power ■ Thermal power by design hierarchy ■ Thermal power by block type ■ Thermal power dissipation by clock domain ■ Off-chip (non-thermal) power dissipation ■ Device supply currents *(2)*

Notes to Table 13–1:

(1) EPE output varies by device family as some features might not be available.

(2) Available only for Arria GX, Cyclone II, Cyclone III, Hardcopy II, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

The result of the PowerPlay Power Analyzer is only an estimation of power and must not be treated as a specification. The purpose of the estimation is to help you to establish a guide for the power budget of your design. Altera recommends measuring the actual power on the board. You must measure the total dynamic current of your design during device operation because the estimate is design dependent and depends on many variable factors, including input vector quantity, quality, and exact loading conditions of a PCB design. Static power consumption must not be based on empirical observation. The values reported by the PowerPlay Power Analyzer or data sheet must be used because the tested devices might not exhibit worst-case behavior.

Types of Power Analysis

Understanding the uses of power analysis and the factors affecting power consumption helps you to effectively use the PowerPlay Power Analyzer. Power analysis meets two significant planning requirements:

- **Thermal planning—**You must ensure that the cooling solution is sufficient to dissipate the heat generated by the device. The computed junction temperature must fall within normal device specifications.
- **Power supply planning—**Power supplies must provide adequate current to support device operation.

The two types of analyses are closely related because much of the power supplied to the device is dissipated as heat from the device. However, in some situations, the two types of analyses are not identical. For example, if you are using terminated I/O standards, some of the power drawn from the power supply of the device is dissipated in termination resistors, rather than in the device.

Power analysis also addresses the activity of your design over time as a factor that impacts the power consumption of the device. Static power is defined as the power consumed regardless of design activity. Dynamic power is the additional power consumed due to signal activity or toggling.

☞ For power supply planning, you can use the PowerPlay EPE at the early stages of your design cycle, or use the Quartus II PowerPlay Power Analyzer reports when your design is completed to get an estimate of your design power requirement.

Factors Affecting Power Consumption

This section describes the factors affecting power consumption. Understanding these factors lets you use the PowerPlay Power Analyzer and interpret its results effectively.

Device Selection

Different device families have different power characteristics. Many parameters affect the device family power consumption, including choice of process technology, supply voltage, electrical design, and device architecture. For example, the Cyclone II device family architecture is designed to consume less static power than the high-performance and full-featured Stratix II device family.

Power consumption also varies in a single device family. A larger device typically consumes more static power than a smaller device in the same family, due to its larger transistor count. Dynamic power can also increase with device size in devices that employ global routing architectures, such as the MAX device family. Cyclone, Max II, and Stratix devices do not exhibit significantly increased dynamic power as device size increases.

The choice of device package also affects the ability of the device to dissipate heat. This choice can impact your cooling solution choice required to meet junction temperature constraints.

Process variation can affect power consumption. Process variation primarily impacts static power, because sub-threshold leakage current varies exponentially with changes in transistor threshold voltage. As a result, it is critical to consult device specifications for static power and not rely on empirical observation. Process variation has a weak effect on dynamic power.

Environmental Conditions

Operating temperature primarily affects device static power consumption. Higher junction temperatures result in higher static power consumption. The device thermal power and cooling solution that you use must result in the device junction temperature remaining within the maximum operating range for the device. The main environmental parameters affecting junction temperature are the cooling solution and ambient temperature.

Air Flow

Air flow is a measure of how quickly heated air is removed from the vicinity of the device and replaced by air at ambient temperature. Air flow can either be specified as "still air" when no fan is used, or as the linear feet per minute rating of the fan used in the system. Higher air flow decreases thermal resistance.

Heat Sink and Thermal Compound

A heat sink allows more efficient heat transfer from the device to the surrounding area because of its large surface area exposed to the air. The thermal compound that interfaces the heat sink to the device also influences the rate of heat dissipation. The case-to-ambient thermal resistance (θ_{CA}) parameter describes the cooling capacity of the heat sink and thermal compound employed at a given airflow. Larger heat sinks and more effective thermal compounds reduce θ_{CA}.

Junction Temperature

The junction temperature of a device is equal to:

$$T_{Junction} = T_{Ambient} + P_{Thermal} \cdot \theta_{\mathrm{JA}}$$

in which θ_{JA} is the total thermal resistance from the device transistors to the environment, having units of degrees Celsius per watt. The value θ_{JA} is equal to the sum of the junction-to-case (package) thermal resistance (θ_{JC}) and the case-to-ambient thermal resistance (θ_{CA}) of your cooling solution.

Board Thermal Model

The thermal resistance of the path through the board is referred to as the junction-to-board thermal resistance (θ_{JB}) (the units are in degrees Celsius per watt). This is used in conjunction with the board temperature, as well as the top-of-chip θ_{JA} and ambient temperatures, to compute junction temperature.

Device Resource Usage

The number and types of devices resources used greatly affects power consumption.

Number, Type, and Loading of I/O Pins

Output pins drive off-chip components, resulting in high-load capacitance that leads to a high-dynamic power per transition. Terminated I/O standards require external resistors that generally draw constant (static) power from the output pin.

Number and Type of Logic Elements, Multiplier Elements, and RAM Blocks

A design with more logic elements (LEs), multiplier elements, and memory blocks tends to consume more power than a design with fewer such circuit elements. The operating mode of each circuit element also affects its power consumption. For example, a digital signal processing (DSP) block performing 18 × 18 multiplications and a DSP block performing multiply-accumulate operations consume different amounts of dynamic power due to different amounts of internal capacitance being charged on each transition. Static power is also affected, to a small degree, by the operating mode of a circuit element.

Number and Type of Global Signals

Global signal networks span large portions of the device and have high capacitance, resulting in significant dynamic power consumption. The type of global signal is important as well. For example, Stratix II devices support several kinds of global clock networks that span either the entire device or a specific portion of the device (a regional clock network covers a quarter of the device). Clock networks that span smaller regions have lower capacitance and tend to consume less power. The location of the logic array blocks (LABs) driven by the clock network can also have an impact, because the Quartus II software automatically disables unused branches of a clock.

Signal Activities

The final important factor in estimating power consumption is the behavior of each signal in your design. The two vital statistics are the toggle rate and the static probability.

The toggle rate of a signal is the average number of times that the signal changes value per unit of time. The units for toggle rate are transitions per second, and a transition is a change from `1` to `0`, or `0` to `1`.

The static probability of a signal is the fraction of time that the signal is logic `1` during the period of device operation that is being analyzed. Static probability ranges from `0` (always at ground) to `1` (always at logic-high).

Dynamic power increases linearly with the toggle rate as the capacitive load is charged more frequently for logic and routing. The Quartus II models assume full rail-to-rail switching. For high toggle rates, especially on circuit output I/O pins, the circuit can transition before fully charging the downstream capacitance. The result is a slightly conservative prediction of power by the Quartus II PowerPlay Power Analyzer.

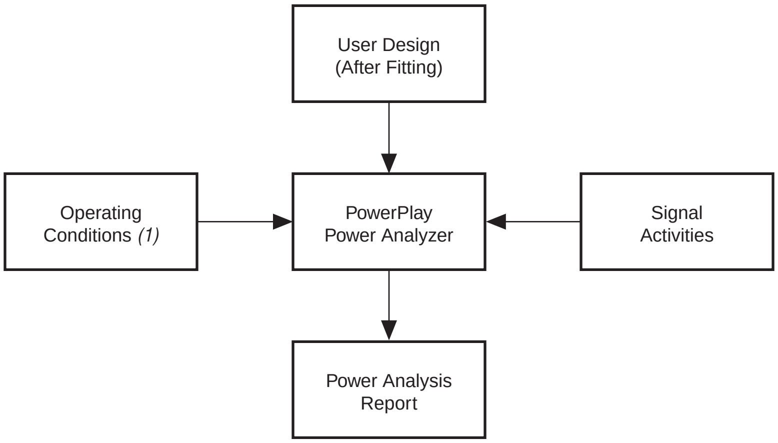
The static power consumed by both routing and logic can sometimes be affected by the static probabilities of their input signals. This effect is due to state-dependent leakage, and has a larger effect on smaller process geometries. The Quartus II software models this effect on devices at 90 nm (or smaller) if it is deemed important to the power estimate. The static power also varies with the static probability of a logic `1` or `0` on the I/O pin when output I/O standards drive termination resistors.

☞ To get accurate results from the power analysis, the signal activities used for analysis must be representative of the actual operating behavior of your design. Inaccurate signal toggle rate data is the largest source of power estimation error.

PowerPlay Power Analyzer Flow

The PowerPlay Power Analyzer supports accurate power estimation by allowing you to specify all the important design factors affecting power consumption. Figure 13–3 shows the high-level PowerPlay Power Analyzer flow.

Figure 13–3. PowerPlay Power Analyzer High-Level Flow



Note to Figure 13–3:

(1) Operating condition specifications are available only for Arria II GX, Arria GX, Cyclone II, Cyclone III series, Cyclone IV, HardCopy series, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

The PowerPlay Power Analyzer requires your design to be synthesized and fitted to the target device. You must specify the electrical standard used by each I/O cell and the capacitive load on each I/O standard in your design to obtain accurate I/O power estimates.

Operating Conditions

For Arria II GX, Arria GX, Cyclone II, Cyclone III series, Cyclone IV, HardCopy series, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families, you can specify the operating conditions for power analysis in the Quartus II software.

The following settings are available in the **Settings** dialog box:

- **Device power characteristics**—You can specify that the device has Typical power consumption characteristics or Maximum power consumption characteristics. The **Typical** setting is useful for comparing to empirical data measured on an average device. The **Maximum** setting uses worst-case data to provide a boundary to the worst-case device that you receive. This setting impacts the static power estimate.
- **Selectable Core Voltage**—You can select a suitable core supply voltage for your design based on performance and power requirements using the **Core Supply Voltage** option, available for Stratix III devices with variable voltage support. The power consumption of a device is heavily dependent on voltage, so it is very important to choose the right core supply voltage for your design. The core supply voltage provides power to device logic resources such as LABs, memory logic array blocks (MLABs), DSP functions, memory, and interconnects.
- **Environmental conditions and junction temperature**—The PowerPlay Power Analyzer automatically computes the junction temperature based on the specified ambient temperature and the cooling solution that you selected. For a more accurate analysis, enter the thermal resistance of your cooling solution. For some cooling solutions, such as a heat sink with no forced airflow, the thermal resistance varies with the amount of thermal power that is dissipated. Air convection increases as the difference between the device temperature and the ambient temperature increases, reducing thermal resistance. If you are entering a thermal resistance in such cases, it is important to use the thermal resistance that occurs when the heat flow (Q) is equal to the thermal power generated by the device.

  ☞ You can also specify a junction temperature in the PowerPlay Power Analyzer. However, Altera does not recommend this because the PowerPlay Power Analyzer provides more accurate results by computing the junction temperature.

- **Board Thermal Modeling**—If you want the PowerPlay Power Analyzer thermal model to take the θ_{JB} into consideration, set the board thermal model to either **Typical** or **Custom**. This feature produces more accurate thermal power estimation.

  A **Typical** board thermal model automatically sets θ_{JB} to a value based on the package and device selected. You must specify a board temperature. If you choose a **Custom** board thermal model, you must specify a value for θ_{JB} and a board temperature. If you do not want the PowerPlay Power Analyzer thermal model to take the θ_{JB} resistance into consideration, set the **Board thermal model** option to **None** (conservative). In this case, the path through the board and the path through power dissipation are not considered, and a more conservative thermal power estimate is obtained.

The **Board thermal model** option is only available if you select the **Auto compute junction temperature** option with the pre-set cooling solution set to a heat sink solution option or custom solution. The **Auto compute junction temperature** option is disabled when a cooling solution with no heat sink is selected, as thermal conduction through the board is included in the θ_{JA} value used to compute a junction temperature.

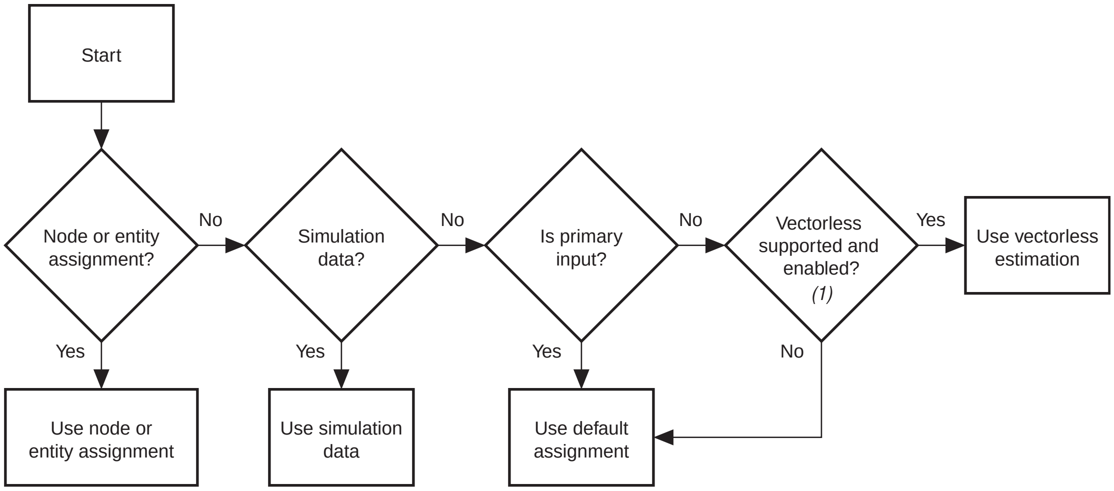
Signal Activities Data Sources

The PowerPlay Power Analyzer provides a flexible framework for specifying signal activities. This reflects the importance of using representative signal activity data during power analysis. You can use the following sources to provide information about signal activity:

- Simulation results
- User-entered node, entity, and clock assignments
- User-entered default toggle rate assignment
- Vectorless estimation

The PowerPlay Power Analyzer allows you to mix and match the signal activity data sources on a signal-by-signal basis. Figure 13–4 shows the priority scheme. The data sources are described in the following sections.

Figure 13–4. Signal Activity Data Source Priority Scheme



Note to Figure 13–4:

(1) Vectorless estimation is available only for the Arria II GX, Arria GX, Cyclone II, Cyclone III series, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

Simulation Results

The PowerPlay Power Analyzer directly reads the waveforms generated by a design simulation. The static probability and toggle rate for each signal is calculated from the simulation waveform. Power analysis is most accurate when simulations are generated using representative input stimuli.

The PowerPlay Power Analyzer reads results generated by the following simulators:

- Quartus II Simulator
- ModelSim® VHDL, Active HDL, ModelSim Verilog HDL, ModelSim-Altera VHDL, ModelSim-Altera Verilog
- NC-Verilog, NC-VHDL
- VCS

Signal activity and static probability information, described in "Signal Activities" on page 13–7, are stored in a Signal Activity File (**.saf**) or are derived from a Verilog Value Change Dump File (**.vcd**). The Quartus II Simulator generates a **.saf** or a **.vcd**, which is read by the PowerPlay Power Analyzer.

For third-party simulators, use the **Quartus II EDA Tool Settings for Simulation** to specify a **Generate Value Change Dump** file script. These scripts instruct the third-party simulators to generate a **.vcd** that encodes the simulated waveforms. The Quartus II PowerPlay Power Analyzer reads this file directly to derive the toggle rate and static probability data for each signal.

Third-party EDA simulators, other than those listed above, can generate a **.vcd** that can then be used with the PowerPlay Power Analyzer. For those simulators, it is necessary to manually create a simulation script to generate the appropriate **.vcd**.

☞ You can use a **.saf** or **.vcd** created for power analysis to optimize your design for power during fitting by utilizing the appropriate settings in the **PowerPlay power optimization** list, available in **Fitter Settings** page of the **Settings** dialog box.

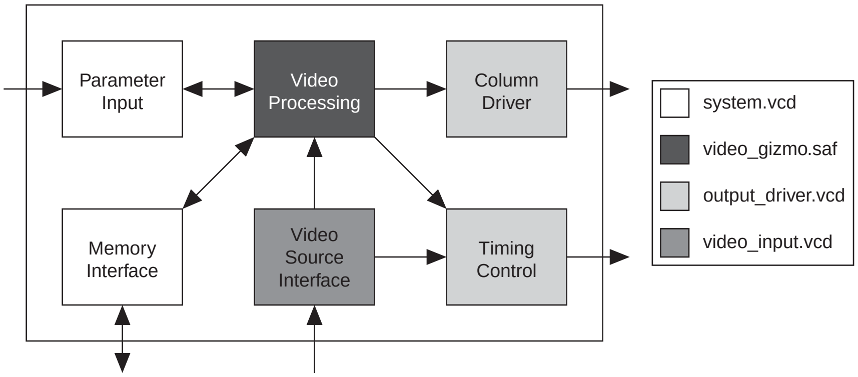
For more information about power optimization, refer to the *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*.

For more information about how to create a **.vcd** in other third-party EDA simulation tools, refer to *Section I. Simulation* in volume 3 of the *Quartus II Handbook*.

Using Simulation Files in Modular Design Flows

A common design practice is to create modular or hierarchical designs in which you develop each design entity separately and then instantiate it in a higher-level entity, forming a complete design. Simulation is performed on a complete design or on each modular design for verification. The Quartus II PowerPlay Power Analyzer supports modular design flows when reading the signal activities generated from these simulation files. An example of a modular design flow is shown in Figure 13–5.

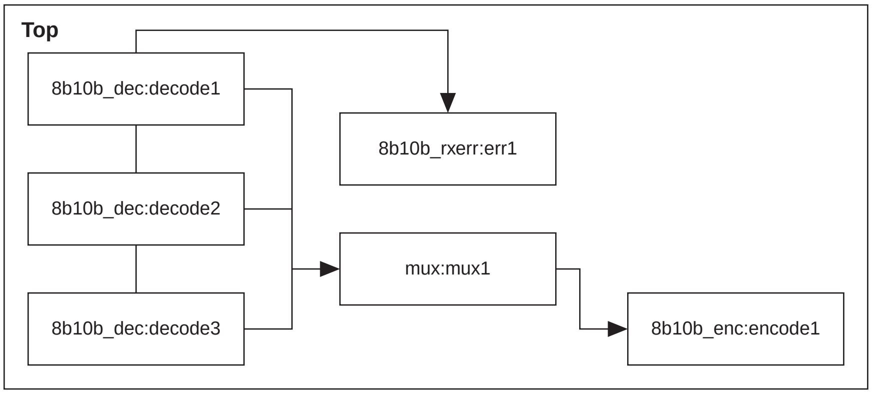
Figure 13–5. Modular Simulation Flow



When specifying a simulation file, an associated design entity name is given, such that the signal activities derived from the simulation file (**.vcd** or **.saf**) are imported into the PowerPlay Power Analyzer for that particular design entity. The PowerPlay Power Analyzer also supports the specification of multiple **.saf** for power analysis, with each having an associated design entity name to allow the integration of partial design simulations into a complete design power analysis. When specifying multiple **.saf** for your design, it is possible that more than one simulation file contains signal activity information for the same signal. When you apply multiple **.saf** to the same design entity, the signal activity used in the power analysis is the equal-weight arithmetic average of each **.saf**. When you apply multiple simulation files to design entities at different levels in your design hierarchy, the signal activity used in the power analysis is derived from the simulation file that is applied to the most specific design entity.

Figure 13–6 shows an example of a hierarchical design. The top-level module of your design, called “top”, consists of three 8b/10b decoders, followed by a multiplexer whose output is then encoded again before being output from your design. There is also an error-handling module that handles any 8b/10b decoding errors. The top contains the top-level entity of your design and any logic not defined as part of another module. The design file for the top-level module might be just a wrapper for the hierarchical entities below it, or it might contain its own logic. The following usage scenarios show common ways that you can simulate your design and import **.saf** into the PowerPlay Power Analyzer.

Figure 13–6. Example Hierarchical Design



Complete Design Simulation

You can simulate the entire design top, generating a **.vcd** if you use a third-party simulator or generating a **.saf** or **.vcd** if you use the Quartus II Simulator. The **.vcd** or **.saf** can then be imported (specifying entity top) into the PowerPlay Power Analyzer. The resulting power analysis uses all the signal activities information from the generated **.vcd** or **.saf**, including those that apply to submodules, such as `decode [1-3]`, `err1`, `mux1`, and `encode1`.

Modular Design Simulation

You can independently simulate submodules of the design top and then import all the resulting **.saf** into the PowerPlay Power Analyzer. For example, you can simulate the `8b10b_dec` independent of the entire design, as well as multiplexer, `8b10b_rxerr`, and `8b10b_enc`. You can then import the **.vcd** or **.saf** generated from each simulation by specifying the appropriate instance name. For example, if the files produced by the simulations are **8b10b_dec.vcd**, **8b10b_enc.vcd**, **8b10b_rxerr.vcd**, and **mux.saf**, the import specifications in Table 13–2 are used.

Table 13–2. Import Specifications

File Name	Entity
8b10b_dec.vcd	`Top|8b10b_dec:decode1`
8b10b_dec.vcd	`Top|8b10b_dec:decode2`
8b10b_dec.vcd	`Top|8b10b_dec:decode3`
8b10b_rxerr.vcd	`Top|8b10b_rxerr:err1`
8b10b_enc.vcd	`Top|8b10b_enc:encode1`
mux.saf	`Top|mux:mux1`

The resulting power analysis applies the simulation vectors found in each file to the assigned entity. Simulation provides signal activities for the pins and for the outputs of functional blocks. If the inputs to an entity instance are input pins for the entire design, the simulation file associated with that instance does not provide signal activities for the inputs of that instance. For example, an input to an entity such as `mux1` has its signal activity specified at the output of one of the decode entities.

Multiple Simulations on the Same Entity

You can perform multiple simulations of an entire design or specific modules of a design. For example, in the process of verifying the design top, you can have three different simulation testbenches: one for normal operation, and two for corner cases. Each of these simulations produces a separate **.vcd** or **.saf**. In this case, apply the different **.vcd** or **.saf** names to the same top-level entity, shown in Table 13–3.

Table 13–3. Multiple Simulation File Names and Entities

File Name	Entity
normal.saf	`Top`
corner1.vcd	`Top`
corner2.vcd	`Top`

The resulting power analysis uses an arithmetic average the signal activities calculated from each simulation file to obtain the final signal activities used. If a signal `err_out` has a toggle rate of zero toggles per second in **normal.saf**, 50 toggles per second in **corner1.vcd**, and 70 toggles per second in **corner2.vcd**, the final toggle rate that is used in the power analysis is 40 toggles per second.

Overlapping Simulations

You can perform a simulation on the entire design top and more exhaustive simulations on a sub-module, such as `8b10b_rxerr`. Table 13–4 shows the import specification for overlapping simulations.

Table 13–4. Overlapping Simulation Import Specifications

File Name	Entity
full_design.vcd	`Top`
error_cases.vcd	`Top|8b10b_rxerr:err1`

In this case, signal activities from **error_cases.vcd** are used for all of the nodes in the generated **.saf** and signal activities from **full_design.vcd** are used for only those nodes that do not overlap with nodes in **error_cases.vcd**. In general, the more specific hierarchy (the most bottom-level module) is used to derive signal activities for overlapping nodes.

Partial Simulations

You can perform a simulation in which the entire simulation time is not applicable to signal activity calculation. For example, if you run a simulation for 10,000 clock cycles and reset the chip for the first 2,000 clock cycles. If the signal activity calculation is performed over all 10,000 cycles, the toggle rates are typically only 80% of their steady state value (because the chip is in reset for the first 20% of the simulation). In this case, you must specify the useful parts of the **.vcd** for power analysis. The **Limit VCD Period** option enables you to specify a start and end time to be used when performing signal activity calculations.

Node Name Matching Considerations

Node name mismatches happen when you have **.saf** or **.vcd** applied to entities other than the top-level entity. In a modular design flow, the gate-level simulation files created in different Quartus II projects may not match their node names with the current Quartus II project.

For example, if you have a file named **8b10b_enc.vcd**, which was generated in a separate project called **8b10b_enc** and is simulating the `8b10b` encoder, and you import that **.vcd** into another project called **Top**, you might encounter name mismatches when applying the **.vcd** to the `8b10b_enc` module in the **Top** project. This is because all the combinational nodes in the **8b10b_enc.vcd** might be named differently in the **Top** project.

You can avoid name mismatching with only RTL simulation data, in which register names usually do not change, or with an incremental compile flow that preserves node names in conjunction with a gate-level simulation.

To ensure the best accuracy, Altera recommends using an incremental compilation flow to preserve the node names of your design.

For more information about the incremental compile flow, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

Glitch Filtering

The PowerPlay Power Analyzer defines a glitch as two signal transitions so closely spaced in time that the pulse, or glitch, occurs faster than the logic and routing circuitry can respond. The output of a transport delay model simulator (the default mode of the Quartus II simulator) generally contains glitches for some signals. The logic and routing structures of the device form a low-pass filter that filters out glitches tens to hundreds of picoseconds long, depending on the device family.

Some third-party simulators use different models than the transport delay model as default model. Different models cause differences in signal activity and power estimation. The inertial delay model, which is the ModelSim default model, filters out more glitches than the transport delay model and it usually yields a lower power estimate.

Altera recommends using the transport simulation model when using Quartus II glitch filtering support with third-party simulators. If the inertial simulation model is used, simulation glitch filtering has little effect.

For more information about how to set the simulation model type for your specific simulator, refer to the Quartus II Help.

Glitch filtering in a simulator can also filter a glitch on one LE (or other circuit element) output from propagating to downstream circuit elements to ensure that the glitch does not affect simulated results. This prevents a glitch on one signal from producing non-physical glitches on all downstream logic, which would result in a signal toggle rate and a power estimate that are too high. Circuit elements in which every input transition produces an output transition, including multipliers and logic cells configured to implement `XOR` functions, are especially prone to glitches. Therefore, circuits with such functions can have power estimates that are too high when glitch filtering is not used.

Altera recommends using the glitch filtering feature to obtain the most accurate power estimates. For **.vcd**, the PowerPlay Power Analyzer flows support two levels of glitch filtering, both of which are recommended for power estimation.

In the first level of glitch filtering, glitches are filtered during simulation. To enable this level of glitch filtering in the Quartus II software for supported third-party simulators, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page appears.
3. Select the **Tool Name** to use for the simulation.
4. Turn on the **Enable glitch filtering** option.

To enable this level of glitch filtering in the Quartus II software using the Quartus II simulator, refer to "Generating a .saf or .vcd Using the Quartus II Simulator" on page 13–20.

The second level of glitch filtering occurs while the PowerPlay Power Analyzer is reading the **.vcd** generated by the Quartus II simulator or a third-party simulator. To enable this level of glitch filtering, perform the following steps:

On the Assignments menu, click **Settings**. The **Settings** dialog box appears.

1. In the **Category** list, select **PowerPlay Power Analyzer Settings**. The **PowerPlay Power Analyzer Settings** page appears.
2. Under **Input File(s)**, turn on the **Perform glitch filtering on VCD files** option.

The **.vcd** file reader performs complementary filtering to the filtering performed during simulation and is often not as effective. While the **.vcd** file reader can remove glitches on logic blocks, it has no way of determining how downstream logic and routing are affected by a given glitch, and may eliminate the impact of the glitch completely. Filtering the glitches during simulation avoids switching downstream routing and logic automatically.

When running simulation for design verification (rather than to produce input to the Quartus PowerPlay Power Analyzer), Altera recommends turning off the glitch filtering option. This produces the most rigorous and conservative simulation from a functionality viewpoint. When performing simulation to produce input for the Quartus II PowerPlay Power Analyzer, Altera recommends turning on the glitch filtering option to produce the most accurate power estimates.

Node and Entity Assignments

You can assign specific toggle rates and static probabilities to individual nodes and entities in the design. These assignments have the highest priority, overriding data from all other signal activity sources.

You must use the Assignment Editor or Tcl commands to create the **Power Toggle Rate** and **Power Static Probability** assignments. You can specify the power toggle rate as an absolute toggle rate in transitions using the **Power Toggle Rate** assignment or you can use the **Power Toggle Rate Percentage** assignment to specify a toggle rate relative to the clock domain of the assigned node for more specific assignment made in terms of hierarchy level.

If the **Power Toggle Rate Percentage** assignment is used, and the given node does not have a clock domain, a warning is issued and the assignment is ignored.

For more information about how to use the Assignment Editor in the Quartus II software, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

This method is appropriate for signals in which you have specific knowledge of the signal or entity being analyzed. For example, if you know that a 100-MHz data bus or memory output produces data that is essentially random (uncorrelated in time), you can directly enter a 0.5 static probability and a toggle rate of 50 million transitions per second.

Bidirectional I/O pins are treated specially. The combinational input port and the output pad for a given pin share the same name. However, those ports might not share the same signal activities. For the purpose of reading signal activity assignments, the PowerPlay Power Analyzer creates a distinct name <*node_name~output*> when the bidirectional signal is configured as an output and <*node_name~result*> when the signal is configured as an input. For example, if a design has a bidirectional pin named `MYPIN`, assignments for the combinational input use the name `MYPIN~result`, and the assignments for the output pad use the name `MYPIN~output`.

When creating the logic assignment in the Assignment Editor, you will not find the `MYPIN~result` and `MYPIN~output` node names in the Node Finder. Therefore, to create the logic assignment, you must manually enter the two differentiating node names to create the specific assignment for the input and output port of the bidirectional pin.

Timing Assignments to Clock Nodes

For clock nodes, the PowerPlay Power Analyzer uses the timing requirements to derive the toggle rate when neither simulation data nor user entered signal activity data is available. f_{MAX} requirements specify full cycles per second, but each cycle represents a rising transition and a falling transition. For example, a clock f_{MAX} requirement of 100 MHz corresponds to 200 million transitions per second.

Default Toggle Rate Assignment

You can specify a default toggle rate for primary inputs and all other nodes in the design. The default toggle rate is used when no other method has specified the signal activity data.

The toggle rate is specified in absolute terms (transitions per second) or as a fraction of the clock rate in effect for each particular node. The toggle rate for a given clock is derived from the timing settings for the clock. For example, if a clock is specified with an f_{MAX} constraint of 100 MHz and a default relative toggle rate of 20%, nodes in this clock domain transition in 20% of the clock periods, or 20 million transitions occur per second. In some cases, the PowerPlay Power Analyzer cannot determine the clock domain for a given node because there is either no clock domain for the node or it is ambiguous. In these cases, the PowerPlay Power Analyzer substitutes and reports a toggle rate of zero.

Vectorless Estimation

For some device families, the PowerPlay Power Analyzer automatically derives estimates for signal activity on nodes with no simulation or user-entered signal-activity data. Vectorless estimation is available and enabled by default for Arria GX, Cyclone II, Cyclone III, HardCopy II, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families. Vectorless estimation statistically estimates the signal activity of a node based on the signal activities of all nodes feeding that node, and on the actual logic function implemented by the node. The **PowerPlay Power Analyzer Settings** dialog box lets you disable vectorless estimation. When enabled, vectorless estimation takes priority over default toggle rates. Vectorless estimation does not override clock assignments.

☞ Vectorless estimation cannot derive signal activities for primary inputs. Vectorless estimation is generally accurate for combinational nodes, but not for registered nodes. Therefore, simulation data for at least the registered nodes and I/O nodes is required for accuracy.

Using the PowerPlay Power Analyzer

For all the flows that use the PowerPlay Power Analyzer, synthesize your design first and then fit it to the target device. You must either provide timing assignments for all the clocks in the design or use a simulation-based flow to generate activity data. The I/O standard used on each device input or output and the capacitive load on each output must be specified in the design.

Common Analysis Flows

You can use the analysis flows in this section with the PowerPlay Power Analyzer. However, vectorless activity estimation is only available for some device families.

Signal Activities from Full Post-Fit Netlist (Timing) Simulation

This flow provides the highest accuracy because all node activities reflect actual design behavior, provided that supplied input vectors are representative of typical design operation. Results are better if the simulation filters glitches. The disadvantage of this method is that the simulation time is long.

Signal Activities from Full Post-Fit Netlist (Zero Delay) Simulation

The zero delay simulation flow is used with designs for which signal activities from a full post-fit netlist (timing) simulation are not available. Zero delay simulation is as accurate as timing simulation in 95% of designs (designs with no glitches).

☞ If your design has glitches, power may be underestimated. Altera recommends using the signal activities from a full post-fit netlist (timing) simulation to achieve accurate power estimation of your design.

The following designs might exhibit glitches:

- Designs with many `XOR` gates, (for example, an encryption core)
- Designs with arithmetic blocks without input and output registers (DSPs and carry chains)

  For more information about creating zero delay simulation signal activities, refer to the "Generating a .vcd from Full Post-Fit Netlist (Zero Delay) Simulation" on page 13–23.

Signal Activities from RTL (Functional) Simulation, Supplemented by Vectorless Estimation

In this flow, simulation provides toggle rates and static probabilities for all pins and registers in the design. Vectorless estimation fills in the values for all the combinational nodes between pins and registers. This method yields good results, because vectorless estimation is accurate, given that the proper pin and register data is provided. This flow usually provides a compilation time benefit to the user in the third-party RTL simulator.

☞ RTL simulation may not provide signal activities for all registers in the post-fitting netlist because some register names might be lost during synthesis. For example, synthesis might automatically transform state machines and counters, thus changing the names of registers in those structures.

Signal Activities from Vectorless Estimation and User-Supplied Input Pin Activities

This option provides a low level of accuracy, because vectorless estimation for registers is not entirely accurate.

Signal Activities from User Defaults Only

This option provides the lowest degree of accuracy.

Generating a .saf or .vcd Using the Quartus II Simulator

While performing a timing or functional simulation using the Quartus II simulator, you can generate a **.saf** or **.vcd**. These files store the toggle rate and static probability for each connected output signal based on the simulation vectors entered in the Vector Waveform File (**.vwf**) or the Vector File (**.vec**). You can use the **.saf** or **.vcd** as input to the PowerPlay Power Analyzer to estimate power for your design. For accurate results, use the **.saf** created in the Quartus II simulator as the input to the PowerPlay power analyzer.

To create a **.saf** or **.vcd** for your design, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulator Settings**.
3. In the **Simulation mode** list, select either **Timing** or **Functional**. For a description of the difference in accuracy between the two types of simulation modes, refer to“Common Analysis Flows” on page 13–19.
4. (Optional) Click **More Settings**. The **More Simulator Settings** dialog box appears.
5. (Optional) Turn on glitch filtering. To turn on glitch filtering, in the **Glitch filtering options** list, select **Always**.
6. In the **Category** list, click the “+” icon to expand **Simulator Settings** and select **Simulation Output Files**.
7. Turn on **Generate Signal Activity File** and enter the file name for the **.saf**. When generating a **.vcd** from the Quartus simulator, ensure that you add **all nodes** to the input vector wave file. Only the nodes that have been added to your vector file are output to the Quartus-generated **.vcd**. This is not the case when generating a **.saf**. The Quartus II simulator creates a **.saf**, including all the internal nodes of your design, even if the stimuli file contains only the input vectors for your simulation.

   For more information about the Quartus II simulator and how to create a **.saf**, refer to the *Quartus II Simulator* chapter in volume 3 of the *Quartus II Handbook*.

8. (Optional) Click **Signal Activity File Options**. The **Signal Activity File Options** dialog box appears. Turn on the **Limit signal activity period** option to specify the simulation period to use when calculating the signal activities.

   Power estimation is performed for the entire simulation time or for a portion of the simulation time. This allows you to look at the power consumption at different points in your overall simulation without having to rework your testbenches. This feature is also useful when multiple clock cycles are necessary to initialize the state of the design, but you want to measure the signal activity only during the normal operation of the design and not during its initialization phase. You can specify the start time and end time in the **Signal Activity File Options** dialog box by turning on the **Limit signal activity period** option. Simulation information is used during this time interval only to calculate toggle rates and static probabilities. If no time interval is specified, the whole simulation is used to compute signal activity data.

9. After the simulation is complete, a **.saf** is generated with the specified filename and stored in the main project directory.

For more information about how to perform simulations in the Quartus II software, refer to the Quartus II Help.

Generating a .vcd Using a Third-Party Simulator

You can use other EDA simulation tools, such as the ModelSim® software, to perform a simulation and create a **.vcd**. You can use this file as the input to the PowerPlay Power Analyzer to estimate power for your design. You must instruct the Quartus II software to generate a script file that is used as input to the third-party simulator. This script tells the third-party simulator to generate a **.vcd** that contains all the output signals. For more information about the supported third-party simulators, refer to "Simulation Results" on page 13–11.

To create a **.vcd** for your design, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page appears.
3. In the **Tool name** list, select the appropriate EDA simulation tool.
4. In the **Format for output netlist** list, select **VHDL** or **Verilog**.
5. Turn on **Generate Value Change Dump (VCD) file script**.

This turns on the **Map illegal HDL characters** and **Enable glitch filtering** options.

6. (Optional) The **Map illegal HDL characters** option ensures that all signals have legal names and that signal toggle rates are available later in the PowerPlay Power Analyzer.
7. (Optional) By turning on **Enable glitch filtering**, glitch filtering logic is the output when you generate an EDA netlist for simulation. This option is always available, regardless of whether or not you want to generate the **.vcd** scripts. For more information about glitch filtering, refer to "Glitch Filtering" on page 13–15.

When performing simulation using ModelSim, the **+nospecify** option for the `vsim` command disables the **specify path delays and timing checks** option in ModelSim. By enabling glitch filtering on the **Simulation** page, the simulation models include specified path delays. Thus, ModelSim can fail to simulate a design if glitch filtering is enabled, and the **+nospecify** option is specified. Altera recommends removing the **+nospecify** option from the ModelSim `vsim` command to ensure accurate simulation for power estimation.

8. Click **Script Settings**. The **Script Settings** dialog box appears.

   Select which signals must be output to the **.vcd**. With **All signals** selected, the generated script instructs the third-party simulator to write all connected output signals to the **.vcd**. With **All signals except combinational lcell outputs** selected, the generated script tells the third-party simulator to write all connected output signals to the **.vcd**, except logic cell combinational outputs.

   The file can become extremely large if you write all output signals to the file (because its size depends on the number of output signals being monitored and the number of transitions that occur).

9. Click **OK**.
10. Type a name for your testbench in the **Design instance name** box.
11. Compile your design with the Quartus II software and generate the necessary EDA netlist and script that tells the third-party simulator to generate a **.vcd**.

    For more information about NativeLink use, refer to *Section I. Simulation* in volume 3 of the *Quartus II Handbook*.

12. Perform a simulation with the third-party EDA simulation tool. Call the generated script in the simulation tool before running the simulation. The simulation tool generates the **.vcd** and places it in the project directory.

Generating a .vcd from ModelSim Software

To successfully produce a **.vcd** with the ModelSim software, perform the following steps:

1. In the Quartus II software, on the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, point to **EDA Tools Settings** and select **Simulation.** On the **Simulation** page, choose the appropriate ModelSim selection in the **Tool Name** list, and turn on the **Generate Value Change Dump File Script** option.
3. To generate the **.vcd**, perform a full compilation.
4. In the ModelSim software, compile the files necessary for simulation.
5. Load your design by clicking **Start Simulation** on the Tools menu, or use the `vsim` command.
6. Use the **.vcd** script created in step 3 using the following command:
   `source <design>_dump_all_vcd_nodes.tcl`
7. Run the simulation (for example, `run 2000ns` or `run -all`).
8. Quit the simulation using the `quit -sim` command, if required.
9. Exit the ModelSim software. If you do not exit the software, the ModelSim software might end the writing process of the **.vcd** improperly, resulting in a corrupted **.vcd**.

Generating a .vcd from Full Post-Fit Netlist (Zero Delay) Simulation

To successfully generate a **.vcd** from the full post-fit Netlist (zero delay) simulation, perform the following steps:

1. Perform design compilation in the Quartus II software to generate the Netlist <*project_name*>**.vo**.
2. In <*project_name*>**.vo**, search for the include statement for <*project_name*>**.sdo**, comment the statement out, and save the file.
3. Generate a **.vcd** for power estimation by performing the steps in "Generating a .vcd Using a Third-Party Simulator" on page 13–21.

Standard Delay Format Output File (**.sdo**) is required for gate-level timing simulation. The **.sdo** contains the delay information of each architecture primitive and routing element specific to your design. You must exclude the **.sdo** for zero delay simulation.

For more information about how to create a **.vcd** in other third-party EDA simulation tools, refer to *Section I. Simulation* in volume 3 of the *Quartus II Handbook*.

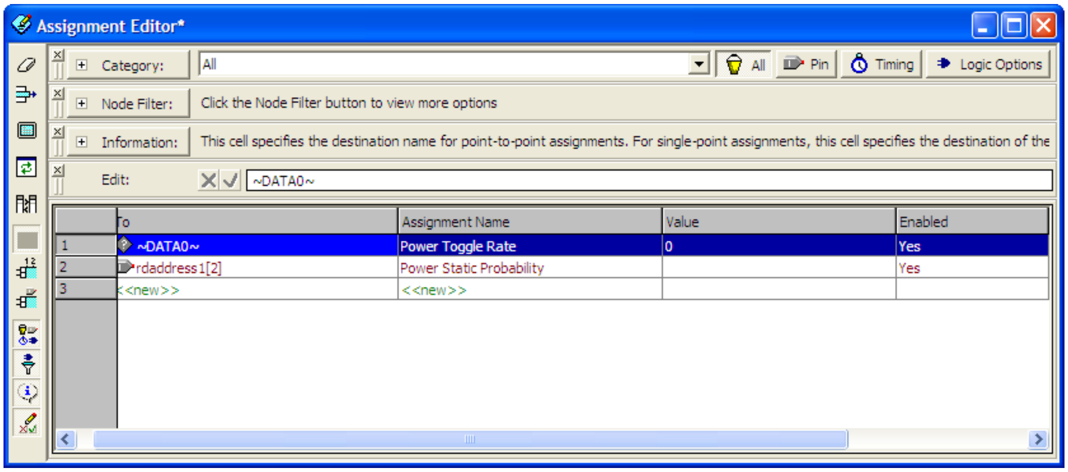
Running the PowerPlay Power Analyzer Using the Quartus II GUI

To run the PowerPlay Power Analyzer using the Quartus II GUI, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **PowerPlay Power Analyzer Settings**.
3. (Optional) If you want to use either **.saf** or **.vcd**, or both as an input to the PowerPlay Power Analyzer, turn on the **Use input file(s) to initialize toggle rates and static probabilities during power analysis** option.
4. Click **Add**. The **Add Power Input File** dialog box appears.
5. Add your **.saf** or **.vcd** by clicking **browse** for the **File name** field.
6. The **Entity** field enables you to specify the design entity (hierarchy) to which the entered power input file applies. To enter the entity, you can type in the box or browse through the list of your design entities. To browse your design entities, click **browse.** The **Select Hierarchy** dialog box appears. You can specify multiple entities in the entity text box with comma delimiters. You can specify whether the input file is a **.vcd** or **.saf** under **Input File Type**. The **Limit VCD period** option is turned on only when **VCD file** is selected. Turning on the **Limit VCD period** option enables you to specify the simulation period when calculating the signal activities. For more information, refer to "Generating a .saf or .vcd Using the Quartus II Simulator" on page 13–20.
7. Click **OK**. The **Add Power Input File** dialog box appears.
8. Click **OK**.

9. (Optional) Turn on the **Write out signal activities used during power analysis** option. In the **Output file name** list, select the output file name. The output file contains all the signal activities information used during the power estimation of your design. Altera recommends turning on the **Write out signal activities used during power analysis** option you use a **.vcd** as input into the PowerPlay Power Analyzer, because it reduces the run time of any subsequent power estimation. You can use the generated **.saf** as input instead of the original **.vcd**.
10. (Optional) Turn on the **Write signal activities to report file** option.
11. (Optional) Turn on the **Write power dissipation by block to report file** option to enable the output of detailed thermal power dissipation by block to be included in the PowerPlay Power Analyzer report.
12. (Optional) You can also use the Assignment Editor to enter the **Power Toggle Rate** or **Power Toggle Rate Percentage**, and the **Power Static Probability** assignments for a node or entity in your design, shown in Figure 13–7.

Figure 13–7. Assignment Editor *(Notes 1), (2)*



Category: All

Node Filter: Click the Node Filter button to view more options

Information: This cell specifies the destination name for point-to-point assignments. For single-point assignments, this cell specifies the destination of the

Edit: ~DATA0~

	To	Assignment Name	Value	Enabled
1	~DATA0~	Power Toggle Rate	0	Yes
2	rdaddress1[2]	Power Static Probability		Yes
3	<<new>>	<<new>>		

Notes to Figure 13–7:

(1) The assignments made with the Assignment Editor override the existing values in the **.saf** or **.vcd**.

(2) You can also use Tcl script commands to create these assignments.

For more information about how to use the Assignment Editor in the Quartus II software, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*. For information about scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

13. Specify the toggle rate in the **Default toggle rate used for input I/O signals** field. This toggle rate is used for all unspecified input I/O signal toggle rates regardless of whether or not the device family supports vectorless estimation. By default, its value is set to 12.5%. The default static probability for unspecified input I/O signals is 0.5 and cannot be changed.

14. Select either **Use default value** or **Use vectorless estimation** for Arria GX, Cyclone II, Cyclone III, HardCopy II, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families. For all other device families, only **Use default value** is available. This setting controls how the remainders of the unspecified signal activities are calculated. For more information, refer to "Vectorless Estimation" on page 13–18 and "Default Toggle Rate Assignment" on page 13–18.

15. In the **Category** list, select **Operating Settings and Conditions**. This option is only available for the Arria GX, Cyclone II, Cyclone III, HardCopy II, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

16. In the **Device power characteristics** list, select **Typical** or **Maximum**.

17. In the **Category** list, click the "+" icon to expand **Operating Settings and Conditions** and click **Voltage**. The **Voltage** page appears.

18. For the devices with selectable core voltage support, in the **Core supply voltage** list, select the core supply voltage for your device. This option is available for the latest devices with variable voltage selection.

19. In the **Category** list, under **Operating Settings and Conditions,** select **Temperature**. The **Temperature** page appears.

20. Under **Junction temperature range**, specify a junction temperature in degrees Celsius and specify the junction temperature range. Select the **Low temperature** and **High temperature** range for your selected device.

21. Specify the junction temperature and cooling solution settings. You can select **Specify junction temperature** or **Auto compute junction temperature using cooling solution**.

22. (Optional) Under **Board thermal modeling**, select the **Board thermal model** and type the **Board temperature**. This feature can only be turned on when you have selected **Auto compute junction temperature using cooling solution**.

    For more information about how to use the operating condition settings, refer to "Operating Conditions" on page 13–9.

26. Click **OK**.

27. On the Processing menu, click **PowerPlay Power Analyzer Tool**. The **PowerPlay Power Analyzer Tool** dialog box appears.

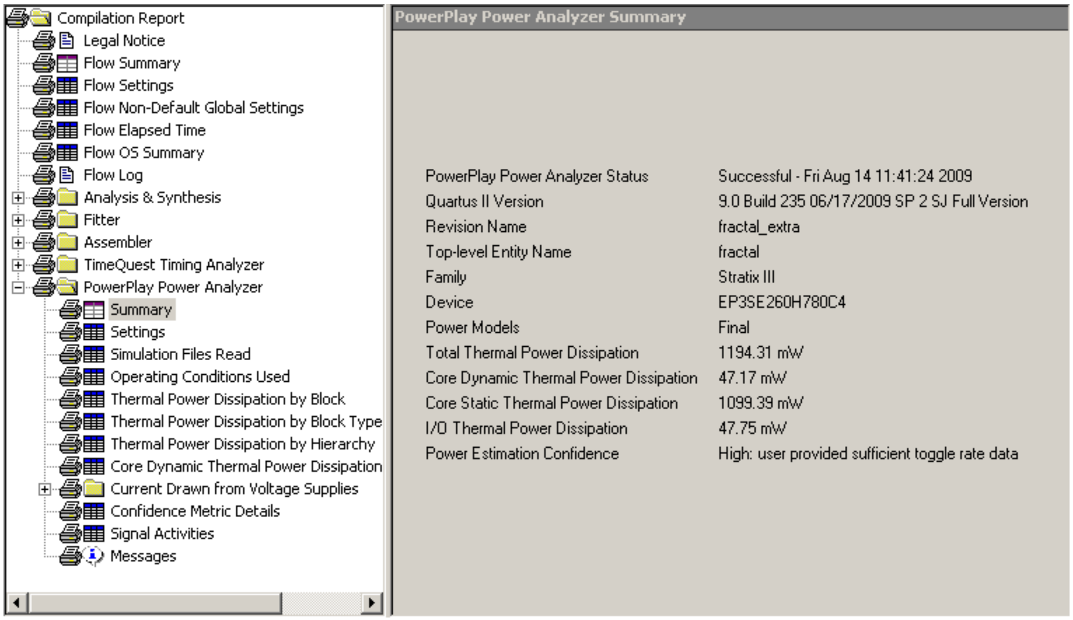
28. Click **Start** to run the PowerPlay Power Analyzer. Be sure that all the settings are correct.

    > You can also change some of your settings in the **PowerPlay Power Analyzer Tool** dialog box. For example, click **Add Power Input File(s)** to make changes to your input files, or click the **Cooling Solution and Temperature** to make changes to your design temperature and cooling solution selection.

29. Click **OK**.

30. In the **PowerPlay Power Analyzer Tool** dialog box, click **Report** to open the PowerPlay Power Analyzer Summary window. You can also view the summary in the **PowerPlay Power Analyzer Summary** page of the Compilation Report (Figure 13–8).

Figure 13–8. PowerPlay Power Analyzer Summary



PowerPlay Power Analyzer Status	Successful - Fri Aug 14 11:41:24 2009
Quartus II Version	9.0 Build 235 06/17/2009 SP 2 SJ Full Version
Revision Name	fractal_extra
Top-level Entity Name	fractal
Family	Stratix III
Device	EP3SE260H780C4
Power Models	Final
Total Thermal Power Dissipation	1194.31 mW
Core Dynamic Thermal Power Dissipation	47.17 mW
Core Static Thermal Power Dissipation	1099.39 mW
I/O Thermal Power Dissipation	47.75 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

PowerPlay Power Analyzer Compilation Report

The PowerPlay Power Analyzer section of the Compilation Report is divided into the following sections.

Summary

This section of the report shows the estimated total thermal power consumption of your design. This includes dynamic, static, and I/O thermal power consumption. The I/O thermal power consumption is the total I/O power contributed by both the V_{CCIO} power supplies and some portion of the V_{CCINT}. The report also includes a confidence metric that reflects the overall quality of the data sources for the signal activities. For example, a **Low** power estimation confidence value reflects that you have provided insufficient toggle rate data, or most of the signal activity information used for power estimation is from default or vectorless estimation settings (For more information about the input data, refer to the PowerPlay Power Analyzer Confidence Metric report).

Settings

This section of the report shows the PowerPlay Power Analyzer settings information of your design, including the default input toggle rates, operating conditions, and other relevant setting information.

Simulation Files Read

This section of the report lists simulation output files (**.vcd** or **.saf**) used for power estimation. This section also includes the file ID, file type, entity, VCD start time, VCD end time, the unknown percentage, and the toggle percentage. The unknown percentage indicates the portion of the design module that is not exercised by the simulation vectors.

Operating Conditions Used

This section of the report shows device characteristics, voltages, temperature, and cooling solution, if any, that were used during the power estimation. This section also shows the entered junction temperature or auto-computed junction temperature that was used during the power analysis. This page is created only for Arria GX, Cyclone II, Cyclone III, HardCopy II, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

Thermal Power Dissipated by Block

This section of the report shows estimated thermal dynamic power and thermal static power consumption categorized by atoms. This information provides you with estimated power consumption for each atom in their design.

Thermal Power Dissipation by Block Type (Device Resource Type)

This section of the report shows the estimated thermal dynamic power and thermal static power consumption categorized by block types. This information is further categorized by estimated dynamic and static power that was used, as well as providing an average toggle rate by block type. Thermal power is the power dissipated as heat from the FPGA device.

Thermal Power Dissipation by Hierarchy

This section of the report shows estimated thermal dynamic power and thermal static power consumption categorized by design hierarchy. This is further categorized by the dynamic and static power that was used by the blocks and routing in that hierarchy. This information is very useful in locating problem modules in your design.

Core Dynamic Thermal Power Dissipation by Clock Domain

This section of the report shows the estimated total core dynamic power dissipation by each clock domain. This provides designs with estimated power consumption for each clock domain in their design. If the clock frequency for a domain is unspecified by a constraint, the clock frequency is listed as “unspecified.” For all the combinational logic, the clock domain is listed as no clock with zero MHz.

Current Drawn from Voltage Supplies

This section of the report lists the current that was drawn from each voltage supply. The V_{CCIO} voltage supply is further categorized by I/O bank and by voltage. The minimum safe power supply size (current supply ability) is also listed for each supply voltage. This page is created only for Arria GX, Cyclone II, Cyclone III, HardCopy II, MAX II, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

The transceiver-based devices have multiple voltage supplies which are V_{CCH}, V_{CCT}, V_{CCR}, V_{CCA}, and V_{CCP}. The report also shows the static and dynamic current (in mA) drawn from each voltage supply. Total static and dynamic power consumed by the transceivers on all voltage supplies is listed under the “Thermal Power Dissipation by Block Type” report section, which contains a row that starts with “GXB Transceiver.”

The I/O thermal power dissipation which is listed on the summary page does not correlate directly to the power drawn from the V_{CCIO} voltage supply listed in this report. This is because the I/O thermal power dissipation value also includes portions of the V_{CCINT} power, such as the I/O element (IOE) registers which are modeled as I/O power, but do not draw from the V_{CCIO} supply.

Confidence Metric Details

The confidence metric indicates the quality of the signal toggle rate data used to compute a power estimate. The confidence metric is low if the signal toggle rate data comes from sources that are considered poor predictors of real signal toggle rates in the device during an operation. Toggle rate data that comes from simulation, user-entered assignments on specific signals, or entities are considered reliable. Toggle rate data from default toggle rates (for example, 12.5% of the clock period) or vectorless estimation are considered relatively inaccurate. This section gives an overall confidence rating in the toggle rate data, from low to high. This section also summarizes how many pins, registers, and combinational nodes obtained their toggle rates from each of simulation, user entry, vectorless estimation, or default toggle rate estimations. This detailed information helps you understand how to increase the confidence metric, letting you decide on your own confidence in the toggle rate data.

Signal Activities

This section lists toggle rate and static probabilities assumed by power analysis for all signals with fan-out and pins. The signal type is provided (pin, registered, or combinational), as well as the data source for the toggle rate and static probability. By default, all signal activities are reported. This can be turned off by turning off the **Write signal activities to report file** option on the P**owerPlay Power Analyzer Settings** page.

☞ Altera recommends turning off the **Write signal activities to report file** option for a large design because of the large number of signals present. You can use the Assignment Editor to specify that activities for individual nodes or entities are reported by assigning an on value to those nodes for the **Power Report Signal Activities** assignment.

Messages

This section lists the messages generated by the Quartus II software during the analysis.

Specific Rules for Reporting

In a Stratix GX device, the XGM II state machine block is always used together with GXB transceivers, so its power is lumped into the power for the transceivers. Therefore, the power for the XGM II state machine block is reported as zero Watts.

Scripting Support

You can run procedures and create settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For more information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp↵
```

The *Quartus II Scripting Reference Manual* includes the same information in PDF format.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. For more information about all settings and constraints in the Quartus II software, refer to the *Quartus II Settings File Reference Manual*. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Running the PowerPlay Power Analyzer from the Command Line

The separate executable that is used to run the PowerPlay Power Analyzer is `quartus_pow`. For a complete listing of all command line options supported by `quartus_pow`, type the following at a system command prompt:

```
quartus_pow --help or quartus_sh --qhelp ↵
```

The following is an example of using the `quartus_pow` executable with project **sample.qpf**:

- To instruct the PowerPlay Power Analyzer to generate a PowerPlay EPE file, type the following at a system command prompt:

  ```
  quartus_pow sample --output_epe=sample.csv ↵
  ```

- To instruct the PowerPlay Power Analyzer to generate a PowerPlay EPE file without performing the power estimate, type the following command at a system command prompt:

  ```
  quartus_pow sample --output_epe=sample.csv --
  estimate_power=off ↵
  ```

- To instruct the PowerPlay Power Analyzer to use a **.saf** as input (**sample.saf**), type the following at a system command prompt:

  ```
  quartus_pow sample --input_saf=sample.saf ↵
  ```

- To instruct the PowerPlay Power Analyzer to use two **.vcd** files as input files (**sample1.vcd** and **sample2.vcd**), perform glitch filtering on the **.vcd** and use a default input I/O toggle rate of 10,000 transitions per second, type the following at a system command prompt:

  ```
  quartus_pow sample --input_vcd=sample1.vcd --
  input_vcd=sample2.vcd \
  --vcd_filter_glitches=on --\
  default_input_io_toggle_rate=10000transitions/s ↵
  ```

- To instruct the PowerPlay Power Analyzer to not use any input file, a default input I/O toggle rate of 60%, no vectorless estimation, and a default toggle rate of 20% on all remaining signals, type the following at a system command prompt:

```
quartus_pow sample --no_input_file --
default_input_io_toggle_rate=60% \
--use_vectorless_estimation=off --default_toggle_rate=20% ↵
```

> ☞ There are no command line options to specify the information found on the **PowerPlay Power Analyzer Settings Operating Conditions** page. The easiest way to specify these options is to use the Quartus II GUI.

A report file, <*revision name*>**.pow.rpt**, is created by the `quartus_pow` executable and saved in the main project directory. The report file contains the same information as described in the "PowerPlay Power Analyzer Compilation Report" on page 13–26.

Conclusion

PowerPlay power analysis tools are designed for accurate estimation of power consumption from early design concept through design implementation. You can use the PowerPlay EPE to estimate power consumption during the design concept stage. Power estimations are refined during design implementation using the Quartus II PowerPlay Power Analyzer tool. The Quartus II PowerPlay Power Analyzer produces detailed reports that you can use to optimize designs for lower power consumption and verify that the design is in your power budget.

Referenced Documents

This chapter references the following documents:

- *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*
- *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*
- *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*
- *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*
- *Quartus II Settings File Reference Manual*
- *Quartus II Simulator* chapter in volume 3 of the *Quartus II Handbook*
- *Section I. Simulation* in volume 3 of the *Quartus II Handbook*
- *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 13–5 shows the revision history for this chapter.

Table 13–5. Document Revision History

Date and Version	Changes Made	Summary of Changes
November 2009 v9.1.0	■ Updated "Creating PowerPlay EPE Spreadsheets" on page 13–2 and "Simulation Results" on page 13–11. ■ Added "Signal Activities from Full Post-Fit Netlist (Zero Delay) Simulation" on page 13–19 and "Generating a .vcd from Full Post-Fit Netlist (Zero Delay) Simulation" on page 13–23. ■ Minor changes to "Generating a .vcd from ModelSim Software" on page 13–22. ■ Updated Figure 13–2 on page 13–3 and Figure 13–8 on page 13–26.	Updated for the Quartus II software version 9.1.
March 2009 v9.0.0	■ This chapter was chapter 11 in version 8.1. ■ Removed Figures 11-10, 11-11, 11-13, 11-14, and 11-17 from 8.1 version.	Updated for the Quartus II software version 9.0.
November 2008 v8.1.0	■ Updated for the Quartus II software version 8.1. ■ Replaced Figure 11-3. ■ Replaced Figure 11-14.	Updated for the Quartus II software version 8.1.
May 2008 v8.0.0	■ Updated Figure 11–5. ■ Updated "Types of Power Analyses" on page 11–5. ■ Updated "Operating Conditions" on page 11–9. ■ Updated "PowerPlay Power Analyzer Compilation Report" on page 11–31. ■ Updated "Current Drawn from Voltage Supplies" on page 11–32.	Updated for the Quartus II software version 8.0.

For previous versions of the *Quartus II Handbook*, refer to the Quartus II Handbook Archive.