

Introduction

Stratix® GX devices combine highly advanced 3.1875-gigabit-per-second (Gbps) four-channel gigabit transceiver blocks with one of the industry's most advanced FPGA architectures. Stratix GX devices are manufactured on a 1.5-V, 0.13- μ m, all-layer copper CMOS process technology with 1.5-V PCML I/O standard support.

Historically, designers have used high-speed transceivers in strictly structured, line-side applications. Now, with the new gigabit transceiver blocks embedded in FPGAs, you can use transceivers in a host of new systems that require flexibility, increased time-to-market, high performance, and top-of-the-line features.

Gigabit Transceiver Block Highlights

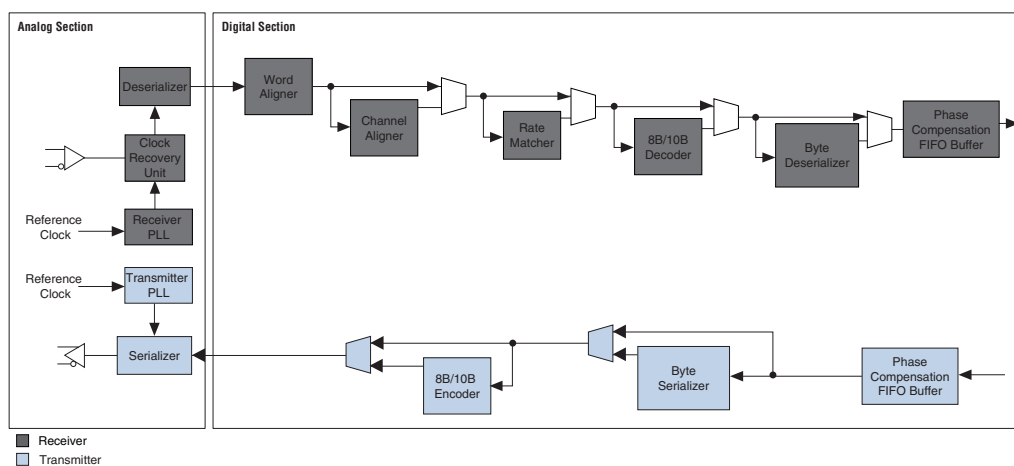
Stratix GX devices are organized into four-channel blocks with four 3.1875 Gbps full-duplex channels per block and up to 20 channels (in five blocks) per device. Each self-contained Stratix GX gigabit transceiver block supports a variety of embedded functions and does the following:

- Supports frequencies from 500 megabits per second (Mbps) to 3.1875 Gbps
- Integrates serializer/deserializer (SERDES), clock data recovery (CDR), word aligner, channel aligner, rate matcher, 8B/10B encoder/decoder, byte serializer/deserializer, and phase compensation first-in first-out (FIFO) modules
- Supports flexible reference clock generation capabilities, including a dedicated transmitter phase-locked loop (PLL) and four receiver PLLs per gigabit transceiver block
- Supports programmable pre-emphasis, equalization, and programmable V_{OD} settings in I/O buffers, and dynamic reprogrammability for each of these features
- Implements XAUI physical media attachment (PMA) and physical coding sublayer (PCS) functionality for 10GBASE-X systems
- Provides built-in Gigabit Ethernet (GigE) physical coding sublayer functionality
- Provides individual transmitter and receiver power-down capability for reduced power consumption during non-operation
- Includes built-in self test (BIST) capability, including embedded Pseudo Random Binary Sequence (PRBS) pattern generation and verification
- Includes three independent loopback paths for system verification

Transceiver Block Architecture

Figure 1-1 shows a block diagram of the gigabit transceiver block (GXB). You can bypass various modules if desired. Refer to “Modes of Operation” on page 1-5 for a description of the supported features in each mode. You can divide the transceiver block into an analog section and a digital section, as shown in Figure 1-1.

Figure 1-1. Block Diagram of a Stratix GX Gigabit Transceiver Block



Analog Section Overview

This section describes the various components within the analog section of the transceiver block.

Transmitter Differential I/O Buffers

The gigabit transmitter block differential I/O buffers support the 1.5-V PCML I/O standard, and contain features that improve system signal integrity. These features include programmable pre-emphasis, which helps compensate for high frequency losses, and a variety of programmable V_{OD} settings that support noise margin tuning.

Receiver Differential I/O Buffers

The gigabit transceiver block differential I/O buffers support the 1.5-V PCML I/O standard, and contain a variety of features that improve system signal integrity. Programmable equalization capabilities are used to compensate for signal degradation across transmission mediums.

Transmitter & Receiver PLLs

Each gigabit transceiver block contains one dedicated transmitter PLL and four dedicated receiver PLLs. These PLLs provide clocking flexibility and support a range of incoming data streams. For data transmission and recovery, these PLLs generate the required clock frequencies based upon the synthesis of an input reference clock. Each transmitter PLL supports multiplication factors of 2, 4, 5, 8, 10, 16, or 20. Either external reference clocks or a variety of clock sources within the Stratix GX device drive the PLLs.

Clock Recovery Unit

The gigabit transceiver block clock recovery unit (CRU) performs analog Clock Data Recovery (CDR). The CRU uses an external reference clock to extract a recovered clock that is frequency and phase aligned with the incoming data, thereby eliminating any clock-to-data skew. This recovered clock then clocks the data through the rest of the gigabit transceiver block.

Serializer Deserializer (SERDES)

The transmitter serializer converts the incoming lower speed parallel signal to a high-speed serial signal on the transmit side. The SERDES supports a variety of conversion factors, ensuring implementation flexibility. For example, the SERDES supports 10- and 20-bit serialization factors, typically required for 8B/10B encoded data, as well as 8- and 16-bit factors.

The receiver deserializer converts the incoming data stream from a high-speed serial signal to a lower-speed parallel signal that can be processed in the FPGA logic array on the receive side. The SERDES supports a variety of conversion factors, ensuring implementation flexibility. For example, the SERDES supports both 10-bit and 8-bit serialization and deserialization factors.

Digital Overview

This section describes the various components in the digital section of the transceiver block.

Transmitter & Receiver Phase Compensation FIFO Buffer

The transmitter and receiver data path has a dedicated phase compensation FIFO buffer that decouples phase variations between the FPGA and transceiver clock domains. These FIFO buffers ensure a consistent, reliable interface to the logic array and simplify system design and timing analysis.

Byte Serializer/Deserializer

The byte serializer converts a 16- or 20-bit data bus into two 8- or 10-bit data buses, respectively, at double the data rate.

The byte deserializer converts an 8- or 10-bit data bus into 16- or 20-bit data buses, allowing maximum throughput of the transceiver without burdening the FPGA logic array.

8B/10B Encoder/Decoder

8B/10B encoding/decoding is the backbone of many transceiver protocols, and it is often used in proprietary implementations. The gigabit transceiver block has dedicated circuitry to perform 8B/10B encoding in the transmitter and decoding in the receiver. This coding technique ensures sufficient data transitions and a DC balanced stream in the data signal for successful data recovery at the receiver.

Word Aligner

The word aligner module contains a fully programmable pattern detector to identify specific patterns within the incoming data stream. The pattern detector includes recognition support /K28.5/ comma characters for 8B/10B encoded data and A1 or A2 frame alignment patterns for scrambled signals. Additionally, you can specify a custom alignment pattern in lieu of the /K28.5/ comma.

The word aligner in the gigabit transceiver block also creates words from the incoming serial data stream by realigning the data based on identified byte boundaries. The realignment function uses a barrel shifter and works with the pattern detector. Additionally, the word aligner has a manual data realignment mode that lets you control the data realignment in user mode without consistent alignment characters.

Channel Aligner

An embedded channel aligner aligns byte boundaries across multiple channels and synchronizes the data entering the logic array from the gigabit transceiver block's four channels. The Stratix GX channel aligner is optimized for a 10-Gigabit Ethernet XAUI 4-channel implementation. The channel aligner includes the control circuitry and channel alignment character detection defined by the XAUI protocol. The channel aligner is only available in XAUI mode.

Rate Matcher

In multi-crystal environments, the clock frequencies of the transmitting and receiving devices do not match. This mismatch can cause the data to transmit at a rate slightly faster or slower than the receiving device can interpret. The Stratix GX rate matcher resolves the frequency differences between the recovered clock and the FPGA logic array clock by inserting or deleting removable characters from the data stream, as defined by the transmission protocol, without compromising transmitted data. If the functional mode is XAUI, the rate matcher is based on the 10-Gigabit Ethernet protocol. If the functional mode is GIGE, the rate matcher is based on the Gigabit Ethernet protocol.

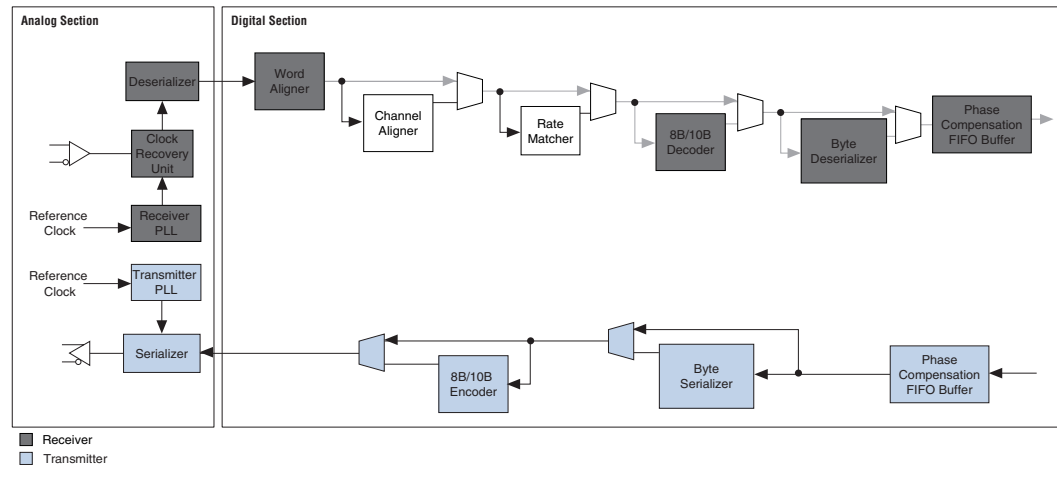
Modes of Operation

You can bypass various modules of the gigabit transceiver block based on the configured mode of operation. Stratix GX transceivers currently support Custom mode, SONET mode, and XAUI mode. This section provides an overview of each supported mode of operation.

Custom Mode

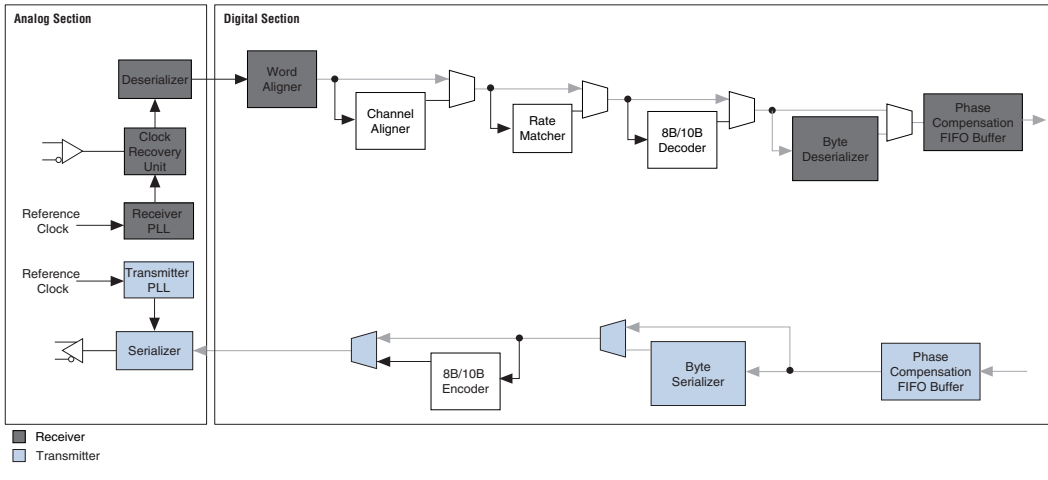
Custom mode enables a subset of the transceiver blocks so you can perform customizable configuration. Channel aligner and the rate matcher features are not available in this mode. Refer to the *Custom Mode* chapter for more details on the configurability of this mode. [Figure 1-2](#) shows a block diagram of a duplex channel configured in Custom mode.

Figure 1–2. Block Diagram of a Duplex Channel Configured in Custom Mode



SONET Mode

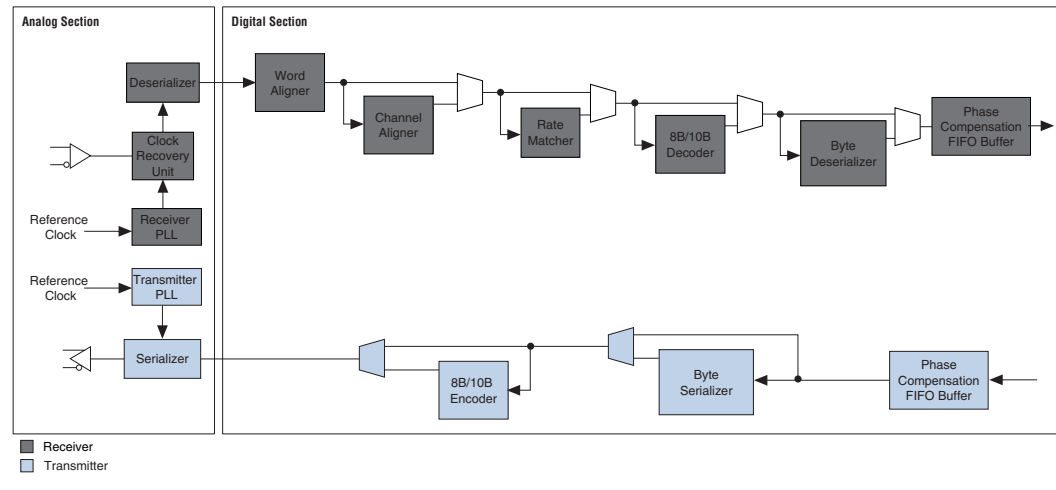
SONET mode lets you to select a subset of the transceiver blocks to perform SONET-like configuration. SONET-like implies that the data width can either be 8 or 16 bits and that the 8B/10B encoder/decoder, channel aligner, and the rate matcher features are not available. Refer to the *SONET Mode* chapter for more details on the configurability of this mode. [Figure 1–3](#) shows a block diagram of a duplex channel configured in SONET mode.

Figure 1–3. Block Diagram of a Duplex Channel Configured in SONET Mode

XAUI Mode

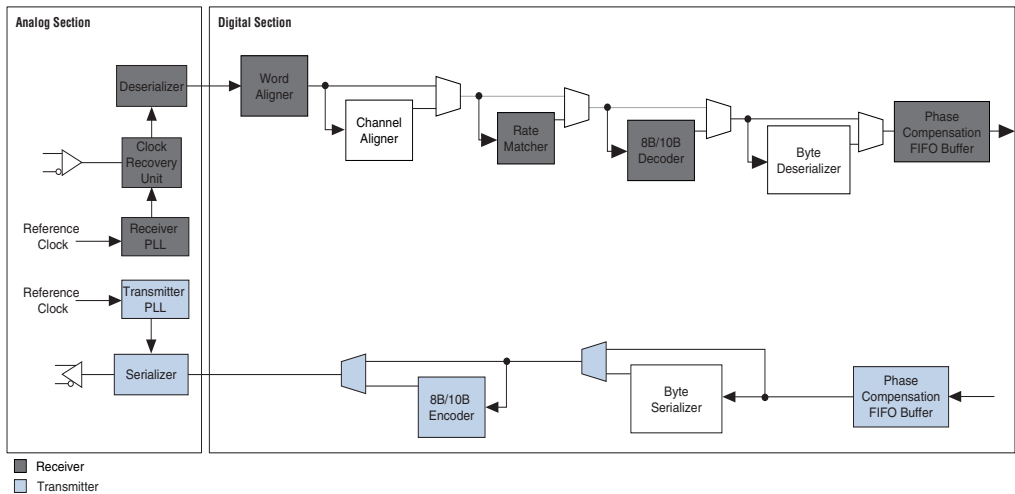
Stratix GX transceivers contain embedded macros dedicated to supporting the XAUI protocol, specified in clause 47 of the IEEE 802.3ae specification. These macros include synchronization, channel deskew, rate matching, XGXS to XGMII, and XGMII to XGXS code-group conversion. Refer to the *XAUI Mode* chapter for more details on the configurability of this mode. [Figure 1–4](#) shows a block diagram of a duplex channel configured in XAUI mode.

Figure 1–4. Block Diagram of a Duplex Channel Configured in XAUI Mode



GIGE Mode

Stratix GX devices in GIGE mode can use the 8B/10B encoder/decoder, rate matcher, synchronizer, and byte serializer/deserializer built-in hard macros. Refer to the *GIGE Mode* chapter of the *Stratix GX Device Handbook, Volume 2* for more information about this mode. The rate matcher and word aligner each have a dedicated state machine governing their functions. These state machines are active only in GIGE mode. Figure 1–5 shows a block diagram of a duplex channel configured in GIGE mode.

Figure 1–5. Block Diagram of a Duplex Channel Configured in GIGE Mode

Loopback

There are three different loopback modes to use in the gigabit transceiver block to allow for a complete method of in-system verification. The loopback modes are versatile and robust enough to accommodate all protocols and let you to choose whether to retime the data.

Built-In Self Test

The gigabit transceiver block contains several features that simplify design verification. An embedded PRBS pattern generator provides a bitstream pattern that you can use to test the device and board connections. The PRBS pattern generator works with a PRBS receiver to implement a full self-test path. Additionally, serial and parallel loopback paths let you test the FPGA logic without monitoring external signals. The reverse loopback path enables external system testing with minimal device interaction.

