

### Introduction

You can apply several loopback modes to the Stratix® GX block. The main forms of loopback are as follows:

- Serial loopback
- Parallel loopback
- Reverse serial loopback

Loopback refers to feeding the data from the transmitter directly to the receiver. Reverse loopback refers to feeding the data from the receiver directly to the transmitter. Serial loopback and parallel loopback feed data from the transmitter block to the receiver. Reverse serial loopback feeds the data from the receiver to the transmitter.

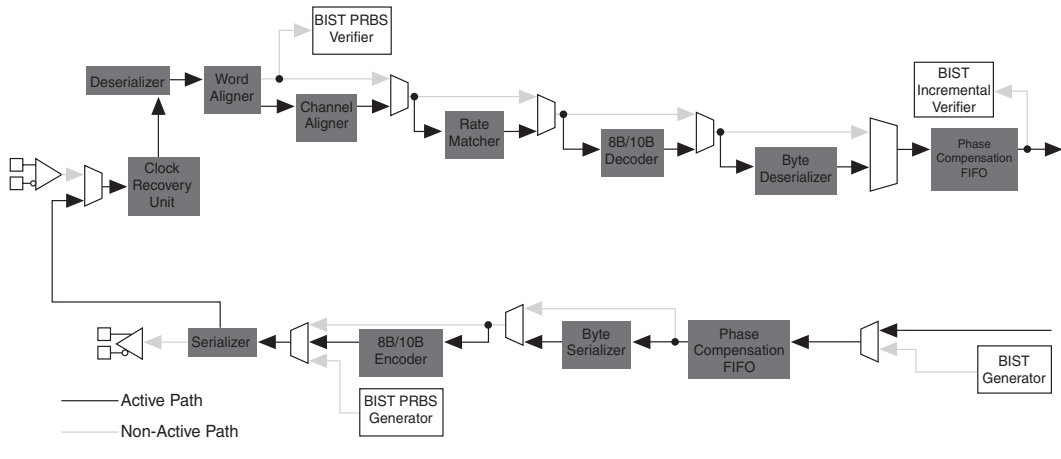
### Serial Loopback

Figure 7–1 shows the data path for serial loopback. A data stream is fed to the transmitter from the FPGA logic array and has the option of using all the blocks in the transmitter. The data then traverses from the transmitter in serial form to the receiver. The serial data is the data that is transmitted from the Stratix GX device. Once the data enters the receiver in serial form, it can use any of the receiver blocks and is then fed into the FPGA logic array. The PRBS block generates data when using serial loopback.

Serial loopback is dynamically enabled on a channel-by-channel basis using the `rx_slpbk` port. When serial loopback is enabled, the output swing is reduced on the `tx_out []` port except when the  $V_{OD}$  is set to 400 mV. In that case, the output is tri-stated.

Serial loopback is often used to check the analog portion of the transceiver. The data is retimed through different clock domains and an alignment pattern is still necessary for the word aligner.

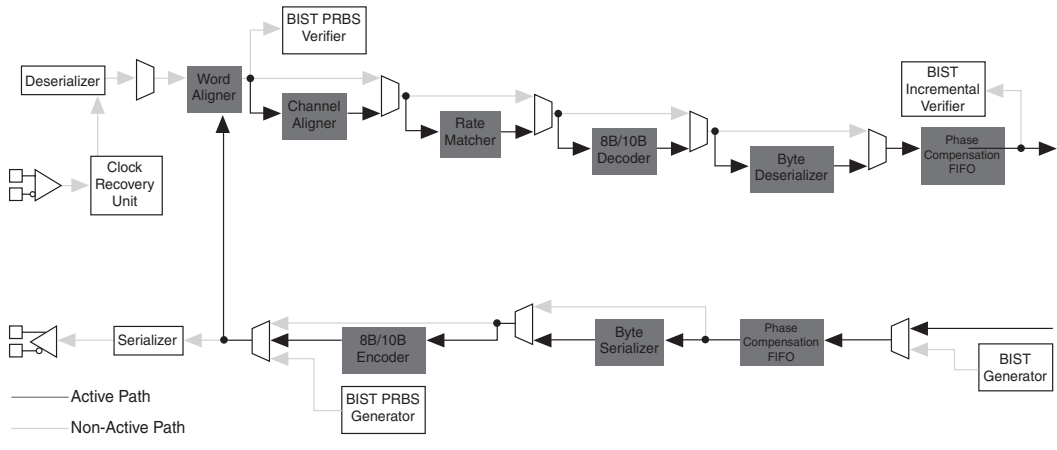
**Figure 7-1. Stratix GX Block in Serial Loopback Mode**



## Parallel Loopback

Figure 7-2 shows the data path for parallel loopback. A data stream is fed to the transmitter from the FPGA logic array and has the option of using blocks in the transmitter block. The data then exits the transmitter into the receiver in parallel form before entering the serializer. The data enters the receiver block after the deserializer and has the option of using any of the subsequent receiver blocks before being output by the receiver into the FPGA logic array. The PRBS block generates data. When using parallel loopback, the tx\_out ports are active, and the differential output voltage on the tx\_out ports is based on the current setting in the Quartus® II software or on the user setting.

Figure 7–2. Stratix GX Block in Parallel Loopback Mode



## Reverse Serial Loopback

Figure 7–3 shows the data path for reverse serial loopback. Data comes in from the `rx_in` ports in the receiver. The data is then fed through the CDR block in serial form directly to the `tx_out` ports in the transmitter block.

Reverse serial loopback is enabled for all channels through the software or is dynamically enabled on a channel-by-channel basis using the `tx_srlpbk` port. When using reverse serial loopback, the  $V_{OD}$  must be 400mV.

The reverse serial loopback is enabled but the logic array is still seeing data.

Reverse serial loopback is often implemented when using a Bit Error Rate Tester (BERT).

Figure 7-3. Stratix GX Block in Reverse Serial Loopback Mode

