

Input Ports

Table 11–1 lists the input ports of the Stratix® GX device.

<i>Table 11–1. Input Ports (Part 1 of 5)</i>			
Port Name	Required	Description	Comments
inclk []	See comments	Transceiver block transmitter PLL reference input clock.	Input port [NUMBER_OF_QUADS - 1..0] wide. If you use the transmitter PLL, the inclk [] port is required. If you set the OPERATION_MODE parameter to TX or DUPLEX, the inclk [] port is required.
pll_areset []	No	Asynchronous reset for the transceiver block transmitter PLL. This signal powers down the entire transceiver block. When placing reflckb pins, see the <i>REFCLKB Pin Constraints</i> chapter of the <i>Stratix GX Device Handbook, Volume 2</i> for information about analog reads and reflckb pin usage constraints.	Input port [NUMBER_OF_QUADS - 1..0] wide.
rx_in []	Yes	Transceiver block receiver channel data input port.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_cruclk []	No	Clock recovery unit (CRU) for the transceiver block receiver PLL reference input clock.	Input port [NUMBER_OF_QUADS - 1..0] wide. When you set the OPERATION_MODE parameter to TX or DUPLEX, the rx_cruclk [] port cannot be used. If you use this parameter, the transceiver block transmitter PLL cannot be instantiated.

Table 11–1. Input Ports (Part 2 of 5)

Port Name	Required	Description	Comments																		
rx_bitslip[]	No	Controls bit slipping circuitry in the word aligner.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. If you enable the rx_bitslip port, the rx_enacdet[] port cannot be connected and the USE_AUTO_BIT_SLIP parameter must be set to OFF.																		
rx_enacdet[]	No	Enables alignment to the programmed pattern.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. If you enable the rx_enacdet port, the rx_bitslip[] port cannot be connected, and the USE_AUTO_BIT_SLIP parameter must be set to ON.																		
rx_slpbk[]	No	Serial loopback input. Dynamically enables serial loopback from the transceiver block transmitter to the transceiver block receiver in the same channel.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. If you enable the rx_slpbk[] input port, the OPERATION_MODE parameter must be set to DUPLEX, and the serialfdbk port of the transceiver block receiver channel must be connected.																		
rx_ala2size[]	No	Detects A1A2 or A1A1A2A2 input patterns. If the signal is low (0), A1A2 patterns are detected. If the signal is high (1), A1A1A2A2 patterns are detected.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. If you enable the rx_ala2size[] port, the PROTOCOL parameter must be set to SONET.																		
rx_equalizerctrl[]	No	Specifies the equalizer control setting.	Input port [NUMBER_OF_CHANNELS * 3..0] wide. Use the following settings: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Incoming Signal</th> <th>Equalizer Control Setting</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> </tr> <tr> <td>001</td> <td>Reserved</td> </tr> <tr> <td>010</td> <td>1</td> </tr> <tr> <td>011</td> <td>Reserved</td> </tr> <tr> <td>100</td> <td>2</td> </tr> <tr> <td>101</td> <td>3</td> </tr> <tr> <td>110</td> <td>Reserved</td> </tr> <tr> <td>111</td> <td>4</td> </tr> </tbody> </table>	Incoming Signal	Equalizer Control Setting	000	0	001	Reserved	010	1	011	Reserved	100	2	101	3	110	Reserved	111	4
Incoming Signal	Equalizer Control Setting																				
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001	Reserved																				
010	1																				
011	Reserved																				
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101	3																				
110	Reserved																				
111	4																				

Table 11–1. Input Ports (Part 3 of 5)

Port Name	Required	Description	Comments
<code>rx_locktorefclk[]</code>	No	Control signal for transceiver block receiver PLL to lock to the reference clock.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
<code>rx_locktodata[]</code>	No	Control signal for transceiver block receiver PLL to lock the received data.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The <code>rx_locktodata[]</code> port can overwrite the <code>rx_locktorefclk[]</code> port.
<code>tx_in[]</code>	Yes	Transceiver block transmitter channel data input port.	Input port [CHANNEL_WIDTH * NUMBER_OF_CHANNELS - 1..0] wide. If you set the <code>USE_8B_10B_MODE</code> parameter to OFF and the <code>USE_DOUBLE_DATA_MODE</code> parameter is set to OFF, the deserialization factor is CHANNEL_WIDTH. If you set the <code>USE_8B_10B_MODE</code> parameter to OFF and the <code>USE_DOUBLE_DATA_MODE</code> parameter is set to ON, the deserialization factor is CHANNEL_WIDTH / 2. If you set the <code>USE_8B_10B_MODE</code> parameter to ON, the deserialization factor is 10.
<code>tx_ctrlenable[]</code>	No	Control character enable. Enables the 8B/10B encoder to identify control characters. Labels an input character as a control code.	Input port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If <code>tx_ctrlenable[]</code> port is high, the sent word is a control character.
<code>tx_forcedisparity[]</code>	No	Force disparity. When asserted HIGH after coming out of reset, forces the 8B/10B encoder to encode only the first byte after assertion with negative disparity.	Reassertion has no affect on the disparity unless the device is reset.

Table 11–1. Input Ports (Part 4 of 5)

Port Name	Required	Description	Comments																		
tx_srlpbk []	No	Reverse serial loopback input. Dynamically enables reverse serial loopback from the rx_in [] port to the tx_out [] port	Input port [NUMBER_OF_CHANNELS - 1..0] wide.																		
tx_vodctrl []	No	3-bit control signal that dynamically specifies the Voltage Output Differential (VOD) control settings.	Input port [NUMBER_OF_CHANNELS * 3 - 1..0] wide. Use the following settings: <table border="1"> <thead> <tr> <th>Incoming Signal</th> <th>VOD Control Setting</th> </tr> </thead> <tbody> <tr><td>000</td><td>400 mV</td></tr> <tr><td>001</td><td>800 mV</td></tr> <tr><td>010</td><td>1,000 mV</td></tr> <tr><td>011</td><td>1,200 mV</td></tr> <tr><td>100</td><td>1,400 mV</td></tr> <tr><td>101</td><td>1,600 mV</td></tr> <tr><td>110</td><td>1,600 mV</td></tr> <tr><td>111</td><td>1,600 mV</td></tr> </tbody> </table>	Incoming Signal	VOD Control Setting	000	400 mV	001	800 mV	010	1,000 mV	011	1,200 mV	100	1,400 mV	101	1,600 mV	110	1,600 mV	111	1,600 mV
Incoming Signal	VOD Control Setting																				
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011	1,200 mV																				
100	1,400 mV																				
101	1,600 mV																				
110	1,600 mV																				
111	1,600 mV																				
tx_preemphasisctrl []	No	3-bit control signal that dynamically specifies the pre-emphasis settings.	Input port [NUMBER_OF_CHANNELS * 3 - 1..0] wide. Use the following settings: <table border="1"> <thead> <tr> <th>Incoming Signal</th> <th>Pre-emphasis Setting</th> </tr> </thead> <tbody> <tr><td>000</td><td>0</td></tr> <tr><td>001</td><td>1</td></tr> <tr><td>010</td><td>2</td></tr> <tr><td>011</td><td>3</td></tr> <tr><td>100</td><td>4</td></tr> <tr><td>101</td><td>5</td></tr> <tr><td>110</td><td>5</td></tr> <tr><td>111</td><td>5</td></tr> </tbody> </table>	Incoming Signal	Pre-emphasis Setting	000	0	001	1	010	2	011	3	100	4	101	5	110	5	111	5
Incoming Signal	Pre-emphasis Setting																				
000	0																				
001	1																				
010	2																				
011	3																				
100	4																				
101	5																				
110	5																				
111	5																				
txdigitalreset []	No	Sends a reset signal to the digital portion of the transmitter.	Input port [NUMBER_OF_QUADS * 4 - 1..0] wide.																		
rxdigitalreset []	No	Sends a reset signal to the digital portion of the receiver.	Input port [NUMBER_OF_QUADS * 4 - 1..0] wide.																		
rxanalogreset []	No	Sends a power down signal to the analog portion of the receiver.	Input port [NUMBER_OF_QUADS * 4 - 1..0] wide.																		

Table 11–1. Input Ports (Part 5 of 5)

Port Name	Required	Description	Comments
pllenable []	No	Sends an enable signal to the transceiver block transmitter PLL.	Input port [NUMBER_OF_QUADS - 1..0] wide.
pll_areset []	No	Sends a power down signal to the transceiver block transmitter PLL.	Input port [NUMBER_OF_QUADS - 1..0] wide.

Output Ports

Table 11–2 lists the output ports of the Stratix GX device.

Table 11–2. Output Ports (Part 1 of 4)

Port Name	Required	Description	Comments
pll_locked []	No	Gives the status of the transceiver block transmitter PLL.	Output port [NUMBER_OF_QUADS - 1..0] wide. The pll_locked port is available only when the transceiver block transmitter PLL is used. The signal achieves lock status within several clock cycles in simulation. This does not necessarily reflect the real lock time in the hardware, which can take thousands of cycles for some settings.
coreclk_out []	No	Output clock fed by the clk2 port of the transceiver block transmitter PLL.	Output port [NUMBER_OF_QUADS - 1..0] wide. If a transceiver block transmitter PLL is used, the coreclk_out port must be enabled.
rx_out []	Yes	Transceiver block receiver PLL output data.	Output port [CHANNEL_WIDTH * NUMBER_OF_CHANNELS - 1..0] wide. If you set the USE_8B_10B_MODE parameter to OFF and the USE_DOUBLE_DATA_MODE parameter is set to OFF, the deserialization factor is CHANNEL_WIDTH. If you set the USE_8B_10B_MODE parameter to OFF and the USE_DOUBLE_DATA_MODE parameter is set to ON, the deserialization factor is CHANNEL_WIDTH / 2. If you set the USE_8B_10B_MODE parameter to ON, the deserialization factor is 10.

Table 11–2. Output Ports (Part 2 of 4)

Port Name	Required	Description	Comments
rx_clkout []	No	Output clock from the transceiver block receiver channel.	Output port [NUMBER_OF_CHANNELS - 1..0] wide. If you set the USE_RATE_MATCH_FIFO parameter to ON and the CLK_OUT_MODE_REFERENCE parameter is set to ON, the rx_clkout [] port is the PLL reference clock with the period $PLL_INCLOCK_PERIOD / DATA_RATE) * CHANNEL_WIDTH$. If you set the USE_RATE_MATCH_FIFO parameter to ON and the CLK_OUT_MODE_REFERENCE parameter is set to OFF, the rx_clkout [] port is the clock output of the PLL. If you set the USE_RATE_MATCH_FIFO parameter is OFF, the value of the rx_clkout [] port is the same as the value of the rx_recovclockout [] port. If you set the USE_DOUBLE_DATA_MODE parameter OFF, the clock period must be doubled, or the clock frequency must be halved.
rx_locked []	No	Gives the status of the transceiver block receiver channel atom.	Output port [NUMBER_OF_CHANNELS - 1..0] wide. Indicates that the transceiver block receiver PLL is locked to the reference input clock (active low). When the transceiver block receiver PLL is locked, this signal is GND. When the transceiver block receiver PLL is out of lock, this signal is VCC. The signal achieves lock status within several clock cycles in simulation. This does not necessarily reflect the real lock time in hardware, which can take thousands of cycles for some settings.
rx_channelaligned []	Yes	Channel alignment status for the transceiver block receiver channels.	Output port [NUMBER_OF_QUADS - 1..0] wide. If the PROTOCOL parameter is set to XAUI, the rx_channelaligned [] port must be connected.

Table 11–2. Output Ports (Part 3 of 4)

Port Name	Required	Description	Comments
<code>rx_freqlocked[]</code>	No	Indicates whether transceiver block receiver channel is locked to the data mode in the <code>rx_in[]</code> port.	Output port [NUMBER_OF_CHANNELS - 1..0] wide. This port is asserted when the GXB receiver PLL moves to lock to the received data mode. At that time, the clock recovery unit (CRU) for the GXB receiver PLL is frequency and phase-locked to the reference clock and starts using the phase detector to lock onto the incoming data, but it is not yet locked to the data. It takes a finite time before the CRU for the GXB receiver PLL is locked onto the data. The signal achieves lock status within several clock cycles in simulation. This does not necessarily reflect the real lock time in hardware, which can take thousands of cycles for some settings.
<code>rx_rlv[]</code>	No	Indicates whether the transceiver block receiver channel violated the value specified for the <code>RUN_LENGTH</code> parameter.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
<code>rx_syncstatus[]</code>	No	Provides the status of the pattern detector and word aligner.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If you set the <code>PROTOCOL</code> parameter to <code>XAUI</code> or <code>GIGE</code> , the <code>rx_syncstatus[]</code> port is connected to the synchronization state machine and indicates that the channel completed synchronization. If you set the <code>PROTOCOL</code> parameter to anything other than <code>XAUI</code> or <code>GIGE</code> , the <code>rx_syncstatus[]</code> port becomes a resync signal for manual synchronization of the alignment system.
<code>rx_patterndetect[]</code>	No	Indicates whether the pattern detector detected the programmed pattern.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide.
<code>rx_ctrldetect[]</code>	No	Indicates whether the 8B/10B decoder detects a control code.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If you set the <code>USE_8B_10B_MODE</code> parameter to <code>OFF</code> , the <code>rx_ctrldetect</code> port is not available.

Table 11–2. Output Ports (Part 4 of 4)

Port Name	Required	Description	Comments
<code>rx_errdetect []</code>	No	Indicates whether the 8B/10B decoder detects an error code.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If you set the <code>USE_8B_10B_MODE</code> parameter to OFF, the <code>rx_errdetect</code> port is not available.
<code>rx_disperr []</code>	No	Indicates whether the 8B/10B decoder detects a disparity error.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide.
<code>rx_signaldetect []</code>	No	Indicates whether there is a legal voltage level on the input buffer.	Output port [NUMBER_OF_CHANNELS - 1..0] wide. This port is available only if the <code>PROTOCOL</code> parameter is set to <code>XAUI</code> or <code>GIGE</code> . This signal is always set in the modes in which it is enabled. It is still enabled even after the signal is a forced HIGH for backward compatibility with existing designs.
<code>rx_bisterr []</code>	No	Error status signal for the self test.	Output port [NUMBER_OF_CHANNELS - 1..0] wide. This port is available only if the <code>USE_SELF_TEST_MODE</code> parameter is turned on.
<code>rx_bistdone []</code>	No	Indicates whether the self test is complete.	Output port [NUMBER_OF_CHANNELS - 1..0] wide. This port is available only if the <code>USE_SELF_TEST_MODE</code> parameter is turned on.
<code>rx_a1a2sizeout []</code>	No	Reports the <code>a1a2size</code> signal as seen by the word aligner.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide.
<code>tx_out []</code>	Yes	Serialized transceiver block transmitter channel data signal.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.

Parameter Descriptions

Table 11–3 describes the Stratix GX device parameters.

Parameter	Type	Required	Comments										
OPERATION_MODE	String	Yes	Specifies the operation of the transceiver block transmitter PLL and transceiver block receiver PLL. Values are RX, TX, and DUPLEX. If the PROTOCOL parameter is set to XAUI, then you must set the OPERATION_MODE parameter to DUPLEX.										
LOOPBACK_MODE	String	No	Specifies the operation of the loopback. Values are NONE, SLB, and PLB. If omitted, the default is NONE. Values other than NONE are available only when the OPERATION_MODE parameter is set to DUPLEX.										
REVERSE_LOOPBACK_MODE	String	No	Specifies the operation of the reverse loopback. Values are NONE, and RSLB. If omitted, the default is NONE. Values other than NONE are available only when the OPERATION_MODE parameter is set to DUPLEX.										
PROTOCOL	String	Yes	Specifies the protocol. Values are XAUI, SONET, GIGE, and Custom.										
NUMBER_OF_CHANNELS	Integer	Yes	Specifies the number of transceiver block receiver or transmitter channels. Values are 1 through 20.										
NUMBER_OF_QUADS	Integer	Yes	Specifies the number of transceiver blocks.										
CHANNEL_WIDTH	Integer	Yes	<p>Specifies the width of the dataout signal from the transceiver block receiver or transmitter channel atom. Use the following settings:</p> <table border="1"> <thead> <tr> <th>Setting of PROTOCOL Parameter</th> <th>Channel Width Values</th> </tr> </thead> <tbody> <tr> <td>XAUI</td> <td>16</td> </tr> <tr> <td>SONET</td> <td>8 and 16</td> </tr> <tr> <td>GIGE</td> <td>8</td> </tr> <tr> <td>Custom</td> <td>8, 10, 16, and 20</td> </tr> </tbody> </table> <p>For more information, see the table in the comments for the DATA_RATE parameter.</p>	Setting of PROTOCOL Parameter	Channel Width Values	XAUI	16	SONET	8 and 16	GIGE	8	Custom	8, 10, 16, and 20
Setting of PROTOCOL Parameter	Channel Width Values												
XAUI	16												
SONET	8 and 16												
GIGE	8												
Custom	8, 10, 16, and 20												

Table 11–3. Parameter Descriptions (Part 2 of 6)

Parameter	Type	Required	Comments
PLL_INCLOCK_PERIOD	Integer	Yes	Specifies, in picoseconds (ps), the period or frequency of the transceiver block transmitter PLL. If omitted, the default is 0. The value of this parameter is used to compute the input clock frequency in MHz; $(1 / \text{PLL_INCLOCK_PERIOD}) * 1,000,000$. When you specify PLL_INCLOCK_PERIOD, the CRU_INCLOCK_PERIOD parameter cannot be used. For more information, see the table in the comments for the DATA_RATE parameter.
DATA_RATE	Integer	Yes	Specifies, in Mbps, the rate of data from the transceiver block transmitter channel and the transceiver block receiver channel. If omitted, the default is 0.
DATA_RATE_REMAINDER	Integer	No	Specifies, in bits per second (bps), the remainder of the DATA_RATE parameter; $\text{DATA_RATE} * 1,000,000$. This parameter helps to specify non-integral data rates. If omitted, the default is 0.
USE_DOUBLE_DATA_MODE	String	No	Specifies whether to use double data width mode. If you enable this parameter, the CHANNEL_WIDTH parameter value is 16 or 20. When the CHANNEL_WIDTH parameter value is 8 or 10, the transceiver block receiver channel is not in double data width mode. Values are ON and OFF. If omitted, the default is OFF.
USE_8B_10B_MODE	String	No	Specifies whether to use the 8B/10B decoder. If this parameter is turned on, the deserialization factor is 10, and the CHANNEL_WIDTH parameter value is 8 or 16. Values are ON and OFF. If omitted, the default is OFF.
DWIDTH_FACTOR	Integer	No	Specifies the width of the double data factor. Values are 1 and 2. If omitted, the default is 1. A value of 1 means that value of the USE_DOUBLE_DATA_MODE parameter is OFF, and a value of 2 means that value of the USE_DOUBLE_DATA_MODE parameter is ON.
CRU_INCLOCK_PERIOD	Integer	No	Specifies, in picoseconds (ps), the period or frequency of the transceiver block receiver PLL. If omitted, the default is 0. The value of this parameter computes the input clock frequency in MHz; $(1 / \text{CRU_INCLOCK_PERIOD}) * 1,000,000$. When you specify the CRU_INCLOCK_PERIOD, the PLL_INCLOCK_PERIOD parameter cannot be used. For more information, see the table in the comments for the DATA_RATE parameter.

Table 11–3. Parameter Descriptions (Part 3 of 6)

Parameter	Type	Required	Comments
RUN_LENGTH	Integer	No	Specifies the maximum run length supported for the incoming data signal. This parameter is ignored if the RUN_LENGTH_ENABLE parameter is turned off. If the deserialization factor is 8, legal values are 4–128, in multiples of four. If the deserialization factor is 10, legal values are 5–160, in multiples of five. If omitted, the default is 0.
RUN_LENGTH_ENABLE	String	No	Specifies whether to use run length detection. Values are ON and OFF. If omitted, the default is OFF.
USE_CHANNEL_ALIGN	String	No	Specifies whether to use the channel aligner and enable the deskew system. The USE_CHANNEL_ALIGN parameter can only be used when the PROTOCOL parameter is set to XAUI. Values are ON and OFF. If omitted, the default is OFF.
USE_AUTO_BIT_SLIP	String	No	Specifies whether to use internal bit slipping circuitry. If you enable this parameter, the bit slip transceiver block receiver channel is ignored, and an internal register controls the byte alignment functions. If this parameter is turned off, the bit slipping operation is controlled by the rx_bitslip[] signal. Values are ON and OFF. If omitted, the default is OFF.
USE_SYMBOL_ALIGN	String	No	Specifies whether to use the word aligner. Values are ON and OFF. If omitted, the default is ON.
ALIGN_PATTERN	String	No	Specifies the pattern of 7, 10, or 16 bits used by the word aligner for the USE_SYMBOL_ALIGN parameter. If the USE_SYMBOL_ALIGN parameter is turned off, this parameter is ignored. If the PROTOCOL parameter is set to XAUI or GIGE, the only legal pattern is 0101111100.
ALIGN_PATTERN_LENGTH	Integer	No	Specifies the length of the ALIGN_PATTERN parameter. Values are 7, 10, or 16. If omitted, the default is 0.
CLK_OUT_MODE_REFERENCE	String	No	Specifies whether to use the clock that operates the post rate matching FIFO module of the transceiver block receiver channel. This parameter is ignored if the USE_RATE_MATCH_FIFO parameter is turned off. Values are ON and OFF. If omitted, the default is OFF.
USE_SELF_TEST_MODE	String	No	Indicates whether to use the built-in self test mode. Values are ON and OFF. If omitted, the default is OFF.

Table 11–3. Parameter Descriptions (Part 4 of 6)

Parameter	Type	Required	Comments												
SELF_TEST_MODE	Integer	No	Indicates which self test mode to use. Values are 0, 1, 2, 3, or 4. If omitted, the default is 0. This parameter is ignored if the USE_SELF_TEST_MODE parameter is turned off. Use the following settings: <table style="margin-left: 40px;"> <thead> <tr> <th>Value</th> <th>Test</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PRBS</td> </tr> <tr> <td>1</td> <td>00-FF, followed by 5 K28.5+ and repeat</td> </tr> <tr> <td>2</td> <td>High frequency pattern, repeat of D21.5- D21.5+</td> </tr> <tr> <td>3</td> <td>Low frequency pattern, repeat of K28.7- K28.7+</td> </tr> <tr> <td>4</td> <td>Mixed frequency pattern, repeat of K28.5- K28.5+</td> </tr> </tbody> </table>	Value	Test	0	PRBS	1	00-FF, followed by 5 K28.5+ and repeat	2	High frequency pattern, repeat of D21.5- D21.5+	3	Low frequency pattern, repeat of K28.7- K28.7+	4	Mixed frequency pattern, repeat of K28.5- K28.5+
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3	Low frequency pattern, repeat of K28.7- K28.7+														
4	Mixed frequency pattern, repeat of K28.5- K28.5+														
USE_EQUALIZER_CTRL_SIGNAL	String	No	Specifies whether to use the equalizer control signal. Values are ON and OFF. If omitted, the default is OFF.												
EQUALIZER_CTRL_SETTING	Integer	No	Specifies the magnitude of the equalizer control settings. Refer to the Quartus® II help menu for more information regarding the variable values. This parameter should be specified if the USE_EQUALIZER_CTRL_SIGNAL parameter is turned off.												
SIGNAL_LOSS_THRESHOLD_SELECT	Integer	No	Specifies the signal loss threshold. Refer to the Quartus II software Help menu for more information about the variable values.												
PLL_BANDWIDTH_TYPE	String	No	Specifies the transceiver block receiver PLL or the transceiver block transmitter bandwidth type. Values are LOW and HIGH. If omitted, the default is HIGH.												
RX_BANDWIDTH_TYPE	String	No	Specifies the transceiver block receiver PLL bandwidth type. Values are LOW and HIGH. If omitted, the default is HIGH.												
PLL_ENABLE_DC_COUPLING	String	No	Specifies whether to enable DC coupling on the transceiver block transmitter PLL clock input. Values are ON and OFF. If omitted, the default is OFF.												
RX_ENABLE_DC_COUPLING	String	No	Specifies whether to enable DC coupling on the transceiver block receiver PLL data input. Values are ON and OFF. If omitted, the default is OFF.												
USE_VOD_CTRL_SIGNAL	String	No	Specifies whether the VOD control signal is used. If this parameter is turned on, the tx_vodctrl port is used and the VOD_CTRL_SETTING parameter is ignored. Values are ON and OFF. If omitted, the default is OFF.												

Table 11–3. Parameter Descriptions (Part 5 of 6)

Parameter	Type	Required	Comments
VOD_CTRL_SETTING	Integer	No	Specifies, in mV, the value of the V _{OD} control signal. Values are 400, 800, 1000, 1200, 1400, 1600. If omitted, the default is 1000.
USE_PREAMPHASIS_CTRL_SIGNAL	String	No	Specifies whether the pre-emphasis control signal is used. If you enable this parameter, the tx_preamphasisctrl port is used and the PREAMPHASIS_CTRL_SETTING parameter is ignored. Values are ON and OFF. If omitted, the default is OFF.
PREAMPHASIS_CTRL_SETTING	Integer	No	Specifies, as a percentage of the V _{OD} control setting, the value of the pre-emphasis control signal. Values are 0, 1, 2, 3, 4, or 5. If omitted, the default is 0.
USE_RX_CLKOUT	String	No	Specifies whether the output clock from the transceiver block receiver channel is used. Values are ON and OFF. If omitted, the default is OFF. If you enable this parameter, the rx_clkout port must be used.
USE_RX_CRUCLK	String	No	Specifies whether the clock recovery unit (CRU) is used for the transceiver block receiver PLL reference input clock. Values are ON and OFF. If omitted, the default is OFF. If you enable this parameter, the rx_cruclk port must be used.
RX_PPM_SETTING	Integer	No	Specifies the value of the PPM threshold between the transceiver block receiver PLL VCO and the clock recovery unit (CRU). Values are 125, 250, 500, or 1000. If omitted, the default is 1000.
RX_FORCE_SIGNAL_DETECT	String	No	Specifies whether the rx_signaldetect[] port is used. Values are ON and OFF. If omitted, the default is ON.
USE_RX_CORECLK	String	No	Specifies whether the rx_coreclk[] port is used. Values are ON and OFF. If omitted, the default is OFF.
USE_TX_CORECLK	String	No	Specifies whether the tx_coreclk[] port is used. Values are ON and OFF. If omitted, the default is OFF.
FLIP_RX_OUT	String	No	Specifies whether the transceiver block receiver channel output data bits are flipped. Values are ON and OFF. If omitted, the default is OFF.
FLIP_TX_IN	String	No	Specifies whether the transceiver block transmitter channel input data bits are flipped. Values are ON and OFF. If omitted, the default is OFF.
INSTANTIATE_TRANSMITTER_PLL	String	No	Specifies whether the transceiver block transmitter PLL is instantiated. Values are ON and OFF. If omitted, the default is OFF.

Table 11–3. Parameter Descriptions (Part 6 of 6)													
Parameter	Type	Required	Comments										
CONSIDER_INSTANTIATE_TRANSMITTER_PLL	String	No	Specifies whether the INSTANTIATE_TRANSMITTER_PLL parameter is turned on. Values are ON and OFF. If omitted, the default is OFF.										
TX_TERMINATION	Integer	No	<p>Specifies the termination setting on the pin fed by the transceiver block transmitter channel tx_out [] port. Values are 0, 1, 2, or 3. If omitted, the default is 2. Use the following settings:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Termination Setting</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>150 Ω</td> </tr> <tr> <td>1</td> <td>120 Ω</td> </tr> <tr> <td>2</td> <td>100 Ω</td> </tr> <tr> <td>3</td> <td>External termination</td> </tr> </tbody> </table>	Value	Termination Setting	0	150 Ω	1	120 Ω	2	100 Ω	3	External termination
Value	Termination Setting												
0	150 Ω												
1	120 Ω												
2	100 Ω												
3	External termination												
RX_DATA_RATE	Integer	No	Specifies, in Mbps, the rate of data from the GXB receiver channel. If omitted, the default is 0.										
RX_DATA_RATE_REMAINDER	Integer	No	Specifies, in bits per second (bps), the remainder of the RX_DATA_RATE parameter; $RX_DATA_RATE * 1000000$. This parameter helps to specify non-integral data rates. If omitted, the default is 0.										
INTENDED_DEVICE_FAMILY	String	No	Use this parameter for modeling and behavioral simulation purposes. Create the altgxb megafunction with the MegaWizard® Plug-in Manager to calculate the value for this parameter.										