

Introduction

The Stratix® GX device does not have delay information for the following paths:

- Transmitter PLL input clock to `coreclk_out`
- Reference clock pin (`inclk`) to the transmitter PLL
- Reference clock pin (`rx_crucclk`) to `rx_clkout` (recovered clock)
- Reference clock pin (`rx_crucclk`) to the receiver PLL
- Interquad (IQ) lines (in a multi-transceiver block application, if the clocking scheme utilizes interquad lines for clock distribution or routing, IQ lines are not modeled)

The Fitter in the Quartus® II software generates warning messages for paths that involve these clocks or IQ lines. The warning messages state clearly that the connections are not recommended because accurate delay information is not available.

There are three starting points for the checks:

- Transmitter PLL `coreclk_out`
- Receiver PLL `rx_clkout`
- IQ lines used for clocking the reference clock of transceivers (`refclkb` pins)

The warnings are specific to any path with one of the three starting points. The warnings appear in the Fitter's processing log and are associated with unreliable timing paths that contain the following:

- Incorrect clock to output time (t_{CO})
- Incorrect propagation delay (t_{PD})
- Incorrect register-to-register timing

The warnings generated by the Fitter fall into four categories and are associated with the following:

- Signals that originate from the GXB connected to an IO pin or a signal that originates from the GXB that feeds through a register to an IO pin
- Data that originates from a pin that is clocked by a clock that originates from the GXB

- A clock from one of the starting points feeds a register that is involved in a register-to-register transfer and the destination register is being clocked by a clock related to the starting point
- IQ delay line warnings because the design uses REFCLKB pins for reference clocks when using multiple transceivers in the device



Altera® strongly recommends that you review and resolve the warnings generated by the Fitter in the Quartus II software.

If the starting point is the transmitter PLL, the Fitter in the Quartus II software generates the warning messages for the following configurations:

- t_{PD} warning messages
The starting point (GXB Transmitter PLL `coreclk`) feeds an I/O pin directly. This configuration causes the Fitter to incorrectly report t_{PD} . [Figure 5-1](#) shows the t_{PD} (propagation delay) from `inclk` to the transmitter PLL through `coreclk_out` to the IO pin. Some example warnings are provided below.

Warning: Clock connectivity to I/O pins from a GXB transmitter PLL `coreclk` is not recommended

Warning: I/O pin `coreclk_out` is fed by GXB transmitter PLL<*design-specific path*>

- t_{CO} warning messages
The starting point feeds an I/O register directly. This configuration causes the Fitter to incorrectly report t_{CO} . Clock connectivity to I/O pins through registers originating from a GXB transmitter PLL `coreclk` is not recommended (see [Figure 5-1](#)). In this case, `coreclk_out` from the transmitter PLL clocks a register (`inst3`) and the output of that register is connected directly to an output pin. Because `coreclk_out` is related to `inclk` and there is no delay information from `inclk` through the transmitter PLL to `coreclk_out`, the Fitter reports incorrect t_{CO} .

The Fitter flags a warning if any similar type of connectivity occurs. An example warning is shown below.

Warning: Register `inst3` clocked by GXB transmitter PLL<*design-specific path*>

- t_{SU} and t_{H} messages:
The starting point feeds a register that is involved in a register-to-register transfer from a register that is clocked by a clock related to the starting point. In this configuration, the Fitter performs

incorrect register-to-register analysis. This could result in the Fitter providing incorrect t_{SU} (setup time) and t_H (hold time). Register-to-register transfer between different clock domains is not recommended if one of the clocks is from either the GXB transmitter PLL (`coreclk`) or from the receiver PLL (`rx_clkout`). In the example warning shown below, there is a clock domain crossing between `inclk` (the starting point) and `coreclk_out` (the clock related to the starting point)

Warning: Data is transferred from source register `inst4` (clocked by clock `inclk`) to destination register `inst3` (clocked by the GXB transmitter PLL `<design-specific path>`).

Figure 5-1 highlights the paths that trigger warning messages from the Fitter. The Fitter reports an incorrect path delay for these paths.

t_{CO} delays are also incorrect for these paths (any register that is being clocked by `coreclk_out`).

The Fitter generates register-to-register warning messages because of the clock domain crossing from `inclk` (input clock to the transmitter PLL) to `coreclk_out` (output of the transmitter PLL).

Figure 5-1. Transmit PLL `coreclk_out` Showing t_{PD} & t_{CO} Registers

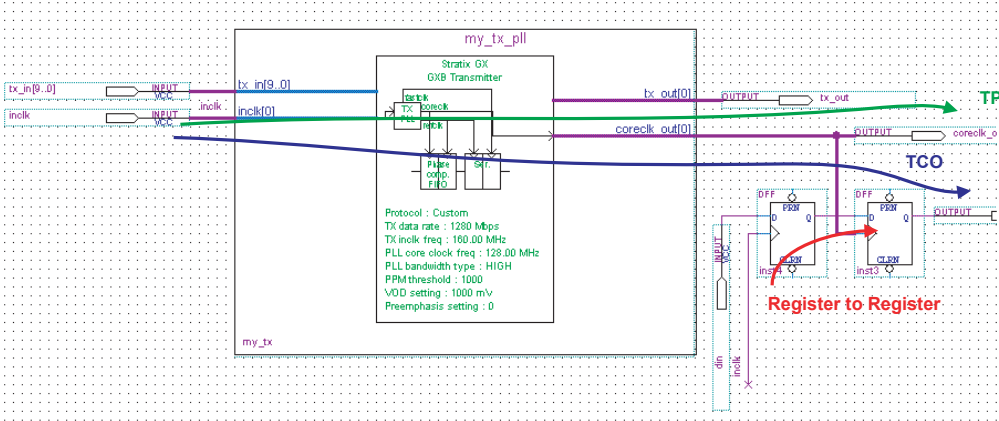
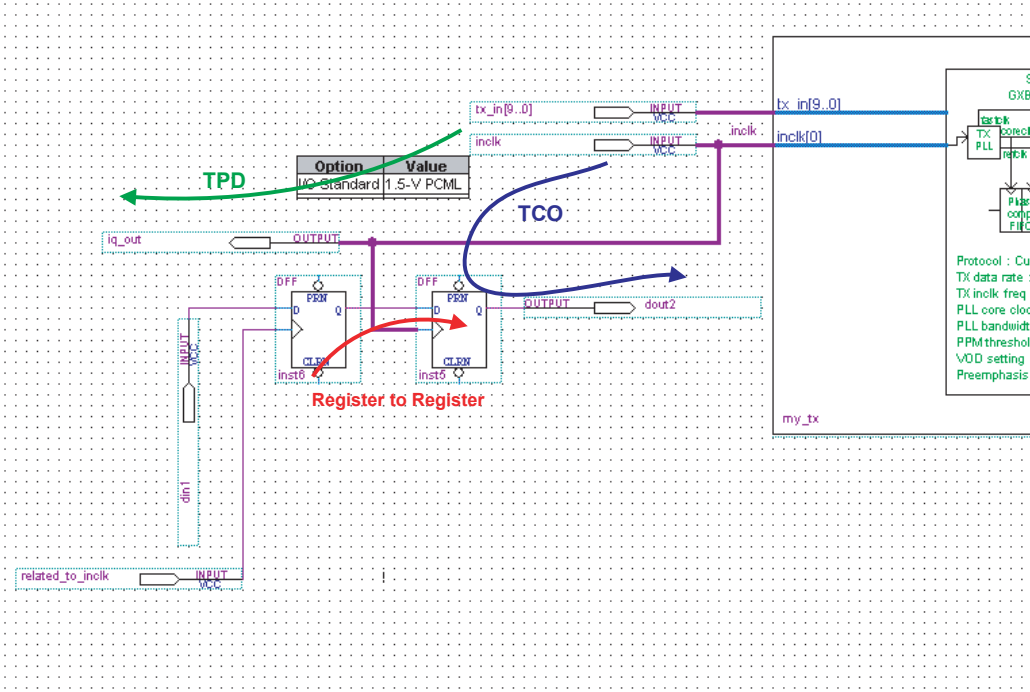


Figure 5-2 shows the t_{PD} (propagation delay) from `rx_crucclk` through the receiver PLL, through `rx_clkout`, and to the I/O pin. The Fitter reports an incorrect path delay for this path.

Figure 5–3. Multi-Transceiver Block Clcking Using IQ Lines Showing t_{PD} & t_{CO} Registers



Suppressing Fitter Warnings

Altera strongly recommends that you review the paths that generate the warning messages. If you decide on this connectivity for design purposes after evaluating the warnings, you can suppress the Fitter warnings.

Use the **Cut** command (in the Assignment Editor for the specific path) to suppress these warnings. The command suppresses the messages in the Fitter and instructs the Timing Analyzer to not perform timing analysis on these paths.

Design Suggestions

This section offers some possible design solutions to help you avoid the paths that cause errors and generate warnings.

Register-to-Register Warnings

If the warning messages generated by the Fitter are of type register-to-register, you should revisit the clock scheme and data path to effectively decouple different clock domains. You do this by clock-decoupling logic and FIFOs as required.

Registers Originating From GXB Connected to IO Pins

Avoid this connectivity as much as possible. If the clocking scheme cannot be changed because of design requirements, then you must resolve this issue at the pin level of the receive device. The receiver on the other end must include some type of dynamic phase adjustment of the clock with respect to the data bus.

In some cases, you might monitor certain GXB signals for test and debug purposes. If you feed these signals to an I/O pin for monitoring, you can suppress the warnings by using the **Cut** command.

Using REFCLKB Pins for Input Reference Clock

If you assign a REFCLKB pin as the input reference clock, the Fitter automatically routes the input using IQ lines. The *Stratix GX Analog Description* chapter of the *Stratix GX Device Handbook, Volume 2* provides information on how IQ lines help in clocking multiple transceivers with one REFCLKB pin and its connectivity across multiple quads. Because of the lack of accurate delay information on IQ lines (used to route the clocks to different transceivers in the device), you should use global clocks for the input reference clock to the transceivers as much as possible (try to avoid using REFCLKB pins). Applications that are sensitive to jitter typically use IQ lines because they are exclusive routing resources for transceivers.

It is not necessary to avoid using REFCLKB pins entirely, but be aware of the issues of using IQ lines for routing input clocks.



Refer to the *REFCLKB Pin Constraints* chapter of the *Stratix GX Device Handbook, Volume 2* before using REFCLKB pins for system clocking.



Refer to the *Stratix GX Transceiver User Guide* section of the *Stratix GX Handbook, Volume 2* for details on the various clocks and functional modes of operation of the Stratix GX device.

You can use decoupling FIFOs to address the lack of delay information. The transmit clock can be an external clock (`tx_coreclk`) from the PLD or an internal clock (output from the transmitter PLL). On the receive side, it can be either `rx_coreclk` fed from the PLD or various internal

clocks clocking out the data. In a synchronous system, the decoupling FIFOs must be able to handle phase differences between the clock domains of GXB output clocks (`rx_clkout`) and the PLD system clock. In asynchronous systems, the decoupling FIFOs must also compensate for frequency variations between the recovered clock (`rx_clkout`) and the PLD system clock. See the *Stratix GX Transceiver User Guide* section of the *Stratix GX Device Handbook, Volume 2* for information on possible clocking configurations.

PLD-to-Transceiver Clocking

Figure 5-4 shows a system-level clocking scheme you can use to work around the issues described in this chapter. This clocking scheme may not be the most optimal for designs that have tight jitter requirements because of cascading PLLs.

Figure 5-4. PLD & Transceiver Clocking Scheme

