



# Upcoming Stratix IV Device Features

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Upcoming Features

This document lists the Stratix<sup>®</sup> IV device features that include transceivers, LVDS, and memory interfaces, which will be enabled in future Quartus<sup>®</sup> II software versions. It provides a high-level overview of the upcoming features.

## Transceiver Analog Power ( $V_{CCA\_L/R}$ )

$V_{CCA\_L/R}$  is the transceiver analog power that provides power to the PMA blocks in all the Stratix IV GX transceiver channels. Separate  $V_{CCA}$  pins ( $V_{CCA\_L}$  and  $V_{CCA\_R}$ ) are provided for the transceiver channels on the left and right side of the device, respectively.

### Current Support

The available option for the  $V_{CCA\_L/R}$  supply is 3.0 V.

### Future Support

The ALTGX MegaWizard<sup>®</sup> Plug-In Manager (**Ports/Cal Blk** screen) will support 2.5 V as an option for transceiver analog power. When the  $V_{CCA\_L/R}$  option is set to 2.5 V, all transceiver channels on that side can run from 600 Mbps to 4.25 Gbps data rate. The  $V_{CCA\_L/R}$  setting of 2.5 V will not support LC tank PLLs. This additional option of 2.5 V is intended for sharing power supplies (simplification of power distribution network on the board) to Stratix IV devices.

## Transmitter Buffer Supply ( $V_{CCH}$ )

$V_{CCH}$  is the transmitter buffer supply voltage available per transceiver block.

### Current Support

The available option for  $V_{CCH}$  supply is 1.4 V. The I/O standard of 1.4-V PCML is supported.

### Future Support

The Stratix IV GX device will allow 1.5 V in addition to the 1.4 V option. The ALTGX MegaWizard Plug-In Manager (**TX Analog** screen) will support 1.5 V. Note that all transceiver channels within a transceiver block must have the same  $V_{CCH}$  setting. For a  $V_{CCH}$  setting of 1.5 V, the transceiver channels can run from 600 Mbps to 4.25 Gbps data rate. In

In addition to 1.4-V PCML I/O standard, the 1.5-V PCML I/O standard will be supported. This additional option of 1.5 V is intended for sharing power supplies (simplification of power distribution network on the board) to Stratix IV devices.

### Configuring Clock Multiplier Unit (CMU) Channels as Additional Transceiver Channels

#### Current Support

Each Stratix IV GX transceiver block consists of four regular transceiver channels that can run from 600 Mbps to 6.375 Gbps, and two CMU channels: CMU0 channel and CMU1 channel. The CMU channels provide the high-speed serial and low-speed parallel clocks (in bonded functional modes) to the regular transceiver channels.

#### Future Support

The Stratix IV GX device will allow the CMU channels to be configured as additional transceiver channels providing a total of six transceiver channels within a transceiver block. The Quartus II software will allow you to configure each CMU channel as an additional transceiver channel.

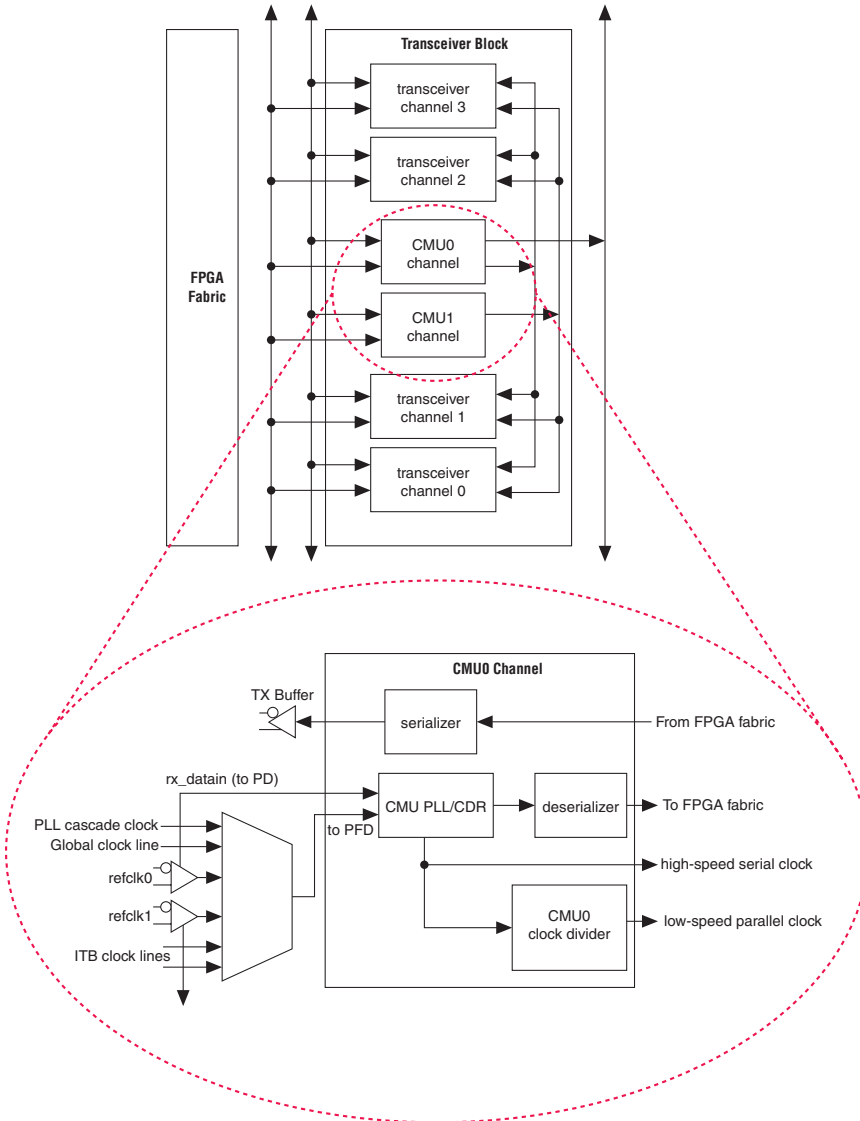
Each CMU channel comprises of a transmitter buffer, CMU phase-locked loop (PLL), serializer, and deserializer. When the CMU channels are configured as transceiver channels, the `refclk` pins in the transceiver block receive the serial input data. The CMU PLL will get configured as a clock and data recovery unit (CDR). The CMU channels also have parts per million (PPM) detection capability to detect the PPM difference between the recovered clock and the local reference clock.

The following features are available when the CMU channels are configured as transceiver channels:

- The CMU0 and CMU1 channels will run from 600 Mbps to 3.2 Gbps serial data rates. The data rate range above 3.2 Gbps will be determined after characterization.
- The CMU channels have PMA functionality only. (No physical coding sublayer [PCS] hard macro blocks).
- The PCI Express (PIPE) rateswitch circuitry is not available.

Figure 1 shows how to configure the CMU channels as additional transceiver channels.

**Figure 1. Configuring the CMU Channels as Additional Transceiver Channels**



## **PMA Direct Mode**

### **Future Support**

The Stratix IV GX device will provide a physical medium attachment (PMA) direct mode in which all the PCS blocks including the phase compensation FIFOs will be bypassed. All the signals from the PMA block in the transceiver channel will drive directly into the FPGA fabric. Similarly, the data and control signals from the FPGA fabric will be directly provided to the PMA blocks, bypassing the PCS blocks. In PMA direct mode, the transceiver channels will operate from 600 Mbps to 3.2 Gbps. The data rate range above 3.2 Gbps will be determined after characterization.

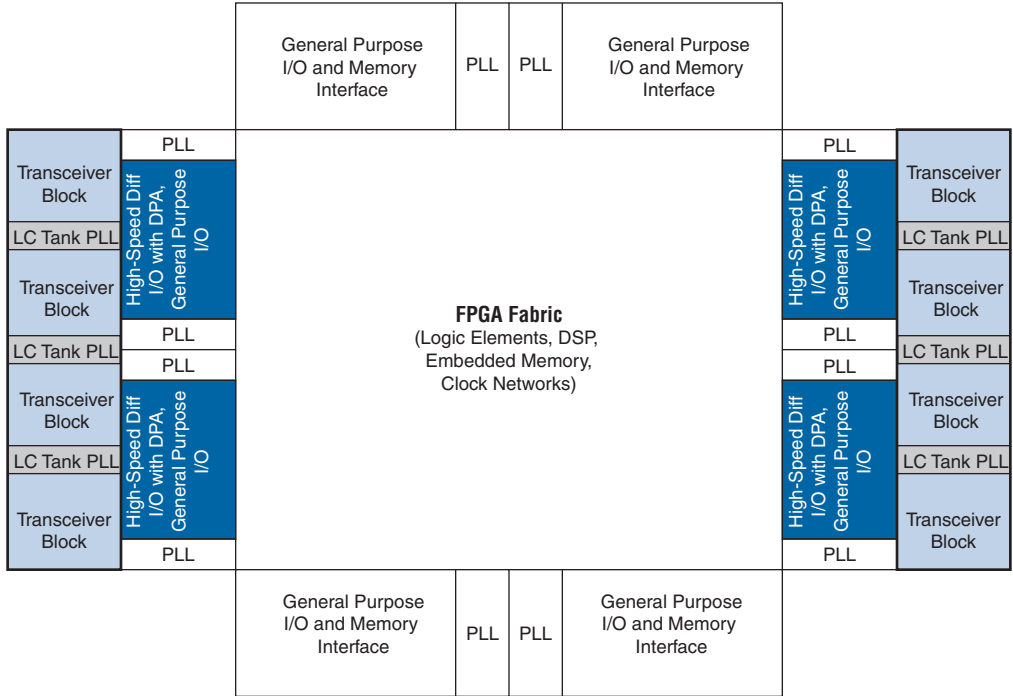
## **LC Tank PLL Support**

### **Future Support**

The Stratix IV GX contains LC tank PLLs located between the transceiver blocks. The LC tank PLL will support data rates ranging from 5 Gbps to 6.375 Gbps and will provide improved transceiver performance at these data rates. When using the LC tank PLL, the transceiver analog power (VCCA\_L/R) must be set to 3.0 V on the same side of the device. The jitter specifications of the transceiver when using the LC tank PLL will be available after characterization. The Quartus II software will implement additional channel placement constraints when the LC tank PLL is enabled.

Figure 2 shows a Stratix IV GX device variant with the maximum number of transceiver blocks.

**Figure 2. LC Tank PLL Support in Stratix IV GX Devices**



## 8.5 Gbps Support

### Future Support

The ALTGX MegaWizard Plug-In Manager will allow you to configure regular transceiver channels in -2 commercial speed grade Stratix IV GX devices to run up to 8.5 Gbps.

## Multichannel Bonding

### Current Support

The Quartus II software allows the following bonded configurations:

- ×4 bonded configuration in basic single-width without rate matcher, XAUI, and PCI Express (PIPE) functional modes. The PCS and PMA functional blocks are bonded in these modes.
- ×4 bonded configuration in (OIF) CEI PHY interface functional mode. The PMA functional blocks are bonded in this mode.
- ×8 bonded configuration in PCI Express (PIPE) ×8 functional mode only.

### *Bonding of PCS and PMA Functional Blocks*

### Future Support

Basic single- and double-width functional modes will be enhanced to support bonding of PCS and PMA functional blocks across eight transceiver channels. Bonding of PCS and PMA functional blocks in more than eight transceiver channels will be determined after characterization.

### *Bonding of PMA Functional Blocks*

### Future Support

Basic single- and double-width functional modes will be enhanced after characterization to support bonding of PMA functional blocks across all transceiver channels on the same side of the device.

### *Flexible Master/Slave Configuration*

### Current Support

The Quartus II software requires the lower transceiver block to be the master for PCI Express (PIPE) ×8 configuration. The master transceiver block provides all the shared control signals and clocks to the adjacent transceiver block. The current Quartus II software requires the physical channel0 in the master transceiver block to be assigned as the logical channel0 of a ×8 link.

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### **Future Support**

Based on characterization, the Quartus II software will allow:

- Any of the two transceiver blocks of a  $\times 8$  link to be configured as the master transceiver block
- Any channel within a  $\times 8$  bonded configuration to be assigned as logical channel0

### **Dynamic Reconfiguration**

#### **Future Support**

Stratix IV GX devices will provide the option to dynamically reconfigure the PMA settings, functional blocks, CMU PLLs, RX CDRs, and input reference clock selection of a transceiver channel without affecting any other transceiver channels or the core logic in the device. This feature will enable you to dynamically switch a transceiver channel between multiple protocols and data rates and adjust the transceiver PMA settings to adapt to multiple high-speed interconnect systems.

The ALTGX MegaWizard Plug-In Manager will provide dynamic reconfiguration options on additional screens. A new MegaWizard Plug-In Manager interface will be available to instantiate a hardware controller (dynamic reconfiguration controller) that will initiate and control the dynamic reconfiguration process without user intervention. The PMA settings that can be dynamically changed will be the  $V_{OD}$  (output differential voltage), preemphasis, equalization, and DC gain. The dynamic reconfiguration controller will also control the adaptive equalization (AEQ) hardware and the CDR and receiver buffer offset cancellation circuitry.

### **Adaptive Equalization**

#### **Future Support**

The adaptive equalization feature will enable the Stratix IV GX transceiver to adapt to changing data rates and backplane characteristics by dynamically tuning the equalization setting of the receiver without user intervention.

## CDR and Receiver Input Buffer Offset Cancellation

### Future Support

Stratix IV GX device will provide an offset cancellation circuit per transceiver channel to counter the offset variations due to process, voltage, and temperature. The Quartus II software will allow you to enable this circuit and control it through the dynamic reconfiguration controller.

## Analog Controls

### Current Support

The analog controls (pre-emphasis, static equalization, and bandwidth settings) are enabled in the ALTGX MegaWizard Plug-In Manager (TX Analog screen) but not functional.

### Future Support

The rules for pre-emphasis will be implemented. Bandwidth settings for protocol functional modes will be set based on characterization.

## Configuring Unused CMU PLLs as General Purpose PLLs

### Future Support

The Stratix IV GX transceiver will allow configuring of an unused CMU PLL in a transceiver block as a general purpose PLL to provide clocks to the FPGA fabric. This will help to effectively utilize PLL resources in the device.

## Decision Feedback Equalization

### Future Support

High-speed signals transmitted across a backplane will experience signal attenuation due to skin effect, dielectric losses, and crosstalk. The Stratix IV GX device will provide a multi-tap decision feedback equalization (DFE) to primarily compensate the backplane attenuation due to crosstalk. DFE cancels out post cursor inter-symbol interference. You can use DFE can be used in conjunction with pre-emphasis, linear equalization (Manual Equalization), and AEQ.

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## Low Uncertainty Latency Option

### Future Support

This option will be enabled to reduce the uncertainty in PMA and PCS data paths.

When this option is enabled, the phase compensation FIFOs are configured in registered mode (one stage register), transmit bitslipper, and a feedback path for the CMU PLL are enabled. This option is typically used in systems implementing protocols like CPRI.

## Electrical Idle in Basic Functional Mode

### Current Support

In Stratix IV GX devices, the Quartus II software supports forcing the transmitter buffer into electrical idle in PCI Express (PIPE) functional mode.

### Future Support

In addition to the current support, the Quartus II software will support forcing the transmitter buffer into electrical idle in Basic functional modes.

## Signal Detect Capability in Basic Functional Mode

### Current Support

In Stratix IV GX devices, signal detect capability is supported by the Quartus II software in PCI Express (PIPE) functional mode only.

### Future Support

In addition to the current support, the Quartus II software will support signal detect capability in Basic functional modes.

## Reducing the Minimum Input Clock Frequency to 27 MHz

### Current Support

The current Quartus II software allows the transceiver input reference clock frequency range from 50 MHz to 637.5 MHz.

### Future Support

In a future software version, the minimum clock frequency limit will be extended down to 27 MHz to support SDI applications. This feature is applicable only to 780 packages.

## GIGE Functional Mode Enhancement

### Current Support

The GIGE functional mode operates at a data rate of 1.25 Gbps.

### Future Support

In addition to the allowed data rate of 1.25 Gbps, the Quartus II software will enhance the GIGE functional mode to support a line rate of 2.5 Gbps.

## HyperTransport Support in Transceivers

### Future Support

The Quartus II software will provide HyperTransport 3.0 support at data rates between 600 Mbps to 3.2 Gbps (Gen1 and Gen3 data rates). The data rates less than 600 Mbps will be supported through oversampling. The transceiver will be configured in bonded channel configuration with PMA direct mode enabled. Support for AC coupling for HyperTransport functional mode will be determined after characterization.

## PCI Express Hard-IP Support

### Current Support

Stratix IV GX devices provide support for PCI Express endpoint modes in Gen1  $\times 1$ ,  $\times 4$ ,  $\times 8$  configurations and Gen2  $\times 1$ ,  $\times 4$  configurations.

### Future Support

In addition to the above, Stratix IV GX devices will support the following modes:

- Endpoint modes in Gen2  $\times 8$  configurations
- Rootport modes in Gen1  $\times 1$ ,  $\times 4$ ,  $\times 8$  and Gen2  $\times 1$ ,  $\times 4$ ,  $\times 8$  configurations
- Runtime switching between endpoint and rootport modes
- Runtime reconfiguration of PCI read only registers

## On-Chip Scope (OCS)

### Future Support

The on-chip scope (OCS) estimates the eye opening of the signal inside the chip at the input of the CDR on the receive side. It provides a way to assess the effectiveness of the receiver equalizer, thereby enabling system engineers to analyze and debug the signal integrity of a transmission link inside the chip.

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## **LVDS Operation Up to 1.6 Gbps**

### **Current Support**

Stratix IV GX devices allow LVDS operation at data rates from 150 Mbps to 1.25 Gbps.

### **Future Support**

Stratix IV GX devices with -2 commercial speed grades will allow LVDS operation up to 1.6 Gbps data rate.

## **DDR3 SDRAM Memory Interface Support**

### **Current Support**

Quartus II design software supports compilation and functional simulation for DDR3 SDRAM interfaces up to 1,067 Mbps/533 MHz. Timing closure is supported for DDR3 interfaces up to 800 Mbps/400 MHz.

### **Future Support**

Timing closure and hardware calibration support for all Stratix IV DDR3 SDRAM interfaces (including 1,067 Mbps/533 MHz DDR3 on -2 commercial speed grade devices).