

This chapter covers the electrical and switching characteristics for Stratix® V devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

 For information regarding the densities and packages of devices in the Stratix V family, refer to the *Stratix V Device Family Overview* chapter.

### Electrical Characteristics

The following sections describe the electrical characteristics of Stratix V devices.

#### Operating Conditions

When you use Stratix V devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix V devices, you must consider the operating requirements described in this chapter.

Stratix V devices are offered in commercial and industrial grades. Commercial devices are offered in -1 (fastest), -2, -3, and -4 speed grades. Industrial devices are offered in -3 and -4 speed grades.

#### Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in [Table 2-1](#) may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 2-1. Absolute Maximum Ratings for Stratix V Devices—Preliminary (Part 1 of 2)**

Symbol	Description	Minimum	Maximum	Unit
$V_{CC}$	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
$V_{CCPT}$	Power supply for programmable power technology	-0.5	1.8	V
$V_{CCPGM}$	Power supply for configuration pins	-0.5	3.75	V
$V_{CC\_AUX}$	Auxiliary supply for the programmable power technology	-0.5	3.75	V

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**Table 2-1. Absolute Maximum Ratings for Stratix V Devices—Preliminary (Part 2 of 2)**

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.75	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V
V <sub>CCD_FPLL</sub>	PLL digital power supply	-0.5	3.75	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	-0.5	3.75	V
V <sub>I</sub>	DC input voltage	-0.5	4.0	V
I <sub>OUT</sub>	DC output current per pin	-25	40	mA
T <sub>J</sub>	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C

Table 2-2 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

**Table 2-2. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices**

Symbol	Description	Devices	Minimum	Maximum	Unit
V <sub>CCA_GXBL</sub>	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSL_L</sub>	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCHSSL_R</sub>	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBL</sub>	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCT_GXBL</sub>	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GXBR</sub>	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V <sub>CCT_GTBR</sub>	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V <sub>CCL_GTBR</sub>	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 2-3 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 2-3 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~5% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to half a year.

**Table 2-3. Maximum Allowed Overshoot During Transitions—Preliminary**

Symbol	Description	Condition (V)	Overshoot Duration as % @ T <sub>J</sub> = 100°C	Unit
V <sub>i</sub> (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 2-4 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 2-4. Recommended Operating Conditions for Stratix V Devices—Preliminary**

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
$V_{CC}$	Core voltage and periphery circuitry power supply	—	0.82	0.85	0.88	V
$V_{CCPT}$	Power supply for programmable power technology	—	1.45	1.50	1.55	V
$V_{CC\_AUX}$	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
$V_{CCPD}$ <sup>(1)</sup>	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
$V_{CCIO}$	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
$V_{CCPGM}$	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
$V_{CCA\_FPLL}$	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
$V_{CCD\_FPLL}$	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
$V_{CCBAT}$ <sup>(2)</sup>	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
$V_I$	DC input voltage	—	-0.5	—	3.6	V
$V_O$	Output voltage	—	0	—	$V_{CCIO}$	V
$T_J$	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	-40	—	100	°C
$t_{RAMP}$	Power supply ramp time	Standard POR	200 $\mu$ s	—	100 ms	—
		Fast POR	200 $\mu$ s	—	4 ms	—

**Notes to Table 2-4:**

- $V_{CCPD}$  must be 2.5 V when  $V_{CCIO}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCIO}$  is 3.0 V.
- If you do not use the design security feature in Stratix V devices, connect  $V_{CCBAT}$  to a 2.5- or 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors  $V_{CCBAT}$ . Stratix V devices will not exit POR if  $V_{CCBAT}$  stays at logic low.

Table 2-5 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 2-5. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices**

Symbol	Description	Devices	Minimum	Typical	Maximum	Unit
$V_{CCA\_GXBL}$ <sup>(1)</sup>	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85, 2.375	3.0, 2.5	3.15, 2.625	V
$V_{CCA\_GXBR}$ <sup>(1)</sup>	Transceiver channel PLL power supply (right side)	GX, GS	2.85, 2.375	3.0, 2.5	3.15, 2.625	V
$V_{CCA\_GTBR}$	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
$V_{CCHIP\_L}$	Transceiver hard IP power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
$V_{CCHIP\_R}$	Transceiver hard IP power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
$V_{CCHSSI\_L}$	Transceiver PCS power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
$V_{CCHSSI\_R}$	Transceiver PCS power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
$V_{CCR\_GXBL}$ <sup>(2)</sup>	Receiver analog power supply (left side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
$V_{CCR\_GXBR}$ <sup>(2)</sup>	Receiver analog power supply (right side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
$V_{CCR\_GTBR}$	Receiver analog power supply for GT channels (right side)	GT	0.95	1.0	1.05	V
$V_{CCT\_GXBL}$ <sup>(2)</sup>	Transmitter analog power supply (left side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
$V_{CCT\_GXBR}$ <sup>(2)</sup>	Transmitter analog power supply (right side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
$V_{CCT\_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	0.95	1.0	1.05	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	0.95	1.0	1.05	V
$V_{CCH\_GXBL}$	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
$V_{CCH\_GXBR}$	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

**Notes to Table 2-5:**


- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 1.0 V or 0.85 V.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

 For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**I/O Pin Leakage Current**

Table 2-6 lists the Stratix V I/O pin leakage current specifications.

**Table 2-6. I/O Pin Leakage Current for Stratix V Devices—Preliminary**

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_I$	Input pin	$V_I = 0\text{ V to }V_{CCIO\text{MAX}}$	-30	—	30	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO\text{MAX}}$	-30	—	30	$\mu\text{A}$

**Bus Hold Specifications**

Table 2-7 lists the Stratix V device family bus hold specifications.

**Table 2-7. Bus Hold Parameters for Stratix V Devices—Preliminary**

Parameter	Symbol	Conditions	$V_{CCIO}$										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$I_{SUSL}$	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	$\mu\text{A}$
High sustaining current	$I_{SUSH}$	$V_{IN} < V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	$\mu\text{A}$
Low overdrive current	$I_{ODL}$	$0\text{ V} < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	$\mu\text{A}$
High overdrive current	$I_{ODH}$	$0\text{ V} < V_{IN} < V_{CCIO}$	—	-120	—	-160	—	-200	—	-300	—	-500	$\mu\text{A}$
Bus-hold trip point	$V_{TRIP}$	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

**On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 2-8 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 2-8. OCT Calibration Accuracy Specifications for Stratix V Devices—Preliminary <sup>(1)</sup> (Part 1 of 2)**

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
25- $\Omega$ $R_S$	Internal series termination with calibration (25- $\Omega$ setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2\text{ V}$	$\pm 15$	$\pm 15$	$\pm 15$	%
50- $\Omega$ $R_S$	Internal series termination with calibration (50- $\Omega$ setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2\text{ V}$	$\pm 15$	$\pm 15$	$\pm 15$	%

**Table 2-8. OCT Calibration Accuracy Specifications for Stratix V Devices—Preliminary <sup>(1)</sup> (Part 2 of 2)**

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
34-Ω and 40-Ω R <sub>S</sub>	Internal series termination with calibration (34-Ω and 40-Ω setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R <sub>S</sub>	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±15	±15	±15	%
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCIO</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	%
25-Ω R <sub>S_left_shift</sub>	Internal left shift series termination with calibration (25-Ω R <sub>S_left_shift</sub> setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	%

**Note to Table 2-8:**

(1) OCT calibration accuracy is valid at the time of calibration only.

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change. Table 2-9 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

**Table 2-9. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices—Preliminary (1)**

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3, I3	C4, I4	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 3.0 and 2.5 V	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±35	±50	±50	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 3.0 and 2.5 V	±30	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±30	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±35	±50	±50	%
100-Ω R <sub>D</sub>	Internal differential termination (100-Ω setting)	V <sub>CCIO</sub> = 2.5 V	±25	±25	±25	%

**Note to Table 2-9:**

(1) Pending silicon characterization.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 2-10 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 2-10 to determine the OCT variation after power-up calibration and Equation 2-1 to determine the OCT variation without re-calibration.

**Equation 2-1. OCT Variation Without Re-Calibration for Stratix V Devices—Preliminary (1), (2), (3), (4), (5), (6)**

$$R_{OCT} = R_{SCAL} \left( 1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

**Notes to Equation 2-1:**

- (1) The  $R_{OCT}$  value calculated from Equation 2-1 shows the range of OCT resistance with the variation of temperature and  $V_{CCIO}$ .
- (2)  $R_{SCAL}$  is the OCT resistance value at power-up.
- (3)  $\Delta T$  is the variation of temperature with respect to the temperature at power-up.
- (4)  $\Delta V$  is the variation of voltage with respect to the  $V_{CCIO}$  at power-up.
- (5)  $dR/dT$  is the percentage change of  $R_{SCAL}$  with temperature.
- (6)  $dR/dV$  is the percentage change of  $R_{SCAL}$  with voltage.

Table 2-10 lists the on-chip termination variation after power-up calibration.

**Table 2-10. OCT Variation after Power-Up Calibration for Stratix V Devices—Preliminary (1), (2)**

Symbol	Description	$V_{CCIO}$ (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/ $^{\circ}$ C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

**Notes to Table 2-10:**

- (1) Valid for a  $V_{CCIO}$  range of  $\pm 5\%$  and a temperature range of  $0^{\circ}$  to  $85^{\circ}$ C.
- (2) Pending silicon characterization.

## Pin Capacitance

Table 2-11 lists the Stratix V device family pin capacitance.

**Table 2-11. Pin Capacitance for Stratix V Devices—Preliminary**

Symbol	Description	Value	Unit
$C_{IOTB}$	Input capacitance on the top and bottom I/O pins	5.5	pF
$C_{IOLR}$	Input capacitance on the left and right I/O pins	5.5	pF
$C_{OUTFB}$	Input capacitance on dual-purpose clock output and feedback pins	5.5	pF

## Hot Socketing

Table 2-12 lists the hot socketing specifications for Stratix V devices.

**Table 2-12. Hot Socketing Specifications for Stratix V Devices—Preliminary**

Symbol	Description	Maximum
$I_{IOPIN} (DC)$	DC current per I/O pin	300 $\mu$ A
$I_{IOPIN} (AC)$	AC current per I/O pin	8 mA <sup>(1)</sup>
$I_{XCVR-TX} (DC)$ <sup>(2)</sup>	DC current per transceiver transmitter pin	100 mA
$I_{XCVR-RX} (DC)$ <sup>(2)</sup>	DC current per transceiver receiver pin	50 mA

**Notes to Table 2-12:**

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{IOPIN}| = C dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.
- (2) These specifications are preliminary.

## Internal Weak Pull-Up Resistor

Table 2-13 lists the weak pull-up resistor values for Stratix V devices.

**Table 2-13. Internal Weak Pull-Up Resistor for Stratix V Devices—Preliminary** <sup>(1), (2)</sup>

Symbol	Description	$V_{CCIO}$ Conditions (V) <sup>(3)</sup>	Value <sup>(4)</sup>	Unit
$R_{PU}$	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 $\pm$ 5%	25	k $\Omega$
		2.5 $\pm$ 5%	25	k $\Omega$
		1.8 $\pm$ 5%	25	k $\Omega$
		1.5 $\pm$ 5%	25	k $\Omega$
		1.35 $\pm$ 5%	25	k $\Omega$
		1.25 $\pm$ 5%	25	k $\Omega$
		1.2 $\pm$ 5%	25	k $\Omega$

**Notes to Table 2-13:**

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG  $\overline{TCX}$  pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (4) These specifications are valid with a  $\pm$ 10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 2-14 through Table 2-19 list the input voltage ( $V_{IH}$  and  $V_{IL}$ ), output voltage ( $V_{OH}$  and  $V_{OL}$ ), and current drive characteristics ( $I_{OH}$  and  $I_{OL}$ ) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The  $V_{OL}$  and  $V_{OH}$  values are valid at the corresponding  $I_{OH}$  and  $I_{OL}$ , respectively.

For an explanation of the terms used in Table 2-14 through Table 2-19, refer to “Glossary” on page 2-35.

**Table 2-14. Single-Ended I/O Standards for Stratix V Devices—Preliminary**

I/O Standard	$V_{CCIO}$ (V)			$V_{IL}$ (V)		$V_{IH}$ (V)		$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{OL}$ (mA)	$I_{OH}$ (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVC MOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * $V_{CCIO}$	0.65 * $V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * $V_{CCIO}$	0.65 * $V_{CCIO}$	$V_{CCIO} + 0.3$	0.25 * $V_{CCIO}$	0.75 * $V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * $V_{CCIO}$	0.65 * $V_{CCIO}$	$V_{CCIO} + 0.3$	0.25 * $V_{CCIO}$	0.75 * $V_{CCIO}$	2	-2

**Table 2-15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices—Preliminary (Part 1 of 2)**

I/O Standard	$V_{CCIO}$ (V)			$V_{REF}$ (V)			$V_{TT}$ (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$	0.49 * $V_{CCIO}$	0.5 * $V_{CCIO}$	0.51 * $V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—

**Table 2-15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices—Preliminary (Part 2 of 2)**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)			V <sub>TT</sub> (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.53 * V <sub>CCIO</sub>	—	V <sub>CCIO</sub> /2	—
HSUL-12	1.14	1.2	1.3	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	—	—	—

**Table 2-16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices—Preliminary (Part 1 of 2)**

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(DC)</sub> (V)		V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>ol</sub> (mA)	I <sub>oh</sub> (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.3	V <sub>REF</sub> - 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> - 0.608	V <sub>TT</sub> + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.3	V <sub>REF</sub> - 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> - 0.81	V <sub>TT</sub> + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCIO</sub> + 0.3	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	V <sub>TT</sub> - 0.603	V <sub>TT</sub> + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCIO</sub> + 0.3	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	0.28	V <sub>CCIO</sub> - 0.28	13.4	-13.4
SSTL-15 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCIO</sub>	0.8 * V <sub>CCIO</sub>	8	-8
SSTL-15 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCIO</sub>	0.8 * V <sub>CCIO</sub>	16	-16
SSTL-135 Class I, II	—	V <sub>REF</sub> - 0.09	V <sub>REF</sub> + 0.09	—	V <sub>REF</sub> - 0.16	V <sub>REF</sub> + 0.16	TBD (†)	TBD (†)	TBD (†)	TBD (†)
SSTL-125 Class I, II	—	V <sub>REF</sub> - 0.85	V <sub>REF</sub> + 0.85	—	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	TBD (†)	TBD (†)	TBD (†)	TBD (†)
SSTL-12 Class I, II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	TBD (†)	TBD (†)	TBD (†)	TBD (†)
HSTL-18 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-18 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-15 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-15 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCIO</sub>	0.75* V <sub>CCIO</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCIO</sub>	0.75* V <sub>CCIO</sub>	16	-16

**Table 2-16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices—Preliminary (Part 2 of 2)**

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{ol}$ (mA)	$I_{oh}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1^* V_{CCIO}$	$0.9^* V_{CCIO}$	TBD (1)	TBD (1)

Note to Table 2-16:

(1) Pending silicon characterization.

**Table 2-17. Differential SSTL I/O Standards for Stratix V Devices—Preliminary**

I/O Standard	$V_{CCIO}$ (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—	—	$V_{CCIO}/2$	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	—	$V_{REF} - 0.135$	$V_{CCIO}/2$	$V_{REF} + 0.135$	TBD (1)	TBD (1)	$V_{REF} - 0.15$	—	$V_{REF} + 0.15$
SSTL-125 Class I, II	1.19	1.25	1.31	TBD (1)	—	TBD (1)	$V_{CCIO}/2$	TBD (1)	TBD (1)	—	TBD (1)	TBD (1)	TBD (1)
SSTL-12 Class I, II	1.14	1.2	1.26	TBD (1)	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30	TBD (1)	TBD (1)	TBD (1)

Note to Table 2-17:

(1) Pending silicon characterization.

**Table 2-18. Differential HSTL and HSUL I/O Standards for Stratix V Devices—Preliminary**

I/O Standard	$V_{CCIO}$ (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5^* V_{CCIO}$	—	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5^* V_{CCIO} - 0.12$	$0.5^* V_{CCIO}$	$0.5^* V_{CCIO} + 0.12$	$0.4^* V_{CCIO}$	$0.5^* V_{CCIO}$	$0.6^* V_{CCIO}$	0.44	0.44

**Table 2-19. Differential I/O Standard Specifications for Stratix V Devices—Preliminary <sup>(1)</sup>**

I/O Standard	V <sub>CCIO</sub> (V) <sup>(7)</sup>			V <sub>ID</sub> (mV)			V <sub>ICM(DC)</sub> (V)			V <sub>OD</sub> (V) <sup>(2)</sup>			V <sub>OCM</sub> (V) <sup>(2)</sup>		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to <a href="#">Table 2-20 on page 2-15</a> .														
2.5 V LVDS	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V <sup>(5)</sup>	—	0.05	D <sub>MAX</sub> ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
							1.05	D <sub>MAX</sub> > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS <sup>(3)</sup>	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V <sup>(5)</sup>	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL <sup>(6)</sup>	2.375	2.5	2.625	300	—	—	0.6	D <sub>MAX</sub> ≤ 700 Mbps	1.8 <sup>(4)</sup>	—	—	—	—	—	—
							1	D <sub>MAX</sub> > 700 Mbps	1.6 <sup>(4)</sup>	—	—	—	—	—	—

**Notes to Table 2-19:**

- (1) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in “[Transceiver Performance Specifications](#)” on page 2-15.
- (2) RL range: 90 ≤ RL ≤ 110 Ω.
- (3) There are no fixed V<sub>ICM</sub>, V<sub>OD</sub>, and V<sub>OCM</sub> specifications for BLVDS. They depend on the system topology.
- (4) For D<sub>MAX</sub> > 700 Mbps, the minimum input voltage is 0.85 V; the maximum input voltage is 1.75 V. For F<sub>MAX</sub> ≤ 700 Mbps, the minimum input voltage is 0.45 V; the maximum input voltage is 1.95 V.
- (5) The minimum VID value is applicable over the entire common mode range, VCM.
- (6) LVPECL is only supported on dedicated clock input pins.
- (7) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.



You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.



For more information about power estimation tools, refer to the [PowerPlay Early Power Estimator User Guide](#) and the [PowerPlay Power Analysis](#) chapter in the [Quartus II Handbook](#).

## Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 2–20 lists the Stratix V GX and GS transceiver specifications.

**Table 2–20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary <sup>(1)</sup> (Part 1 of 4)**

Symbol/ Description	Conditions	–1 Commercial Speed Grade			–2 Commercial/Industrial Speed Grade			–3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>Reference Clock</b>											
Supported I/O Standards	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL										
Input frequency from REFCLK input pins	—	40	—	710	40	—	710	40	—	710	MHz
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V <sub>ICM</sub> (AC coupled)	—	1000/850 <sup>(2)</sup>			1000/850 <sup>(2)</sup>			1000/850 <sup>(2)</sup>			mV
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV

**Table 2-20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary <sup>(1)</sup> (Part 2 of 4)**

Symbol/ Description	Conditions	-1 Commercial Speed Grade			-2 Commercial/Industrial Speed Grade			-3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥1 MHz	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms)	10 KHz to 20 MHz	—	—	3	—	—	3	—	—	3	ps
R <sub>REF</sub>	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω
<b>Transceiver Clocks</b>											
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Avalon-MM PHY management clock (phy_mgmt_clk) frequency	< 150										MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	100	—	125	MHz
<b>Receiver</b>											
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS										
Data rate (Standard PCS) <sup>(7)</sup>	—	600	—	8500	600	—	8500	600	—	6500	Mbps
Data rate (10G PCS) <sup>(7)</sup>	—	600	—	14100	600	—	12500	600	—	8500	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) after device configuration	V <sub>CCR_GXB</sub> = 1.0 V	—	—	1.8	—	—	0.8	—	—	1.8	V
	V <sub>CCR_GXB</sub> = 0.85 V	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(4)</sup>	—	85	—	—	85	—	—	85	—	—	mV

**Table 2-20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary <sup>(1)</sup> (Part 3 of 4)**

Symbol/ Description	Conditions	-1 Commercial Speed Grade			-2 Commercial/Industrial Speed Grade			-3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors	85-Ω setting	85			85			85			Ω
	100-Ω setting	100			100			100			Ω
	120-Ω setting	120			120			120			Ω
	150-Ω setting	150			150			150			Ω
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz)	—	—	16	—	—	16	—	—	16	dB
	Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	2	—	—	2	—	—	2	—	dB
	DC Gain Setting = 2	—	4	—	—	4	—	—	4	—	dB
	DC Gain Setting = 3	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 4	—	8	—	—	8	—	—	8	—	dB
<b>Transmitter</b>											
Supported I/O Standards	1.4-V and 1.5-V PCML										
Data rate (Standard PCS)	—	600	—	8500	600	—	8500	600	—	6500	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500	Mbps
V <sub>OCM</sub>	0.65-V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	85			85			85			Ω
	100-Ω setting	100			100			100			Ω
	120-Ω setting	120			120			120			Ω
	150-Ω setting	150			150			150			Ω
Rise time <sup>(5)</sup>	—	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(5)</sup>	—	30	—	160	30	—	160	30	—	160	ps
<b>CMU PLL</b>											
Supported Data Range	—	600	—	14100	600	—	12500	600	—	8500	Mbps
<b>ATX PLL</b>											


**Table 2-20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary <sup>(1)</sup> (Part 4 of 4)**

Symbol/ Description	Conditions	-1 Commercial Speed Grade			-2 Commercial/Industrial Speed Grade			-3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported Data Range	VCO post-divider L=1	8000	—	14100	8000	—	12500	8000	—	8500	Mbps
	L=2	4000	—	7050	4000	—	7050	4000	—	7050	Mbps
	L=4	2000	—	3525	2000	—	3525	2000	—	3525	Mbps
	L=8	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
Input Reference Clock Frequency <sup>(6)</sup>	—	100	—	710	100	—	710	100	—	710	MHz
<b>Transceiver-FPGA Fabric Interface</b>											
Interface speed	—	25	—	283	25	—	266	25	—	250	MHz

**Notes to Table 2-20:**

- (1) Speed grades shown in Table 2-20 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Family Overview* chapter.
- (2) The reference clock common mode voltage is equal to the  $V_{CCR\_GXB}$  power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (6) The input reference clock frequency options depend on the data rate and the device speed grade.
- (7) The line datarate may be limited by PCS-FPGA interface speed grade.

Table 2-21 lists the Stratix V GT transceivers specifications.

 Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 2-21 are the same as those listed in Table 2-20.

**Table 2-21. Transceiver Specifications for Stratix V GT Devices—Preliminary (Part 1 of 2)**

Symbol/ Description	Conditions	-2 Commercial/Industrial Speed Grade			-3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>Reference Clock</b>								
$V_{ICM}$ (AC coupled)	—	1000			1000			mV
<b>Receiver</b>								
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Programmable equalization (AC Gain)	GT channels	—	15	—	—	15	—	dB

**Table 2-21. Transceiver Specifications for Stratix V GT Devices—Preliminary (Part 2 of 2)**

Symbol/ Description	Conditions	-2 Commercial/Industrial Speed Grade			-3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	$\Omega$
<b>Transmitter</b>								
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	$\Omega$
Rise/Fall time	GT channels	—	15	—	—	15	—	ps

Table 2-22 shows the  $V_{OD}$  settings for the GX channel.

**Table 2-22. Typical  $V_{OD}$  Setting for GX Channel, TX Termination = 100  $\Omega$ —Preliminary**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
<b><math>V_{OD}</math> differential peak to peak typical</b>	0	0	32	640
	1	20	33	660
	2	40	34	680
	3	60	35	700
	4	80	36	720
	5	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 2–23 shows the  $V_{OD}$  settings for the GT channel.

**Table 2–23. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$ —Preliminary**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
$V_{OD}$ differential peak to peak typical	0	0
	1	200
	2	400
	3	600
	4	800
	5	1000

## Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### Clock Tree Specifications

Table 2–24 lists the clock tree specifications for Stratix V devices.

**Table 2–24. Clock Tree Performance for Stratix V Devices—Preliminary <sup>(1)</sup>**

Symbol	Performance			Unit
	–2 Speed Grade	–3 Speed Grade	–4 Speed Grade	
Global and Regional Clock	717	700	500	MHz
Periphery Clock	550	500	500	MHz

**Note to Table 2–24:**

(1) The Stratix V ES devices are limited for the 600 MHz core clock network frequency.

### PLL Specifications

Table 2–25 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 2–25. PLL Specifications for Stratix V Devices—Preliminary <sup>(1)</sup> (Part 1 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}$	Input clock frequency (–2 speed grade)	5	—	800 <sup>(2)</sup>	MHz
	Input clock frequency (–3 speed grade)	5	—	700 <sup>(2)</sup>	MHz
	Input clock frequency (–4 speed grade)	5	—	650 <sup>(2)</sup>	MHz
$f_{INPFD}$	Input frequency to the PFD	5	—	325	MHz
$f_{FINPFD}$	Fractional Input clock frequency to the PFD	50	—	133	MHz
$f_{VCO}$	PLL VCO operating range (–2 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–3 speed grade)	600	—	1400	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

**Table 2–25. PLL Specifications for Stratix V Devices—Preliminary <sup>(1)</sup> (Part 2 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{OUT}$	Output frequency for an internal global or regional clock (–2 speed grade)	—	—	717 <sup>(3)</sup>	MHz
	Output frequency for an internal global or regional clock (–3 speed grade)	—	—	700 <sup>(3)</sup>	MHz
	Output frequency for an internal global or regional clock (–4 speed grade)	—	—	500 <sup>(3)</sup>	MHz
$f_{OUT\_EXT}$	Output frequency for an external clock output (–2 speed grade)	—	—	800 <sup>(3)</sup>	MHz
	Output frequency for an external clock output (–3 speed grade)	—	—	667 <sup>(3)</sup>	MHz
	Output frequency for an external clock output (–4 speed grade)	—	—	533 <sup>(3)</sup>	MHz
$t_{OUTDUTY}$	Duty cycle for an external clock output (when set to 50%)	45	50	55	%
$t_{FCOMP}$	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	TBD <sup>(1)</sup>	—	—
$f_{DYCONFIGCLK}$	Dynamic Configuration Clock	—	—	100	MHz
$t_{LOCK}$	Time required to lock from the end-of-device configuration or deassertion of <i>areset</i>	—	—	1	ms
$t_{DLOCK}$	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CLBW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth <sup>(8)</sup>	—	4	—	MHz
$t_{PLL\_PSERR}$	Accuracy of PLL phase shift	—	—	±50	ps
$t_{ARESET}$	Minimum pulse width on the <i>areset</i> signal	10	—	—	ns
$t_{INCCJ}$ <sup>(4), (5)</sup>	Input clock cycle-to-cycle jitter ( $f_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ( $f_{REF} < 100$ MHz)	–750	—	+750	ps (p-p)
$t_{OUTPJ\_DC}$ <sup>(6)</sup>	Period Jitter for dedicated clock output ( $f_{OUT} \geq 100$ MHz)	—	—	TBD <sup>(1)</sup>	ps (p-p)
	Period Jitter for dedicated clock output ( $f_{OUT} < 100$ MHz)	—	—	TBD <sup>(1)</sup>	mUI (p-p)
$t_{OUTCCJ\_DC}$ <sup>(6)</sup>	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{OUT} \geq 100$ MHz)	—	—	TBD <sup>(1)</sup>	ps (p-p)
	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{OUT} < 100$ MHz)	—	—	TBD <sup>(1)</sup>	mUI (p-p)
$t_{OUTPJ\_IO}$ <sup>(6), (9)</sup>	Period Jitter for a clock output on a regular I/O ( $f_{OUT} \geq 100$ MHz)	—	—	TBD <sup>(1)</sup>	ps (p-p)
	Period Jitter for a clock output on a regular I/O ( $f_{OUT} < 100$ MHz)	—	—	TBD <sup>(1)</sup>	mUI (p-p)
$t_{OUTCCJ\_IO}$ <sup>(6), (9)</sup>	Cycle-to-Cycle Jitter for a clock output on a regular I/O ( $f_{OUT} \geq 100$ MHz)	—	—	TBD <sup>(1)</sup>	ps (p-p)
	Cycle-to-Cycle Jitter for a clock output on a regular I/O ( $f_{OUT} < 100$ MHz)	—	—	TBD <sup>(1)</sup>	mUI (p-p)

**Table 2-25. PLL Specifications for Stratix V Devices—Preliminary <sup>(1)</sup> (Part 3 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CASC\_OUTPJ\_DC}$ (6), (7)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \geq 100$ MHz)	—	—	TBD <sup>(1)</sup>	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} < 100$ MHz)	—	—	TBD <sup>(1)</sup>	mUI (p-p)
$f_{DRIFT}$	Frequency drift after PFDENA is disabled for a duration of 100 $\mu$ s	—	—	$\pm 10$	%
$dK_{BIT}$	Bit number of Delta Sigma Modulator (DSM)	—	24	—	Bits
$k_{VALUE}$	Numerator of Fraction	—	8388608	—	—
$f_{RES}$	Resolution of VCO frequency ( $f_{INPFD} = 100$ MHz)	—	5.96	—	Hz

**Notes to Table 2-25:**

- (1) Pending silicon characterization.
- (2) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (3) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (5)  $f_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (6) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 2-38 on page 2-33.
- (7) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$  MHz
  - b. Downstream PLL:  $\text{Downstream PLL BW} > 2$  MHz
- (8) High bandwidth PLL settings are not supported in external feedback mode.
- (9) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 2-36 on page 2-32.

## DSP Block Specifications

Table 2-26 lists the Stratix V DSP block performance specifications.

**Table 2-26. Block Performance Specifications for Stratix V DSP Devices—Preliminary <sup>(1)</sup> (Part 1 of 2)**

Mode	Performance				Unit
	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
<b>Modes using One DSP</b>					
Three $9 \times 9$	690	620	500	440	MHz
One $18 \times 18$	690	620	500	440	MHz
Two partial $18 \times 18$ (or $16 \times 16$ )	690	620	500	440	MHz
One $27 \times 27$	520	470	370	330	MHz
One $36 \times 18$	520	470	370	330	MHz
One sum of two $18 \times 18$ (One sum of two $16 \times 16$ )	570	520	410	360	MHz
One sum of square	520	470	370	330	MHz
One $18 \times 18$ plus $36(a \times b) + c$	570	520	410	360	MHz
<b>Modes using Two DSPs</b>					

**Table 2-26. Block Performance Specifications for Stratix V DSP Devices—Preliminary <sup>(1)</sup> (Part 2 of 2)**

Mode	Performance				Unit
	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
Three 18 × 18	570	520	410	360	MHz
One sum of four 18 × 18	490	440	350	310	MHz
One sum of two 27 × 27	490	440	350	310	MHz
One sum of two 36 × 18	490	440	350	310	MHz
One complex 18 × 18	570	520	410	360	MHz
One 36 × 36	460	410	330	290	MHz
<b>Modes using Three DSPs</b>					
One complex 18 × 25	400	360	290	250	MHz
<b>Modes using Four DSPs</b>					
One complex 27 × 27	490	440	350	310	MHz

**Note to Table 2-26:**

(1) These numbers are preliminary pending silicon characterization.

## Memory Block Specifications

Table 2-27 lists the Stratix V memory block specifications.

**Table 2-27. Memory Block Performance Specifications for Stratix V Devices—Preliminary <sup>(1), (2), (3)</sup> (Part 1 of 2)**

Memory	Mode	Resources Used		Performance						Unit
		ALUTs	Memory	C1 Speed Grade	C2 Speed Grade	C3 Speed Grade	I3 Speed Grade	C4 Speed Grade	I4 Speed Grade	
MLAB	Single port, all supported widths	0	1	—	600	500	500	450	450	MHz
	Simple dual-port, x32/x64 width	0	1	—	450	400	TBD	315	TBD	MHz
	Simple dual-port, x16 width	0	1	—	675	533	533	400	400	MHz
	ROM, all supported widths	0	1	—	600	500	500	450	450	MHz

**Table 2-27. Memory Block Performance Specifications for Stratix V Devices—Preliminary <sup>(1)</sup>, <sup>(2)</sup>, <sup>(3)</sup> (Part 2 of 2)**

Memory	Mode	Resources Used		Performance						Unit
		ALUTs	Memory	C1 Speed Grade	C2 Speed Grade	C3 Speed Grade	I3 Speed Grade	C4 Speed Grade	I4 Speed Grade	
M20K Block	Single-port, all supported widths	0	1	800	730	680	520	570	470	MHz
	Simple dual-port, all supported widths	0	1	800	730	680	520	570	470	MHz
	Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths	0	1	600	550	470	470	410	410	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	520	470	410	410	360	360	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	690	620	520	520	470	470	MHz
	True dual port, all supported widths	0	1	800	730	680	520	570	470	MHz
	ROM, all supported widths	0	1	800	730	680	520	570	470	MHz
	Min Pulse Width (clock high time)	—	—	800	780	830	830	890	890	ps
	Min Pulse Width (clock low time)	—	—	570	520	650	650	720	720	ps

**Notes to Table 2-27:**

- (1) These numbers are preliminary pending silicon characterization.
- (2) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (3) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in  $F_{MAX}$ .

## JTAG Configuration Specifications

Table 2-28 lists the JTAG timing parameters and values for Stratix V devices.

**Table 2-28. JTAG Timing Parameters and Values for Stratix V Devices—Preliminary <sup>(1)</sup>**

Symbol	Description	Min	Max	Unit
$t_{JCP}$	TCK clock period	30	—	ns
$t_{JCH}$	TCK clock high time	14	—	ns
$t_{JCL}$	TCK clock low time	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns
$t_{JPH}$	JTAG port hold time	5	—	ns
$t_{JPCO}$	JTAG port clock to output	—	11 <sup>(2)</sup>	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	14 <sup>(2)</sup>	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	14 <sup>(2)</sup>	ns

**Notes to Table 2-28:**

- (1) These numbers are preliminary pending silicon characterization.
- (2) A 1 ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{JPCO} = 12$  ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

## Temperature Sensing Diode Specifications

Table 2-29 lists the specifications for the Stratix V temperature sensing diode.

**Table 2-29. External Temperature Sensing Diode Specifications for Stratix V Devices—Preliminary**

Description	Min	Typ	Max	Unit
$I_{\text{bias}}$ , diode source current	8	—	200	$\mu\text{A}$
$V_{\text{bias}}$ , voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	$\Omega$
Diode ideality factor	—	—	1.01	—

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-LVTTL/LVCMOS are capable of a typical 167 MHz and 1.2-LVCMOS at 100 MHz interfacing frequency with a 10 pF load.



The actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specification

Table 2-30 lists high-speed I/O timing for Stratix V devices.

**Table 2-30. High-Speed I/O Specifications for Stratix V Devices—Preliminary <sup>(1), (2)</sup> (Part 1 of 3)**

Symbol	Conditions	-2 Speed Grade			-3 Speed Grade			-4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HSCLK\_in}}$ (input clock frequency) True Differential I/O Standards	Clock boost factor $W = 1$ to 40 <sup>(4)</sup>	5	—	717	5	—	625	5	—	525	MHz
$f_{\text{HSCLK\_in}}$ (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor $W = 1$ to 40 <sup>(4)</sup>	5	—	717	5	—	625	5	—	525	MHz
$f_{\text{HSCLK\_in}}$ (input clock frequency) Single Ended I/O Standards	Clock boost factor $W = 1$ to 40 <sup>(4)</sup>	5	—	520	5	—	420	5	—	420	MHz
$f_{\text{HSCLK\_out}}$ (output clock frequency)	—	5	—	717 <sup>(5)</sup>	5	—	625 <sup>(5)</sup>	5	—	525 <sup>(5)</sup>	MHz

**Table 2-30. High-Speed I/O Specifications for Stratix V Devices—Preliminary <sup>(1)</sup>, <sup>(2)</sup> (Part 2 of 3)**

Symbol	Conditions	-2 Speed Grade			-3 Speed Grade			-4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>Transmitter</b>											
True Differential I/O Standards - $f_{\text{HSDR}}$ (data rate)	SERDES factor J = 3 to 10 <sup>(9)</sup>	(6)	—	1434	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{\text{HSDR}}$ (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10	(6)	—	1100	(6)	—	840	(6)	—	840	Mbps
$t_{\text{x Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{\text{x Jitter}}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.25	UI
$t_{\text{DUTY}}$	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
$t_{\text{RISE}} & t_{\text{FALL}}$	True Differential I/O Standards	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
<b>Receiver</b>											
True Differential I/O Standards - $f_{\text{HSDRDPA}}$ (data rate)	SERDES factor J = 3 to 10	150	—	1434	150	—	1250	150	—	1050	Mbps
$f_{\text{HSDR}}$ (data rate)	SERDES factor J = 3 to 10	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps

**Table 2-30. High-Speed I/O Specifications for Stratix V Devices—Preliminary <sup>(1), (2)</sup> (Part 3 of 3)**

Symbol	Conditions	-2 Speed Grade			-3 Speed Grade			-4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>DPA Mode</b>											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
<b>Soft CDR mode</b>											
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	± PPM
<b>Non DPA Mode</b>											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

**Notes to Table 2-30:**

- (1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) This only applies to DPA and soft-CDR modes.
- (4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.
- (5) This is achieved by using the LVDS clock network.
- (6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
- (8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.
- (9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
- (10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

Figure 2-1 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 2-1. DPA Lock Time Specification with DPA PLL Calibration Enabled**

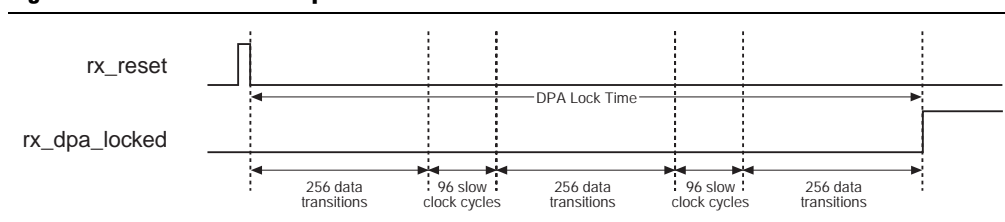


Table 2-31 lists the DPA lock time specifications for Stratix V GX devices.

**Table 2-31. DPA Lock Time Specifications for Stratix V GX Devices Only—Preliminary (Part 1 of 2) <sup>(1), (2), (3)</sup>**

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	000000000111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions

**Table 2-31. DPA Lock Time Specifications for Stratix V GX Devices Only—Preliminary (Part 2 of 2)** <sup>(1), (2), (3)</sup>

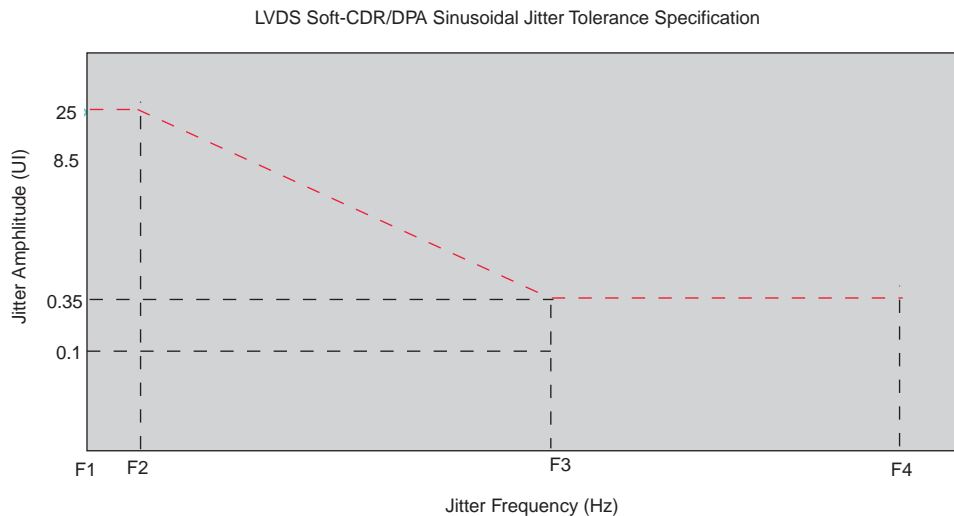
Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

**Notes to Table 2-31:**

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-2 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps. Table 2-32 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps.

**Figure 2-2. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $\geq 1.25$  Gbps**

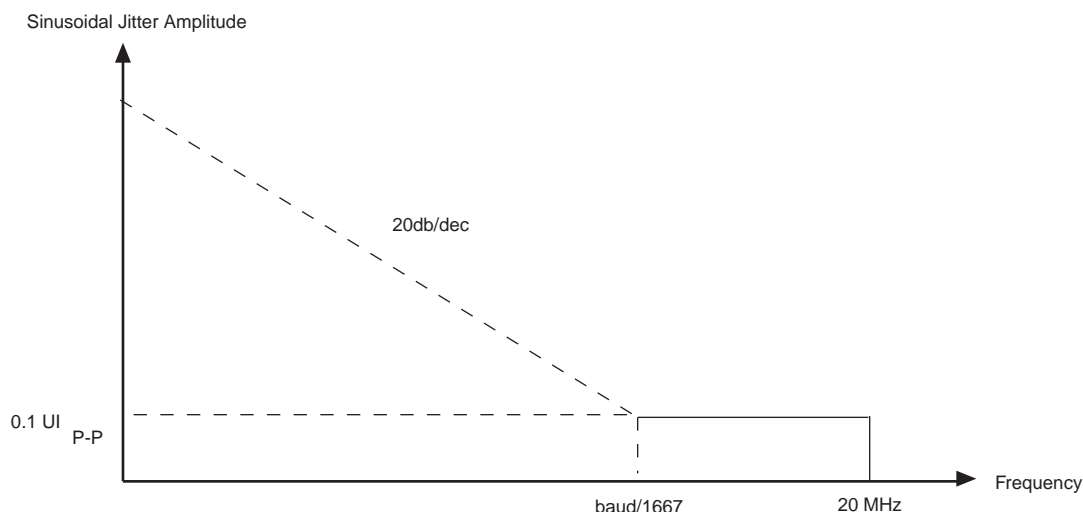


**Table 2-32. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps—Preliminary**

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 2-3 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

**Figure 2-3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps**



### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 2-33 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 2-33. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	Unit
300-1120	300-890	300-890	MHz

**Note to Table 2-33:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 2-34 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 2-34. DQS Phase Offset Delay Per Setting for Stratix V Devices—Preliminary <sup>(1), (2), (3)</sup>**

Speed Grade	Min	Max	Unit
-2	7	13	ps
-3	7	15	ps
-4	7	16	ps

**Notes to Table 2-34:**

- (1) These numbers are preliminary pending silicon characterization.  
 (2) The typical value equals the average of the minimum and maximum values.  
 (3) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 2-35 lists the DQS phase shift error for Stratix V devices.

**Table 2-35. DQS Phase Shift Error Specification for DLL-Delayed Clock ( $t_{DQS\_PSERR}$ ) for Stratix V Devices—Preliminary <sup>(1)</sup>, <sup>(2)</sup>**

Number of DQS Delay Buffers	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	Unit
1	26	28	30	ps
2	52	56	60	ps
3	78	84	90	ps
4	104	112	120	ps

**Notes to Table 2-35:**

- (1) The numbers are preliminary pending silicon characterization.
- (2) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is  $\pm 78$  ps or  $\pm 39$  ps.

Table 2-36 lists the memory output clock jitter specifications for Stratix V devices.

**Table 2-36. Memory Output Clock Jitter Specification for Stratix V Devices <sup>(1)</sup>**

Clock Network	Parameter	Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	-50	50	-55	55	-55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-82.5	82.5	-82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	-75	75	-82.5	82.5	-82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-90	90	-90	90	ps
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-45	45	-56	56	ps

**Note to Table 2-36:**

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

## OCT Calibration Block Specifications

Table 2-37 lists the OCT calibration block specifications for Stratix V devices.

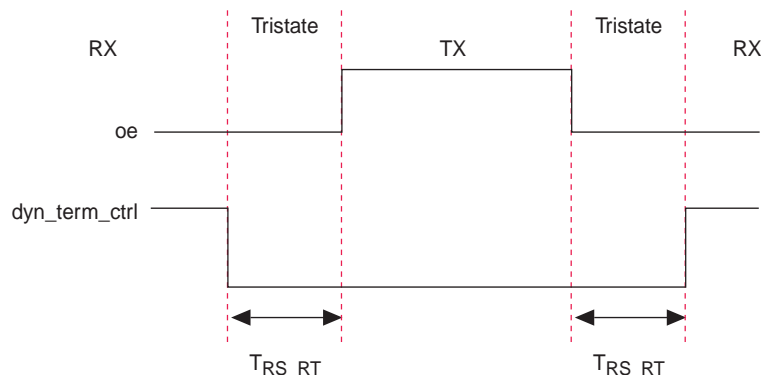
**Table 2-37. OCT Calibration Block Specifications for Stratix V Devices—Preliminary <sup>(1)</sup>**

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT R <sub>S</sub> /R <sub>T</sub> calibration	—	1000	—	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R <sub>S</sub> and R <sub>T</sub> (Figure 2-4)	—	2.5	—	ns

**Note to Table 2-37:**

(1) Pending silicon characterization.

**Figure 2-4. Timing Diagram for oe and dyn\_term\_ctrl Signals**



## Duty Cycle Distortion (DCD) Specifications

Table 2-38 lists the worst-case DCD for Stratix V devices.

**Table 2-38. Worst-Case DCD on Stratix V I/O Pins—Preliminary <sup>(1)</sup>**

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

**Note to Table 2-38:**

(1) The numbers are preliminary pending silicon characterization.

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the [Stratix V Devices Documentation](#) webpage.

## Programmable IOE Delay

Table 2-39 lists the Stratix V IOE programmable delay settings.

**Table 2-39. IOE Programmable Delay for Stratix V Devices—Preliminary <sup>(1)</sup>**

Parameter <sup>(2)</sup>	Available Settings	Min Offset <sup>(3)</sup>	Fast Model		Slow Model					Unit
			Industrial	Commercial	C2	C3	C4	I3	I4	
D1	63	0	0.471	0.514	0.800	0.843	0.918	0.850	0.924	ns
D2	31	0	0.274	0.274	0.423	0.456	0.501	0.453	0.498	ns
D3	7	0	1.668	1.735	2.830	2.985	3.252	3.007	3.274	ns
D5	63	0	0.493	0.474	0.835	0.882	0.960	0.888	0.966	ns
D6	31	0	0.273	0.258	0.463	0.488	0.532	0.492	0.536	ns

**Notes to Table 2-39:**

- (1) Pending the Quartus II software extraction.
- (2) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (3) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 2-40 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 2-40. Programmable Output Buffer Delay for Stratix V Devices—Preliminary <sup>(1)</sup>, <sup>(2)</sup>**

Symbol	Parameter	Typical	Unit
D <sub>OUTBUF</sub>	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

**Notes to Table 2-40:**

- (1) Pending the Quartus II software extraction.
- (2) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

# Glossary

Table 2-41 lists the glossary for this chapter.

Table 2-41. Glossary (Part 1 of 4)

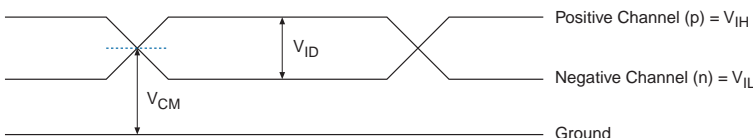
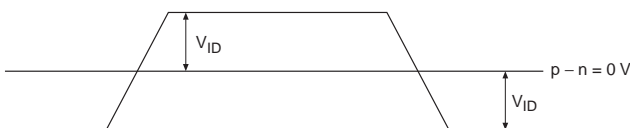
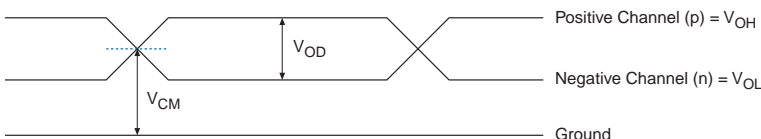
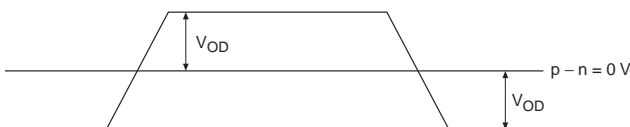
Letter	Subject	Definitions
A		
B		
C		
D	Differential I/O Standards	<p><i>Receiver Input Waveforms</i></p> <p><b>Single-Ended Waveform</b></p>  <p>Positive Channel (p) = <math>V_{IH}</math> Negative Channel (n) = <math>V_{IL}</math> Ground</p> <p><b>Differential Waveform</b></p>  <p><math>p - n = 0\text{ V}</math> <math>V_{ID}</math></p> <p><i>Transmitter Output Waveforms</i></p> <p><b>Single-Ended Waveform</b></p>  <p>Positive Channel (p) = <math>V_{OH}</math> Negative Channel (n) = <math>V_{OL}</math> Ground</p> <p><b>Differential Waveform</b></p>  <p><math>p - n = 0\text{ V}</math> <math>V_{OD}</math></p>
E		
F	$f_{HSCLK}$	Left and right PLL input clock frequency.
	$f_{HSDR}$	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate ( $f_{HSDR} = 1/TUI$ ), non-DPA.
	$f_{HS DRDPA}$	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate ( $f_{HS DRDPA} = 1/TUI$ ), DPA.
G		
H		
I		

Table 2-41. Glossary (Part 2 of 4)

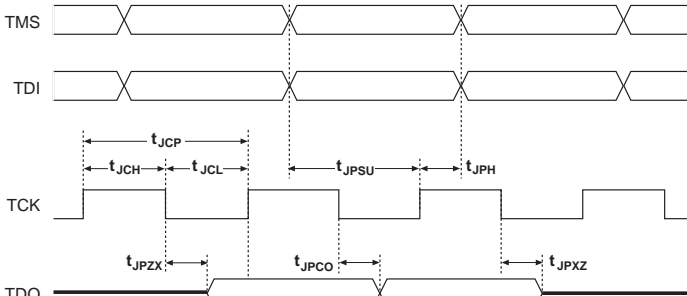
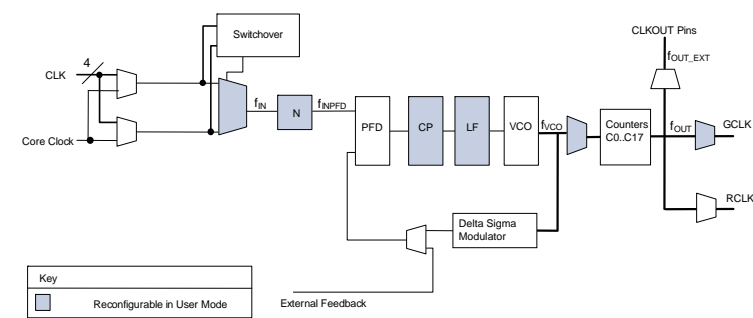
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	<p>JTAG Timing Specifications:</p> 
K L M N O	—	—
P	PLL Specifications	<p><b>Diagram of PLL Specifications (1)</b></p>  <p><b>Note:</b> (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
Q	—	—
R	R <sub>L</sub>	Receiver differential input discrete resistor (external to the Stratix V device).

Table 2-41. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for <b>SSTI</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>
T	$t_c$	High-speed receiver and transmitter input and output clock period.
	<b>TCCS (channel-to-channel-skew)</b>	The timing difference between the fastest and slowest output edges, including $t_{c0}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).
	$t_{DUTY}$	High-speed I/O block—Duty cycle on the high-speed transmitter output clock. <b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_c/w$ )
	$t_{FALL}$	Signal high-to-low transition time (80-20%)
	$t_{INCCJ}$	Cycle-to-cycle jitter tolerance on the PLL clock input.
	$t_{OUTPJ\_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	$t_{OUTPJ\_DC}$	Period jitter on the dedicated clock output driven by a PLL.
$t_{RISE}$	Signal low-to-high transition time (20-80%)	
U	—	—

**Table 2-41. Glossary (Part 4 of 4)**

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{ICM}$	Input common mode voltage—The common mode of the differential signal at the receiver.
	$V_{ID}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	$V_{IH}$	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	$V_{IL}$	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	$V_{OCM}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
	$V_{OD}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	$V_{SWING}$	Differential input voltage
	$V_X$	Input differential cross point voltage
$V_{OX}$	Output differential cross point voltage	
W	W	High-speed I/O block—clock boost factor
X		
Y	—	—
Z		

## Document Revision History

Table 2-42 lists the revision history for this chapter.

**Table 2-42. Document Revision History (Part 1 of 2)**

Date	Version	Changes
February 2012	2.3	<ul style="list-style-type: none"> <li>Updated Table 2-20, Table 2-25, Table 2-26, and Table 2-27.</li> </ul>
December 2011	2.2	<ul style="list-style-type: none"> <li>Added Table 2-31.</li> <li>Updated Table 2-28 and Table 2-34.</li> </ul>
November 2011	2.1	<ul style="list-style-type: none"> <li>Added Table 2-2 and Table 2-21 and updated Table 2-5 with information about Stratix V GT devices.</li> <li>Updated Table 2-11, Table 2-13, Table 2-20, and Table 2-25.</li> <li>Various edits throughout to fix SPRs.</li> </ul>

**Table 2-42. Document Revision History (Part 2 of 2)**

Date	Version	Changes
May 2011	2.0	<ul style="list-style-type: none"><li>■ Updated Table 2-4, Table 2-18, Table 2-19, Table 2-21, Table 2-22, Table 2-23, and Table 2-24.</li><li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li><li>■ Chapter moved to Volume 1.</li><li>■ Minor text edits.</li></ul>
December 2010	1.1	<ul style="list-style-type: none"><li>■ Updated Table 1-2, Table 1-4, Table 1-19, and Table 1-23.</li><li>■ Converted chapter to the new template.</li><li>■ Minor text edits.</li></ul>
July 2010	1.0	Initial release.

