

This document lists the Stratix[®] V device family features that are not enabled in the Quartus[®] II software version 11.1. However, these features will be supported in a future release of the Quartus II software.

Table 1 lists the current available device support.

Table 1. Support for Stratix V Devices

Device Variant	Support
Stratix V E	The Stratix V E FPGAs will be supported in a future release of the Quartus II software.
Stratix V GS	Select Stratix V GS devices are currently supported in the Quartus II software.
Stratix V GX	Select Stratix V GX devices are currently supported in the Quartus II software.
Stratix V GT	The Stratix V GT FPGAs will be supported in a future release of the Quartus II software.

Features of the Stratix V Device Family

Table 2 lists the configuration features that will be supported in a future version of the Quartus II software.

Table 2. Configuration Support for Stratix V Devices

Feature	Future Support
Partial reconfiguration	You will be able to partially reconfigure Stratix V devices while the rest of the device is still operating.
Configuration via PCI Express [®] (PCIe [®])	Configuration via PCIe will allow you to configure the FPGA fabric via the PCIe link using the designated PCIe Hard IP.

Table 3 lists the FPGA fabric features that will be supported in a future version of the Quartus II software.

Table 3. FPGA Fabric Support for Stratix V Devices

Feature	Future Support
Single event upset (SEU) mitigation	The following SEU features will be supported in a future version of the Quartus II software: <ul style="list-style-type: none"> ■ Error classification ■ Scrubbing ■ Fault injection
Anti-tamper	Advanced encryption standard (AES) encryption and additional anti-tamper features will be supported closer to silicon availability.

Table 4 lists the external memory features that are currently supported and features that will be supported in a future version of the Quartus II software.

Table 4. External Memory Support for Stratix V Devices

Feature	Current Support	Future Support
DDR3	DDR3 up to 533 MHz with preliminary IP	Final IP that enables DDR3 functionality up to 1,066 MHz.
RLDRAM II PHY/Controller IP	Not supported	1,067 Mbps, 533 MHz
QDR II/II+ PHY/Controller IP	Not supported	QDRII—1,400 Mbps, 350 MHz QDRII+—2,200 Mbps, 550 MHz
DDR2/3 RDIMM UniPHY-based controller	RDIMM IP support can be achieved via the ALTMEMPHY-based controller	UniPHY-based DDR2/3 RDIMM IP

Table 5 lists the transceiver standard physical coding sublayer (PCS) features that are currently supported and features that will be supported in a future version of the Quartus II software.

Table 5. Transceiver Standard PCS Support for Stratix V Devices

Feature	Current Support	Future Support
Protocols supported using standard PCS	<ul style="list-style-type: none"> ■ PCIe Gen1/Gen2 x1, x4, and x8 modes ■ XAUI using soft PCS ■ Select custom configurations ■ SerialLite and SerialLite II ■ Fiber Channel 1G, 2G, 4G and 8G ■ SONET OC12, OC48 ■ Gigabit Ethernet (GbE) ■ Serial digital interface (SDI) ■ Deterministic latency (CPRI/OBSAI) ■ SATA/SAS ■ Low latency configurations <p>NOTE: For details regarding configurations supported, refer to the <i>Stratix V Device Handbook</i>.</p>	<p>The following transceiver protocol modes will be supported in a future release of the Quartus II software:</p> <ul style="list-style-type: none"> ■ PCIe Gen3 x1, x4, and x8 modes ■ PCIe Gen1/Gen2/Gen3 x2 mode ■ Serial RapidIO[®] (SRIO) v1.2 and v2.1 ■ HiGig, HiGig+, and HiGig2 ■ XAUI using hard PCS ■ QPI
PCIe	<ul style="list-style-type: none"> ■ PCIe Gen1/Gen2 x1, x4, and x8 modes ■ PCIe low latency synchronous mode ■ Reverse parallel loopback 	<p>The following PCIe features will be supported in a future release of the Quartus II software:</p> <ul style="list-style-type: none"> ■ PCIe Gen1/Gen2 x2 mode ■ PCIe Gen3 x1, x2, x4, and x8 modes ■ Dynamic rate switch between Gen1, Gen2, and Gen3 modes
SRIO	Not supported	<ul style="list-style-type: none"> ■ Hard PCS will be enabled to support SRIO 1.2 and 2.1 protocols. ■ x2 and x4 bonding will be available in addition to independent x1 channels.

Table 6 lists the transceiver 10G PCS features that are currently supported and features that will be supported in a future version of the Quartus II software.

Table 6. Transceiver 10G PCS Support for Stratix V Devices

Feature	Current Support	Future Support
Protocols supported using 10G PCS	<ul style="list-style-type: none"> ■ Interlaken (partial support) ■ 10GBASE-R ■ 10GBASE-KR (partial support) ■ SDI 10G ■ 40G/100G Ethernet (partial support) ■ 10G PON ■ 10G EPON ■ Low latency configurations 	<p>The following transceiver protocol modes using the transceiver 10G PCS will be supported in a future release of the Quartus II software:</p> <ul style="list-style-type: none"> ■ Interlaken (full support) ■ 10GBASE-KR (full support) ■ SFI-S ■ 40G/100G Ethernet (full support) ■ SONET OC192

Table 7 lists the transceiver clocking features that are currently supported and features that will be supported in a future version of the Quartus II software.

Table 7. Transceiver Clocking Support for Stratix V Devices (Part 1 of 2)

Feature	Current Support	Future Support
Input reference clock sources	<ul style="list-style-type: none"> ■ Dedicated <code>refclk</code> pins ■ Fractional phase-locked loops (PLLs) outputs ■ Clock from FPGA fabric 	<p>In addition to dedicated <code>refclk</code> pins, the following input reference clock sources will be enabled:</p> <ul style="list-style-type: none"> ■ Dual-purpose receiver/<code>refclk</code> pins—receiver pins of Transmit-only or unused transceiver channels can be used for sourcing input reference clocks. They will support fewer I/O standards when compared with dedicated <code>refclk</code> pins.
Fractional PLL	<ul style="list-style-type: none"> ■ Supported for use in the FPGA fabric as general purpose PLLs ■ Fractional mode support 	<p>The following fractional PLL features will be supported:</p> <ul style="list-style-type: none"> ■ Ability to use fractional PLLs as transmit PLLs for transceivers ■ Cascading output counters to create counters larger than 512 ■ Dynamic reconfiguration ■ Dynamic clock switchover ■ Dynamic phase shift
PLL cascading	<ul style="list-style-type: none"> ■ Recovered <code>clk</code> to fractional PLL cascade—for repeater-type applications that require clock clean-up. ■ Fractional PLL to transmit PLL cascade—using fractional PLLs to generate multiple input reference clocks for transmit PLLs using a single input clock to the fractional PLL. 	<p>The following transceiver PLL cascading will be supported in the future:</p> <ul style="list-style-type: none"> ■ Clock divider to fractional PLL cascade—to save clock sources in systems by using clocks generated by a transmit PLL in the FPGA fabric.

Table 7. Transceiver Clocking Support for Stratix V Devices (Part 2 of 2)

Feature	Current Support	Future Support
Transmit PLL feedback compensation mode	Not supported	Transmit PLL feedback compensation mode will be enabled to support: <ul style="list-style-type: none"> ■ Deterministic latency by compensating for uncertainty introduced by clock dividers for protocols such as CPRI and OBSAI. ■ Multi-channel bonding for data rates beyond 6 Gbps.
Multi-Channel Bonding	The following are supported: <ul style="list-style-type: none"> ■ Bonding up to five channels for configurations using standard PCS ■ Bonding up to 8 channels for PCIe Gen1/Gen2 configurations 	The following will be supported: <ul style="list-style-type: none"> ■ Side-wide bonding for configurations using standard PCS. Data rates will vary based on the number of channels bonded. The data rates will be determined after characterization. ■ Side-wide bonding for configurations using 10G PCS. Data rates will vary based on the number of channels bonded. The data rates will be determined after characterization.
Flexible master/slave configuration	In bonded configurations, a master channel provides control signals and clocks all the remaining slave channels. Currently, you cannot choose which channel is master.	You will be able to choose which channel will be the master.

Table 8 lists the transceiver PMA features that are currently supported and features that will be supported in a future version of the Quartus II software.

Table 8. Transceiver PMA Support for Stratix V Devices

Feature	Current Support	Future Support
Signal detect and electrical idle	<ul style="list-style-type: none"> ■ Electrical idle for PCIe Gen1 ■ Electrical idle inference for PCIe Gen2 ■ Signal detect for SATA 	<ul style="list-style-type: none"> ■ Electrical idle inference for PCIe Gen3 ■ Signal detect for HyperTransport
GT Channels	<ul style="list-style-type: none"> ■ Synthesis and Simulation ■ Full-Compilation and Fitting 	Full support
Built-in Self Test modes	Not supported	The following patterns will be supported for Built-in Self Test mode: <ul style="list-style-type: none"> ■ PRBS 7 (8G, 10G) ■ PRBS 8 (8G) ■ PRBS 9 (10G) ■ PRBS 10 (8G, 10G) ■ PRBS 23 (8G, 10G) ■ PRBS 31 (10G) ■ High Frequency (8G) ■ Low Frequency (8G)

Table 9 lists the signal conditioning features that will be supported in a future version of the Quartus II software.

Table 9. Signal Conditioning Features Support for Stratix V Devices

Feature	Current Support	Future Support
Decision feedback equalization (DFE)	Not Supported	High-speed signals transmitted across a backplane experience signal attenuation due to skin effect, dielectric losses, and crosstalk. Stratix V devices will provide multi-tap DFE to primarily compensate the backplane attenuation due to crosstalk. DFE is effective in canceling post cursor inter-symbol interference (ISI) by boosting only the high frequency components of a signal without noise amplification. You can use DFE in conjunction with pre-emphasis, linear equalization (manual equalization), and AEQ.

Table 10 lists the transceiver dynamic reconfiguration features that are currently supported and features that will be supported in a future version of the Quartus II software.

Table 10. Transceiver Dynamic Reconfiguration Support for Stratix V Devices

Feature	Current Support	Future Support
Dynamic reconfiguration	The Quartus II software supports dynamic reconfiguration in the following analog parameters of a transceiver PMA: <ul style="list-style-type: none"> ■ Differential output voltage (V_{OD}) ■ Pre-emphasis ■ Equalization ■ DC Gain 	Future versions of the Quartus II software will support dynamic reconfiguration of the following transceiver features: <ul style="list-style-type: none"> ■ Transmitter and receiver termination values ■ Common mode voltage for QPI ■ Channel reconfiguration ■ Transmit PLL reconfiguration ■ Transmit PLL selection ■ Channel and transmit PLL reconfiguration ■ AEQ ■ DFE ■ EyeQ
PCIe hard IP reconfiguration	Not supported	Stratix V devices will support dynamic reconfiguration of the following in the PCIe hard IP: <ul style="list-style-type: none"> ■ Endpoint modes in PCIe Gen1/Gen2 ■ Rootport modes in PCIe Gen1/Gen2 ■ Runtime reconfiguration of PCIe read only registers ■ Runtime switching between endpoint and rootport modes

Table 11 lists another transceiver feature that will be supported in a future version of the Quartus II software.

Table 11. Transceiver Feature Support for Stratix V Devices

Feature	Current Support	Future Support
DC Coupling	Supported for RX and TX with compatible far-end common mode	TBD

Document Revision History

Table 12 shows the revision history for this document.

Table 12. Document Revision History

Date	Version	Changes
March 2012	1.6	Updated Table 4 .
November 2011	1.5	Updated for the Quartus II software 11.1 release.
July 2011	1.4	Updated for the Quartus II software 11.0 release.
December 2010	1.3	Updated document for the Quartus II software 10.1 release.
July 2010	1.2	Updated document for Quartus II software 10.0 release.
April 2010	1.1	Updated item 22 and 23 in Table 1.
April 2010	1.0	Initial release.