

Introduction

Stratix® and Stratix GX devices feature the TriMatrix™ memory structure, composed of three sizes of embedded RAM blocks. TriMatrix memory includes 512-bit M512 blocks, 4-Kbit M4K blocks, and 512-Kbit M-RAM blocks, each of which is configurable to support a wide range of features. Offering up to 10 Mbits of RAM and up to 12 terabits per second of device memory bandwidth, the TriMatrix memory structure makes the Stratix and Stratix GX families ideal for memory-intensive applications.

TriMatrix Memory

TriMatrix memory structures can implement a wide variety of complex memory functions. For example, use the small M512 blocks for first-in first-out (FIFO) functions and clock domain buffering where memory bandwidth is critical. The M4K blocks are an ideal size for applications requiring medium-sized memory, such as asynchronous transfer mode (ATM) cell processing. M-RAM blocks enhance programmable logic device (PLD) memory capabilities for large buffering applications, such as internet protocol (IP) packet buffering and system cache.

TriMatrix memory blocks support various memory configurations, including single-port, simple dual-port, true dual-port (also known as bidirectional dual-port), shift-register, ROM, and FIFO mode. The TriMatrix memory architecture also includes advanced features and capabilities, such as byte enable support, parity-bit support, and mixed-port width support. This chapter describes the various TriMatrix memory modes and features.

[Table 2-1](#) summarizes the features supported by the three sizes of TriMatrix memory.



For more information on selecting which memory block to use, see *AN 207: TriMatrix Memory Selection Using the Quartus II Software*.

Feature	M512 Block	M4K Block	M-RAM Block
Performance	319 MHz	290 MHz	287 MHz
Total RAM bits (including parity bits)	576	4,608	589,824
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144
Parity bits	✓	✓	✓
Byte enable		✓	✓
Single-port memory	✓	✓	✓
Simple dual-port memory	✓	✓	✓
True dual-port memory		✓	✓
Embedded shift register	✓	✓	
ROM	✓	✓	
FIFO buffer	✓	✓	✓
Simple dual-port mixed width support	✓	✓	✓
True dual-port mixed width support		✓	✓
Memory initialization file (.mif)	✓	✓	
Mixed-clock mode	✓	✓	✓
Power-up condition	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Input and output registers (1)	Input and output registers (2)	Output registers
Same-port read-during-write	New data available at positive clock edge	New data available at positive clock edge	New data available at positive clock edge
Mixed-port read-during-write	Outputs set to unknown or old data	Outputs set to unknown or old data	Unknown output

Notes to Table 2–1:

- (1) The `rden` register on the M512 memory block does not have a clear port.
- (2) On the M4K block, asserting the clear port of the `rden` and byte enable registers drives the output of these registers high.

The extremely high memory bandwidth of the Stratix and Stratix GX device families is a result of increased memory capacity and speed. Table 2-2 shows the memory capacity for TriMatrix memory blocks in each Stratix device. Table 2-3 shows the memory capacity for TriMatrix memory blocks in each Stratix GX device.

Table 2-2. TriMatrix Memory Distribution in Stratix Devices

Device	M512 Columns/Blocks	M4K Columns/Blocks	M-RAM Blocks	Total RAM Bits
EP1S10	4 / 94	2 / 60	1	920,448
EP1S20	6 / 194	2 / 82	2	1,669,248
EP1S25	6 / 224	3 / 138	2	1,944,576
EP1S30	7 / 295	3 / 171	4	3,317,184
EP1S40	8 / 384	3 / 183	4	3,423,744
EP1S60	10 / 574	4 / 292	6	5,215,104
EP1S80	11 / 767	4 / 364	9	7,427,520

Table 2-3. TriMatrix Memory Distribution in Stratix GX Devices

Device	M512 Columns/Blocks	M4K Columns/Blocks	M-RAM Blocks	Total RAM Bits
EP1SGX10	4 / 94	2 / 60	1	920,448
EP1SGX25	6 / 224	3 / 138	2	1,944,576
EP1SGX40	8 / 384	3 / 183	4	3,423,744

Clear Signals

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

Parity Bit Support

The memory blocks support a parity bit for each byte. Parity bits are in addition to the amount of memory in each RAM block. For example, the M512 block has 576 bits, 64 of which are optionally used for parity bit

storage. The parity bit, along with logic implemented in logic elements (LEs), can implement parity checking for error detection to ensure data integrity. Parity-size data words can also store user-specified control bits.

Byte Enable Support

In the M4K and M-RAM blocks, byte enables can mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable signals (*wren*), in conjunction with the byte enable signals (*byteena*), controls the RAM block's write operations. The default value for the *byteena* signals is high (enabled), in which case writing is controlled only by the *wren* signals.

Asserting the clear port of the byte enable registers drives the byte enable signals to their default high level.

M4K Blocks

M4K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. Table 2-4 summarizes the byte selection.

byteena	datain × 18	datain × 36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 2-4:

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

M-RAM Blocks

M-RAM blocks support byte enables for the $\times 16$, $\times 18$, $\times 32$, $\times 36$, $\times 64$, and $\times 72$ modes. In the $\times 128$ or $\times 144$ simple dual-port mode, the two sets of byteena signals (byteena_a and byteena_b) combine to form the necessary 16 byte enables. Tables 2–5 and 2–6 summarize the byte selection.

Table 2–5. Byte Enable for M-RAM Blocks Notes (1), (2)

byteena	datain $\times 18$	datain $\times 36$	datain $\times 72$
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Notes to Table 2–5:

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, that is, in $\times 16$, $\times 32$, and $\times 64$ modes.

Table 2–6. M-RAM Combined Byte Selection for $\times 144$ Mode (Part 1 of 2), Notes (1), (2)

byteena_a	datain $\times 144$
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]

Table 2–6. M-RAM Combined Byte Selection for $\times 144$ Mode (Part 2 of 2), Notes (1), (2)

byteena_a	datain $\times 144$
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

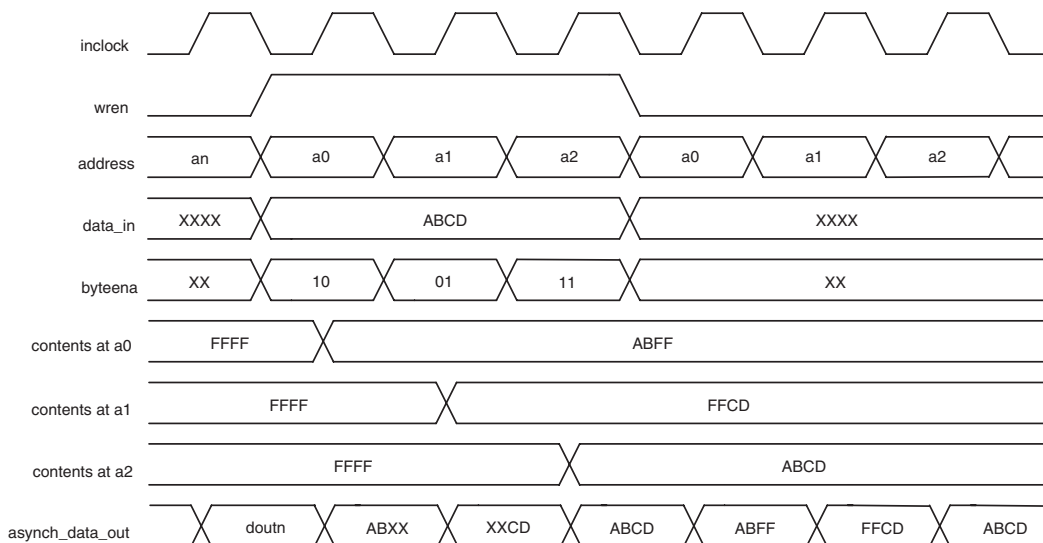
Notes to Table 2–6:

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in $\times 16$, $\times 32$, $\times 64$, and $\times 128$ modes.

Byte Enable Functional Waveform

Figure 2–1 shows how both the wren and the byteena signals control the write operations of the RAM.

Figure 2–1. Byte Enable Functional Waveform Note (1)



Note to Figure 2–1:

- (1) For more information on simulation output when a read-during-write occurs at the same address location, see “Read-During-Write Operation at the Same Address” on page 2–25.

Using TriMatrix Memory

The TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. All TriMatrix memory blocks are pipelined, meaning that all inputs are registered, but outputs are either registered or combinatorial. TriMatrix memory can emulate a flow-through memory by using combinatorial outputs.



For more information, see *AN 210: Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Designs*.

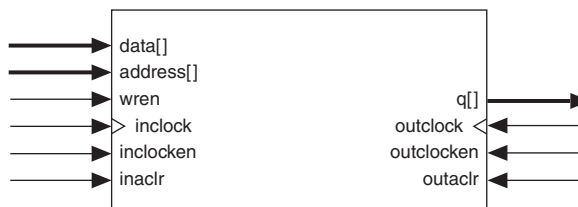
Depending on the TriMatrix memory block type, the memory can have various modes, including:

- Single-port
- Simple dual-port
- True dual-port (bidirectional dual-port)
- Shift-register
- ROM
- FIFO

Implementing Single-Port Mode

Single-port mode supports non-simultaneous reads and writes. [Figure 2-2](#) shows the single-port memory configuration for TriMatrix memory. All memory block types support the single-port mode.

Figure 2-2. Single-Port Memory *Note (1)*



Note to Figure 2-2:

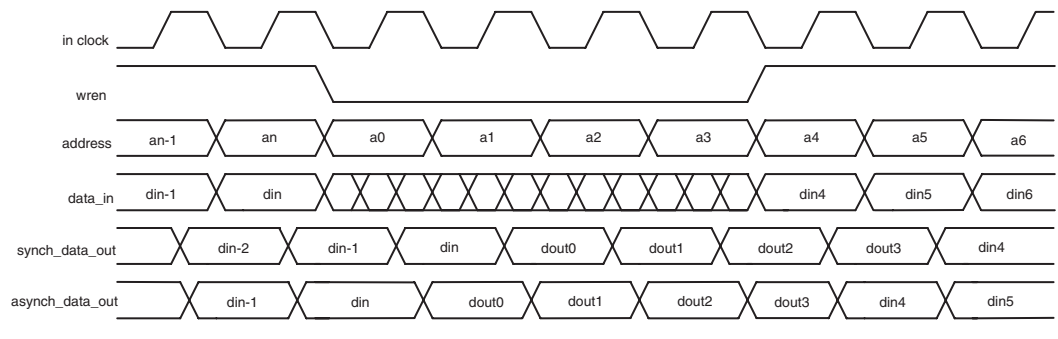
(1) Two single-port memory blocks can be implemented in a single M4K block.

M4K memory blocks can also be divided in half and used for two independent single-port RAM blocks. The Altera Quartus II software automatically uses this single-port memory packing when running low on memory resources. To force two single-port memories into one M4K block, first ensure that each of the two independent RAM blocks is equal to or less than half the size of the M4K block. Second, assign both single-port RAMs to the same M4K block.

In the single-port RAM configuration, the outputs can only be in read-during-write mode, which means that during the write operation, data written to the RAM flows through to the RAM outputs. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle it was written on. For more information about read-during-write mode, see “Read-During-Write Operation at the Same Address” on page 2-25.

Figure 2-3 shows timing waveforms for read and write operations in single-port mode.

Figure 2-3. Single-Port Timing Waveforms

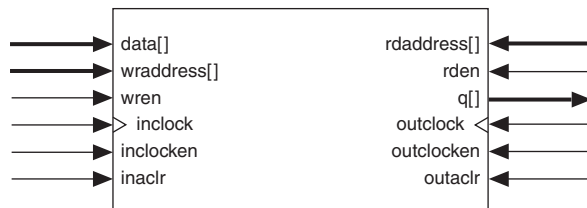


Implementing Simple Dual-Port Mode

Simple dual-port memory supports a simultaneous read and write. Figure 2-4 shows the simple dual-port memory configuration for TriMatrix memory. All memory block types support this configuration.

Figure 2-4. Simple Dual-Port Memory Note (1)

Dual-Port Memory



Note to Figure 2-4:

- (1) Simple dual-port RAM supports read/write clock mode in addition to the input/output clock mode shown.

TriMatrix memory supports mixed-width configurations, allowing different read and write port widths. When using mixed-width mode, the LSB is written to or read from first. For example, take a RAM that is set up in mixed-width mode with write data width $\times 8$ and read data width $\times 2$. If a binary 00000001 is written to write dress 0, the following is read out of the $\times 2$ output side:

Read Address	$\times 2$ data
00	01(LSB of $\times 8$ data)
01	00
10	00
11	00(MSB of $\times 8$ data)

Tables 2-7 to 2-9 show the mixed width configurations for the M512, M4K, and M-RAM blocks, respectively.

Table 2-7. M512 Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port						
	512×1	256×2	128×4	64×8	32×16	64×9	32×18
512×1	✓	✓	✓	✓	✓		
256×2	✓	✓	✓	✓	✓		
128×4	✓	✓	✓		✓		
64×8	✓	✓		✓			
32×16	✓	✓	✓		✓		
64×9						✓	
32×18							✓

Table 2-8. M4K Block Mixed-Width Configurations (Simple Dual-Port Mode) (Part 1 of 2)

Read Port	Write Port								
	$4K \times 1$	$2K \times 2$	$1K \times 4$	512×8	256×16	128×32	512×9	256×18	128×36
$4K \times 1$	✓	✓	✓	✓	✓	✓			
$2K \times 2$	✓	✓	✓	✓	✓	✓			
$1K \times 4$	✓	✓	✓	✓	✓	✓			
512×8	✓	✓	✓	✓	✓	✓			
256×16	✓	✓	✓	✓	✓	✓			

Table 2–8. M4K Block Mixed-Width Configurations (Simple Dual-Port Mode) (Part 2 of 2)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 2–9. M-RAM Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port				
	64K × 9	32K × 18	16K × 36	8K × 72	4K × 144
64K × 9	✓	✓	✓	✓	
32K × 18	✓	✓	✓	✓	
16K × 36	✓	✓	✓	✓	
8K × 72	✓	✓	✓	✓	
4K × 144					✓

M512 blocks support serializer and deserializer (SERDES) applications. By using the mixed-width support in combination with double data rate (DDR) I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks.



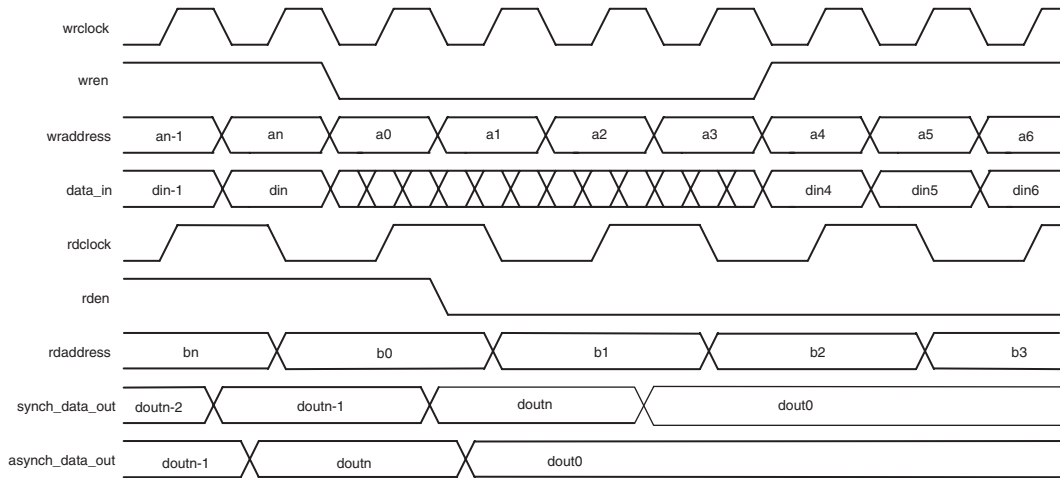
For more information on Stratix device I/O structure see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1*. For more information on Stratix GX device I/O structure see the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.

In simple dual-port mode, the M512 and M4K blocks have one write enable and one read enable signal. The M512 does not support a clear port on the `rden` register. On the M4K block, asserting the clear port of the `rden` register drives `rden` high, which allows the read operation to occur. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is either unknown or can be set to output the old data stored at the memory address. For more information, see [“Read-During-Write Operation at the Same Address”](#) on page 2–25.

M-RAM blocks have one write enable signal in simple dual-port mode. To perform a write operation, the write enable is held high. The M-RAM block is always enabled for read operation. If the read address and the write address select the same address location during a write operation, the M-RAM block output is unknown.

Figure 2-5 shows timing waveforms for read and write operations in simple dual-port mode.

Figure 2-5. Simple Dual-Port Timing Waveforms *Note (1)*

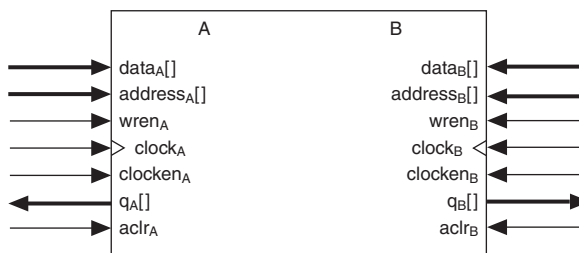


Note to Figure 2-5:

- (1) The `rden` signal is not available in the M-RAM block. A M-RAM block in simple dual-port mode is always reading out the data stored at the current read address location.

Implementing True Dual-Port Mode

M4K and M-RAM blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 2-6 shows the true dual-port memory configuration for TriMatrix memory.

Figure 2–6. True Dual-Port Memory Note (1)**Note to Figure 2–6:**

- (1) True dual-port memory supports input/output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M4K and M-RAM blocks in true dual-port mode is 256×16 -bit ($\times 18$ -bit with parity) and $8K \times 64$ -bit ($\times 72$ -bit with parity), respectively. The 128×32 -bit ($\times 36$ -bit with parity) configuration of the M4K block and the $4K \times 128$ -bit ($\times 144$ -bit with parity) configuration of the M-RAM block are unavailable because the number of output drivers is equivalent to the maximum bit width of the respective memory block. Because true dual-port RAM has outputs on two ports, the maximum width of the true dual-port RAM equals half of the total number of output drivers. Tables 2–10 and 2–11 list the possible M4K RAM block and M-RAM block configurations, respectively.

Table 2–10. M4K Block Mixed-Port Width Configurations (True Dual-Port)

Port A	Port B						
	$4K \times 1$	$2K \times 2$	$1K \times 4$	512×8	256×16	512×9	256×18
$4K \times 1$	✓	✓	✓	✓	✓		
$2K \times 2$	✓	✓	✓	✓	✓		
$1K \times 4$	✓	✓	✓	✓	✓		
512×8	✓	✓	✓	✓	✓		
256×16	✓	✓	✓	✓	✓		
512×9						✓	✓
256×18						✓	✓

Table 2–11. M-RAM Block Mixed-Port Width Configurations (True Dual-Port)

Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

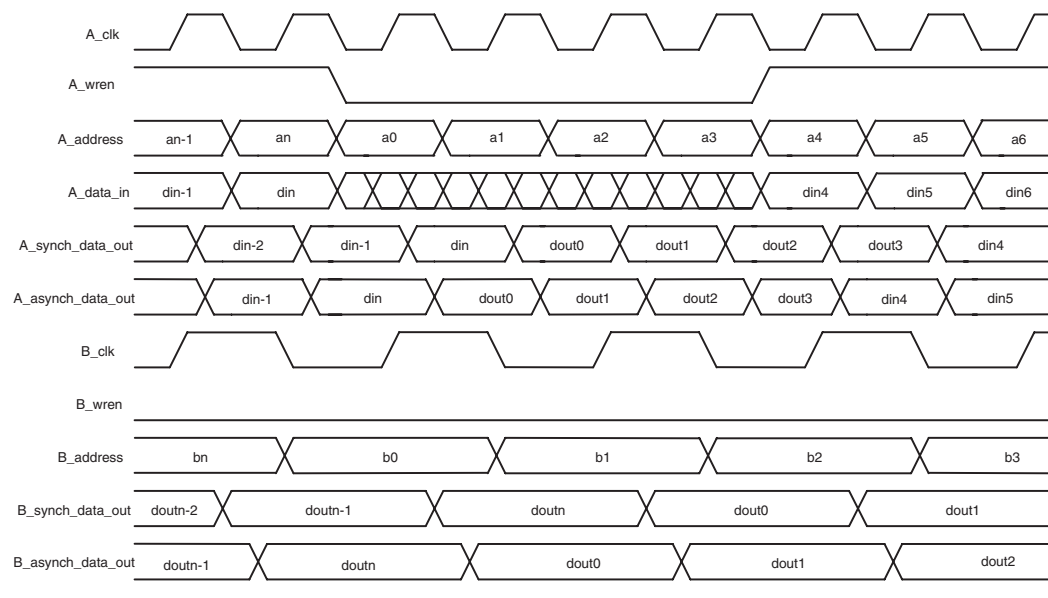
In true dual-port configuration, the RAM outputs can only be configured for read-during-write mode. This means that during write operation, data being written to the A or B port of the RAM flows through to the A or B outputs, respectively. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle it was written on. For waveforms and information on mixed-port read-during-write mode, see [“Read-During-Write Operation at the Same Address” on page 2–25](#).

Potential write contentions must be resolved external to the RAM because writing to the same address location at both ports results in unknown data storage at that location. Data is written on the rising edge of the write clock for the M-RAM block. For a valid write operation to the same address of the M-RAM block, the rising edge of the write clock for port A must occur following the maximum write cycle time interval after the rising edge of the write clock for port B. Since data is written into the M512 and M4K blocks at the falling edge of the write clock, the rising edge of the write clock for port A should occur following half of the maximum write cycle time interval after the falling edge of the write clock for port B. If this timing is not met, the data stored in that particular address is invalid.



See the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1* for the maximum synchronous write cycle time.

[Figure 2–7](#) shows true dual-port timing waveforms for write operation at port A and read operation at port B.

Figure 2–7. True Dual-Port Timing Waveforms

Implementing Shift-Register Mode

Embedded memory block configurations can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops that can quickly consume many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation.

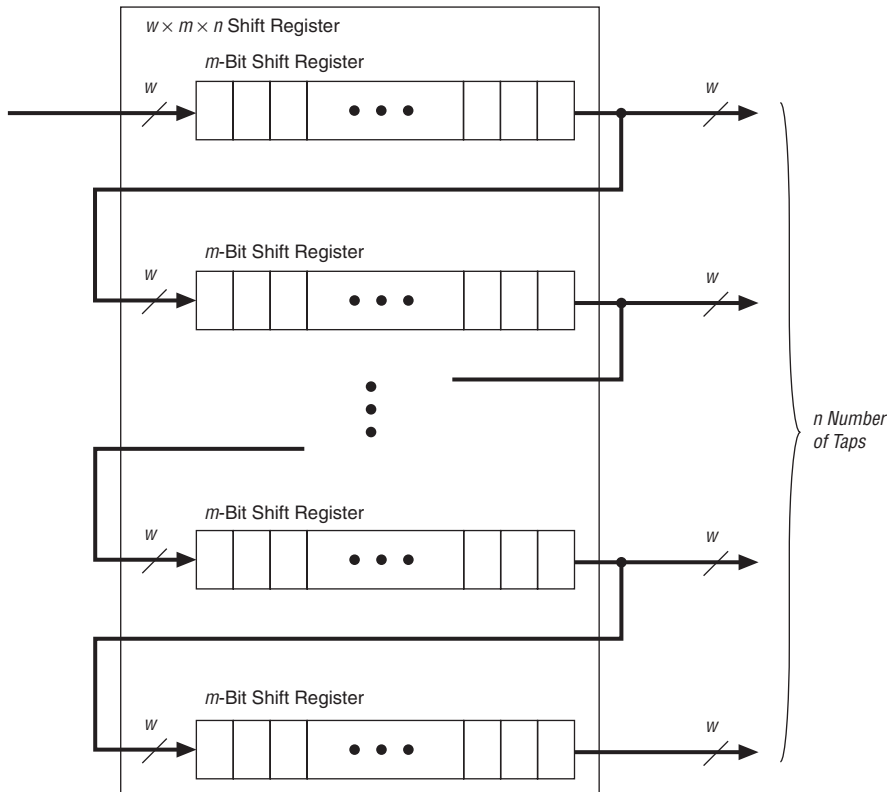
The size of a $(w \times m \times n)$ shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n). The size of a $(w \times m \times n)$ shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512 block and 4,608 bits for the M4K block. In addition, the size of $w \times n$ must be less than or equal to the maximum width of the respective block: 18 bits for the M512 block and 36 bits for the M4K block. If a larger shift register is required, the memory blocks can be cascaded together.



M-RAM blocks do not support the shift-register mode.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift-register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 2-8 shows the TriMatrix memory block in the shift-register mode.

Figure 2-8. Shift-Register Memory Configuration



Implementing ROM Mode

The M512 and the M4K blocks support ROM mode. Use a memory initialization file (.mif) to initialize the ROM contents of M512 and M4K blocks. The M-RAM block does not support ROM mode.

All Stratix memory configurations must have synchronous inputs; therefore, the address lines of the ROM are registered. The outputs can be registered or combinatorial. The ROM read operation is identical to the read operation in the single-port RAM configuration.

Implementing FIFO Buffers

While the small M512 memory blocks are ideal for designs with many shallow FIFO buffers, all three memory sizes support FIFO mode.

All memory configurations have synchronous inputs; however, the FIFO buffer outputs are always combinatorial. Simultaneous read and write from an empty FIFO is not supported.

Clock Modes

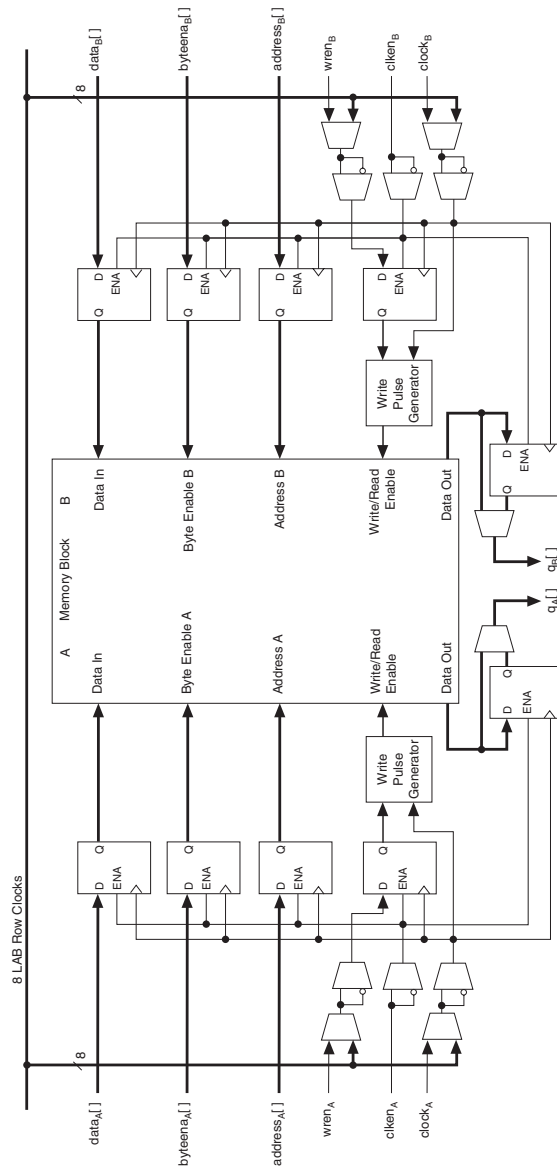
Depending on the TriMatrix memory mode, independent, input/output, read/write, and/or single-port clock modes are available. [Table 2–12](#) shows the clock modes supported by the TriMatrix memory modes.

Clocking Mode	True-Dual Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	
Read/write		✓	
Single-port			✓

Independent Clock Mode

The TriMatrix memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables and asynchronous clear signals for port A and B registers. [Figure 2–9](#) shows a TriMatrix memory block in independent clock mode.

Figure 2-9. Independent Clock Mode Note (1), (2)

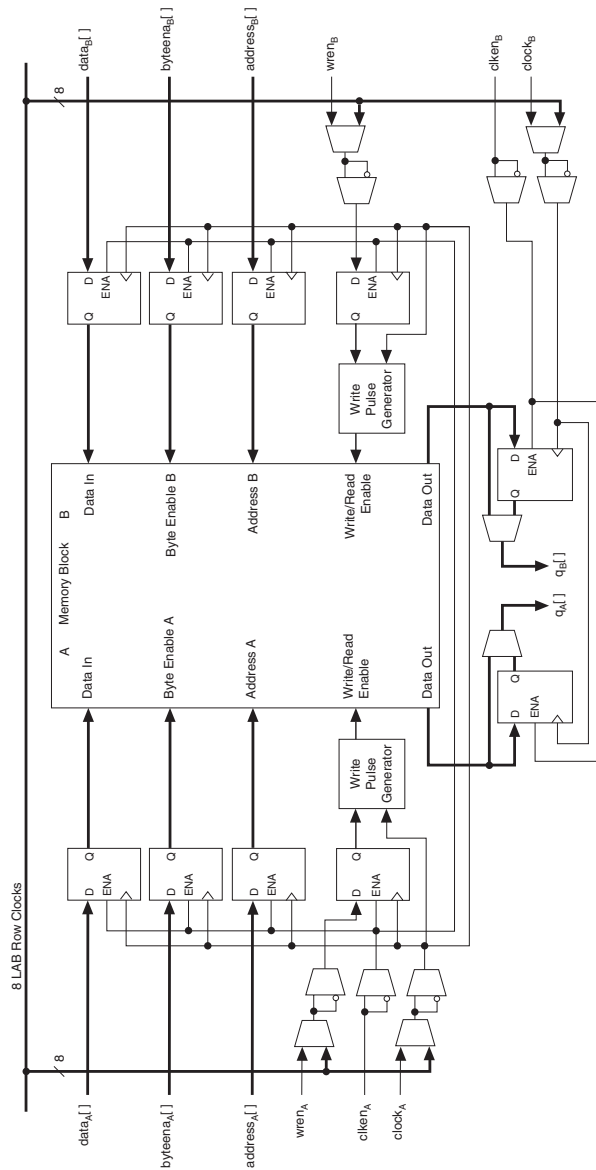
**Note to Figure 2-9:**

- (1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.
- (2) All registers shown have asynchronous clear ports, except when using the M-RAM. M-RAM blocks have asynchronous clear ports on their output registers only.

Input/Output Clock Mode

The TriMatrix memory blocks can implement input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port also supports independent clock enables and asynchronous clear signals for input and output registers. [Figures 2-10](#) and [2-11](#) show the memory block in input/output clock mode for true and simple dual-port modes, respectively.

Figure 2-10. Input/Output Clock Mode in True Dual-Port Mode *Note (1)*

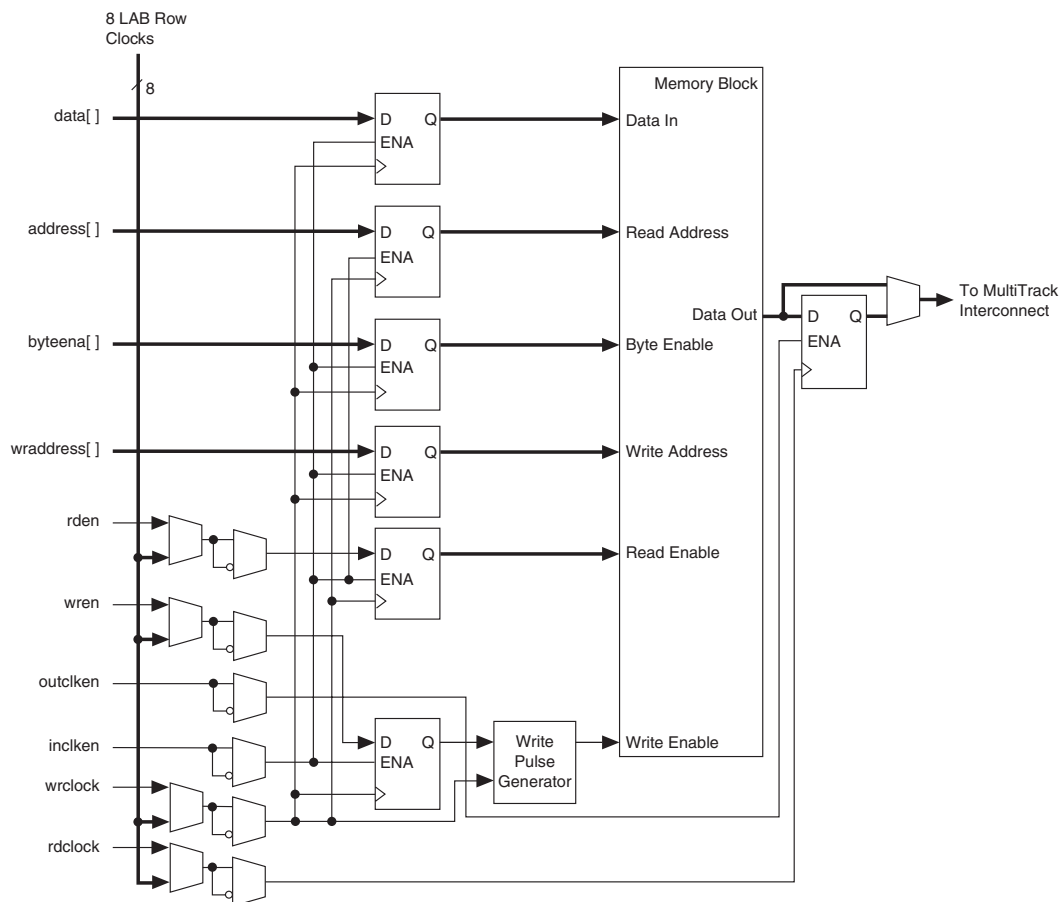


Note to Figure 2-10:

- (1) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

All registers shown have asynchronous clear ports, except when using the M-RAM. M-RAM blocks have asynchronous clear ports on their output registers only.

Figure 2–11. Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2), (3), (4)*



Notes to Figure 2–11:

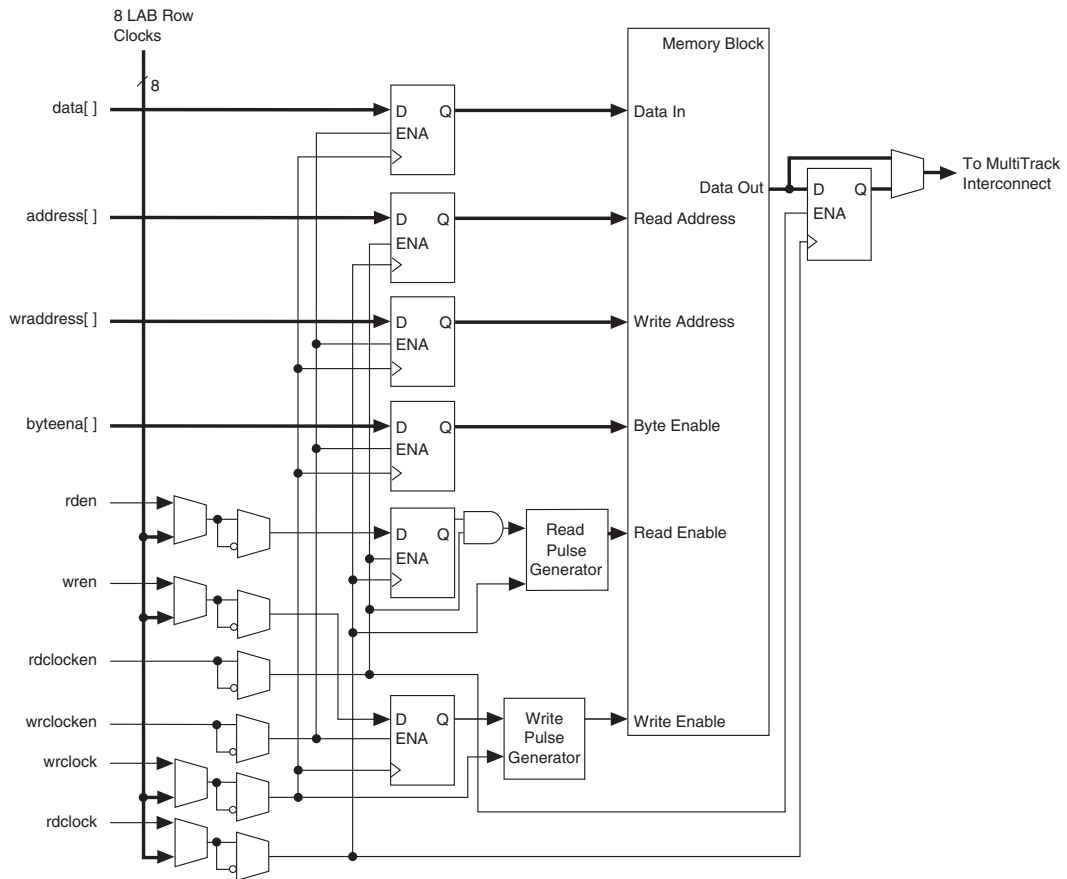
- (1) The *rden* signal is not available in the M-RAM block. A M-RAM block in simple dual-port mode is always reading out the data stored at the current read address location.
- (2) For more information on the MultiTrack™ interconnect, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.
- (3) All registers shown have asynchronous clear ports, except when using the M-RAM. M-RAM blocks have asynchronous clear ports on their output registers only.
- (4) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Read/Write Clock Mode

The TriMatrix memory blocks can implement read/write clock mode for simple dual-port memory. This mode can use up to two clocks. The write clock controls the block's data inputs, *wraddress*, and *wren*. The read clock controls the data output, *rdaddress*, and *rden*. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers.

Figure 2–12 shows a memory block in read/write clock mode.

Figure 2–12. Read/Write Clock Mode in Simple Dual-Port Mode *Notes (1), (2), (3)*



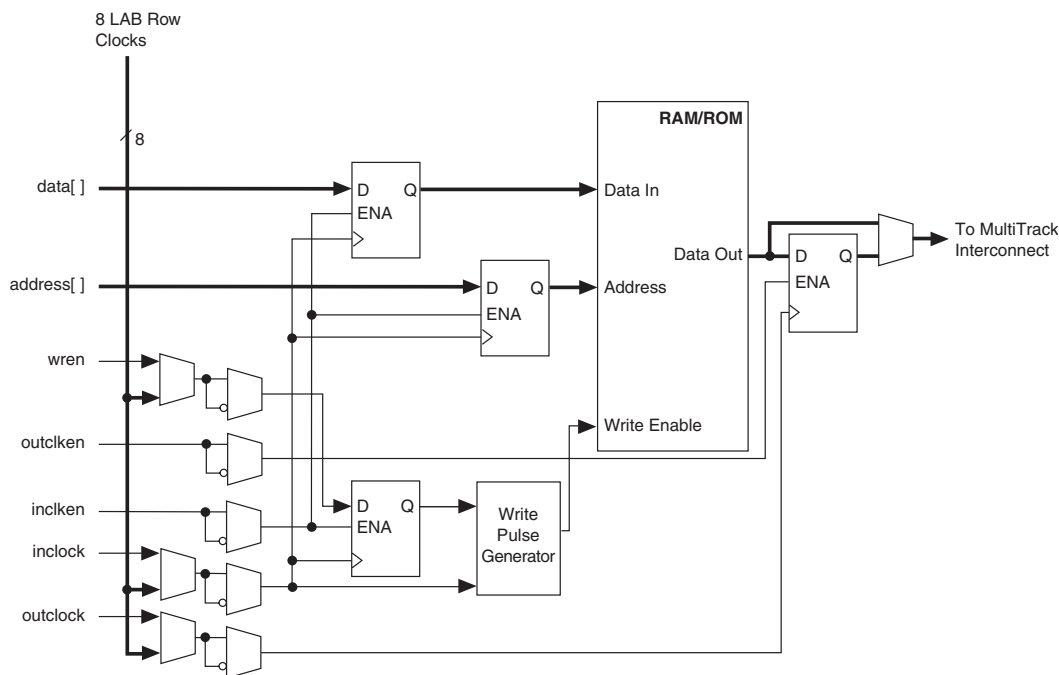
Notes to Figure 2–12:

- (1) For more information on the MultiTrack interconnect, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.
- (2) All registers shown have asynchronous clear ports, except when using the M-RAM. M-RAM blocks have asynchronous clear ports on their output registers only.
- (3) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Single-Port Mode

The TriMatrix memory blocks can implement single-port clock mode for single-port memory mode. Single-port mode is used when simultaneous reads and writes are not required. See [Figure 2-13](#). A single block in a memory block can support up to two single-port mode RAM blocks in M4K blocks.

Figure 2-13. Single-Port Mode *Notes (1), (2), (3)*



Notes to [Figure 2-13](#):

- (1) For more information on the MultiTrack interconnect, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.
- (2) All registers shown have asynchronous clear ports, except when using the M-RAM. M-RAM blocks have asynchronous clear ports on their output registers only.
- (3) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Designing With TriMatrix Memory

When instantiating TriMatrix memory you must understand the various features that set it apart from other memory architectures. The following sections describe some of the important attributes and functionality of TriMatrix memory.



For information on the difference between APEX-style memory and TriMatrix memory, see the *Transitioning APEX Designs to Stratix Devices* chapter.

Selecting TriMatrix Memory Blocks

The Quartus II software automatically partitions user-defined memory into embedded memory blocks using the most efficient size combinations. The memory can also be manually assigned to a specific block size or a mixture of block sizes. [Table 2-1 on page 2-2](#) is a guide for selecting a TriMatrix memory block size based on supported features.



Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.



For more information on selecting which memory block to use, see *AN 207: TriMatrix Memory Selection Using the Quartus II Software*.



Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Pipeline & Flow-Through Modes

TriMatrix memory architecture implements synchronous (pipelined) RAM by registering both the input and output signals to the RAM block. All TriMatrix memory inputs are registered providing synchronous write cycles. In synchronous operation, RAM generates its own self-timed strobe write enable (*wren*) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM *wren* signal while ensuring its data and address signals meet setup and hold time specifications relative to the *wren* signal. The output registers can be bypassed.

In an asynchronous memory neither the input nor the output is registered. While Stratix and Stratix GX devices do not support asynchronous memory, they do support a flow-through read where the output data is available during the clock cycle when the read address is driven into it. Flow-through reading is possible in the simple and true dual-port modes of the M512 and M4K blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.



For more information, see *AN 210: Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Devices*.

Power-up Conditions & Memory Initialization

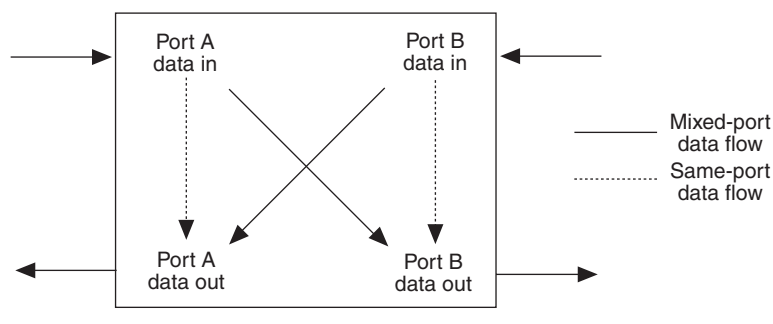
Upon power-up, TriMatrix memory is in an idle state. The M512 and M4K block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if a memory initialization file is used to pre-load the contents of the RAM block, the outputs still power-up cleared. For example, if address 0 is pre-initialized to FF, the M512 and M4K blocks power-up with the output at 00.

M-RAM blocks do not support memory initialization files; therefore, they cannot be pre-loaded with data upon power-up. M-RAM blocks combinatorial outputs and memory controls always power-up to an unknown state. If M-RAM block outputs are registered, the registers power-up cleared. The undefined output appears one clock cycle later. The output remains undefined until a read operation is performed on an address that has been written to.

Read-During-Write Operation at the Same Address

The following two sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two types of read-during-write operations: same-port and mixed-port. [Figure 2-14](#) illustrates the difference in data flow between same-port and mixed-port read-during-write.

Figure 2-14. Read-During-Write Data Flow

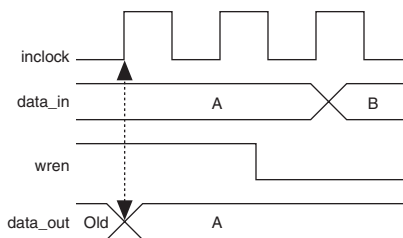


Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle it was written on. This behavior is valid on all memory-block sizes. See [Figure 2-15](#) for a sample functional waveform.

When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown. (See [Figure 2-1 on page 2-6](#).) The non-masked bytes are read out as shown in [Figure 2-15](#).

Figure 2-15. Same-Port Read-During-Write Functionality Note (1)



Note to [Figure 2-15](#):

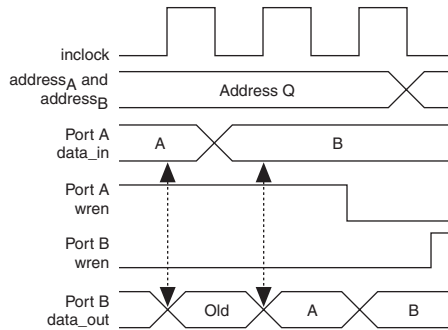
(1) Outputs are not registered.

Mixed-Port Read-During-Write Mode

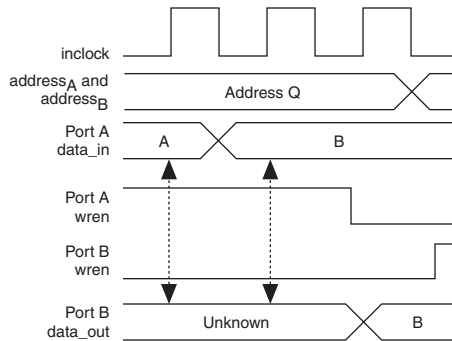
This mode is used when a RAM in simple or true dual-port mode has one port reading and the other port writing to the same address location with the same clock.

The `READ_DURING_WRITE_MODE_MIXED_PORTS` parameter for M512 and M4K memory blocks determines whether to output the old data at the address or a “don’t care” value. Setting this parameter to `OLD_DATA` outputs the old data at that address. Setting this parameter to `DONT_CARE` outputs a “don’t care” or unknown value. See [Figures 2-16 and 2-17](#) for sample functional waveforms showing this operation. These figures assume that the outputs are not registered.

The `DONT_CARE` setting allows memory implementation in any TriMatrix memory block. The `OLD_DATA` setting restricts memory implementation to only M512 or M4K memory blocks. Selecting `DONT_CARE` gives the compiler more flexibility when placing memory functions into TriMatrix memory.

Figure 2–16. Mixed-Port Read-During-Write: OLD_DATA

For mixed-port read-during-write operation of the same address location of a M-RAM block, the RAM outputs are unknown, as shown in [Figure 2–17](#).

Figure 2–17. Mixed-Port Read-During-Write: DONT_CARE

Mixed-port read-during-write is not supported when two different clocks are used in a dual-port RAM. The output value will be unknown during a mixed-port read-during-write operation.

Conclusion

TriMatrix memory, an enhanced RAM architecture with extremely high memory bandwidth in Stratix and Stratix GX devices, gives advanced control of memory applications with features such as byte enables, parity bit storage, and shift-register mode, as well as mixed-port width support and true dual-port mode.

