15. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Stratix II & Stratix II GX Devices

SII52009-3.3

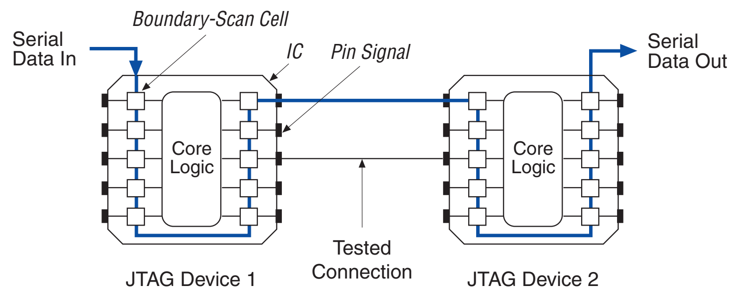
Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (such as; external test probes and "bed-of-nails" test fixture) harder to implement. As a result, cost savings from PCB space reductions increases the cost for traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This Boundary-Scan Test (BST) architecture offers the capability to test efficiently components on PCBs with tight lead spacing.

This BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 15–1 illustrates the concept of BST.

Figure 15–1. IEEE Std. 1149.1 Boundary-Scan Testing



This chapter discusses how to use the IEEE Std. 1149.1 BST circuitry in Stratix® II and Stratix GX devices, including:

- IEEE Std. 1149.1 BST architecture
- IEEE Std. 1149.1 boundary-scan register
- IEEE Std. 1149.1 BST operation control
- I/O Voltage Support in JTAG Chain
- IEEE Std. 1149.1 BST circuitry utilization
- IEEE Std. 1149.1 BST circuitry disabling
- IEEE Std. 1149.1 BST guidelines
- Boundary-Scan Description Language (BSDL) support

In addition to BST, you can use the IEEE Std. 1149.1 controller for Stratix II and Stratix II GX device in-circuit reconfiguration (ICR). However, this chapter only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

For information on configuring Stratix II devices via the IEEE Std. 1149.1 circuitry, refer to the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*, or the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

When configuring via IJAG make sure that Stratix II, Stratix II GX, Stratix, Cyclone™ II, and Cyclone devices are within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix II GX, Stratix, Cyclone II, and Cyclone devices are in the 18th or further position, configuration fails. This does not affect SignalTap® II or boundary-scan testing.

IEEE Std. 1149.1 BST Architecture

A Stratix II and Stratix II GX device operating in IEEE Std. 1149.1 BST mode uses four required pins, `TDI`, `TDO`, `TMS` and `TCK`, and one optional pin, `TRST`. The `TCK` pin has an internal weak pull-down resistor, while the `TDI`, `TMS` and `TRST` pins have weak internal pull-ups. The `TDO` output pin is powered by V_{CCIO} in I/O bank 4. All of the JTAG input pins are powered by the 3.3-V V_{CCPD} supply. All user I/O pins are tri-stated during JTAG configuration.

For recommendations on how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to "I/O Voltage Support in JTAG Chain" on page 15–17.

Table 15–1 summarizes the functions of each of these pins.

Table 15–1. IEEE Std. 1149.1 Pin Descriptions

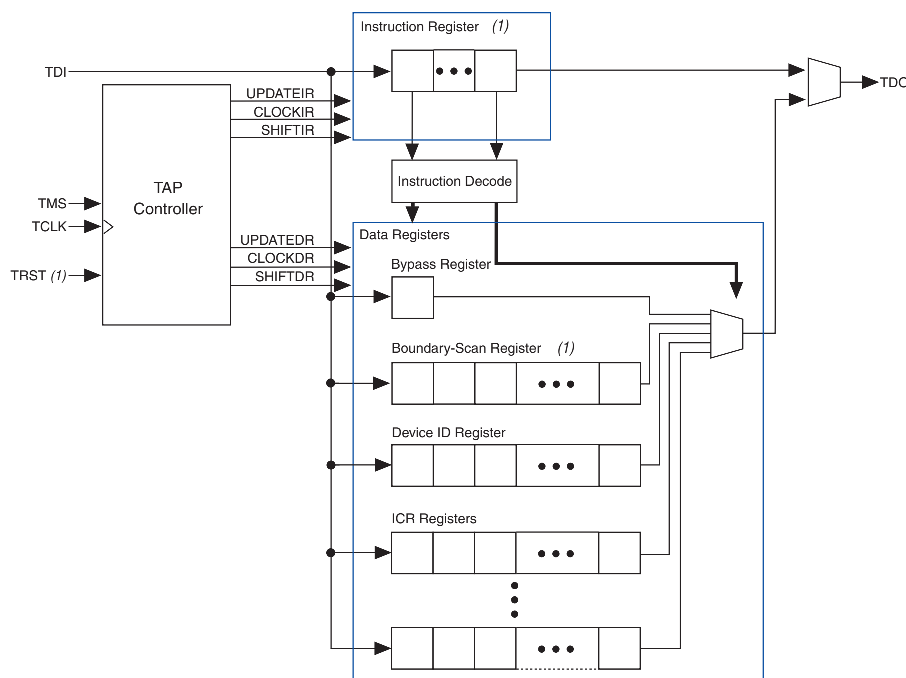
Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the Test Access Port (TAP) controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. This pin should be driven low when not in boundary-scan operation and for non-JTAG users the pin should be permanently tied to GND.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a 1-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

Figure 15–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 15–2. IEEE Std. 1149.1 Circuitry



Note to Figure 15–2:

(1) Refer to the appropriate device data sheet for register lengths.

IEEE Std. 1149.1 boundary-scan testing is controlled by a test access port (TAP) controller. For more information on the TAP controller, refer to "IEEE Std. 1149.1 BST Operation Control" on page 15–7. The TMS and TCK pins operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

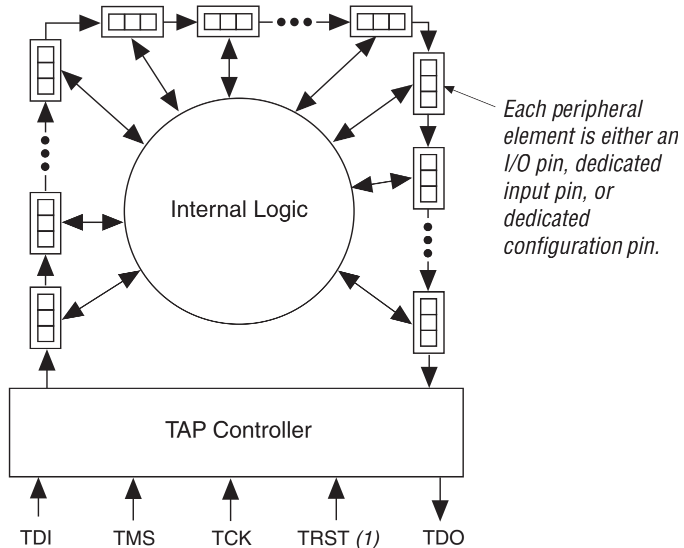
IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with Stratix II or Stratix II GX I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.

Refer to the *Configuration & Testing* chapter in volume 1 of the *Stratix II Device Handbook*, or the *Configuration & Testing* chapter in volume 1 of the *Stratix II GX Device Handbook* for the Stratix II family device boundary-scan register lengths.

Figure 15–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 15–3. Boundary-Scan Register



Boundary-Scan Cells of a Stratix II or Stratix II GX Device I/O Pin

The Stratix II or the Stratix II GX device 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ, OEJ, and PIN_IN signals, while the update registers connect to external data through the PIN_OUT, and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (such as shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 15–4 shows the Stratix II and Stratix II GX device's user I/O boundary-scan cell.

Figure 15–4. Stratix II and Stratix II GX Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry

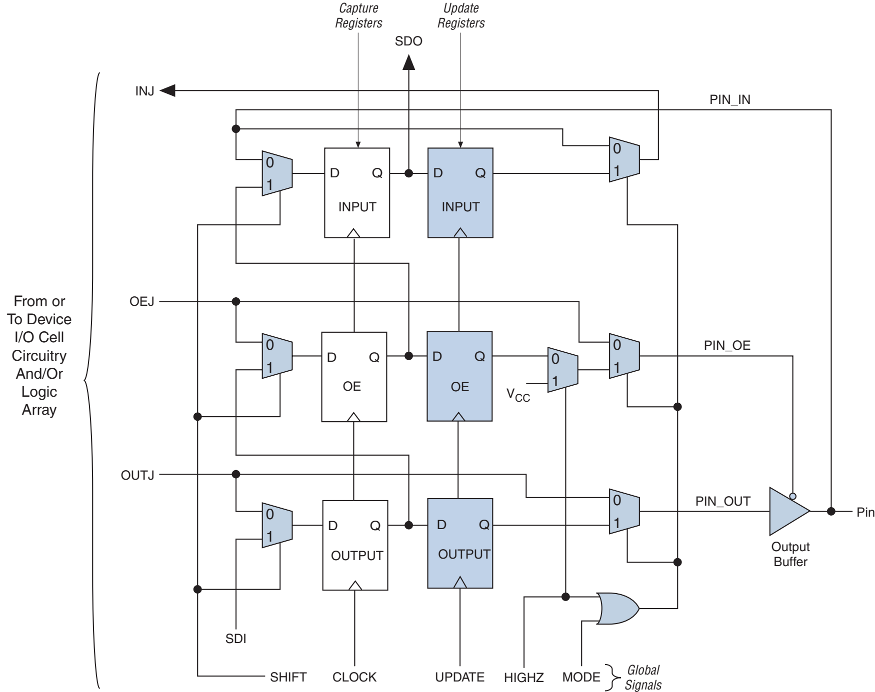


Table 15–2 describes the capture and update register capabilities of all boundary-scan cells within Stratix II and Stratix II GX devices.

Table 15–2. Stratix II and Stratix II GX Device Boundary Scan Cell Descriptions (Part 1 of 2) Note (1)

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	NA
Dedicated clock input	0	1	PIN_IN	N.C. (2)	N.C. (2)	N.C. (2)	PIN_IN drives to clock network or logic array

Table 15–2. Stratix II and Stratix II GX Device Boundary Scan Cell Descriptions (Part 2 of 2) Note (1)

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to control logic
Dedicated bidirectional (open drain) *(4)*	0	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control
Dedicated bidirectional *(5)*	OUTJ	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control and OUTJ drives to output buffer
Dedicated output *(6)*	OUTJ	0	0	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	OUTJ drives to output buffer

Notes to Table 15–2:
(1) TDI, TDO, TMS, TCK, all V_{CC} and GND pin types, VREF, and TEMP_DIODE pins do not have BSCs.
(2) No Connect (N.C.).
(3) This includes pins PLL_ENA, nCONFIG, MSEL0, MSEL1, MSEL2, MSEL3, nCE, VCCSEL, PORSEL, and nIO_PULLUP.
(4) This includes pins CONF_DONE and nSTATUS.
(5) This includes pin DCLK.
(6) This includes pin nCEO.

IEEE Std. 1149.1 BST Operation Control

Stratix II and Stratix II GX devices implement the following IEEE Std. 1149.1 BST instructions:

- SAMPLE/PRELOAD instruction mode is used to take snapshot of the device data without interrupting normal device operations
- EXTEST instruction mode is used to check external pin connections between devices
- BYPASS instruction mode is used when an instruction code consisting of all ones is loaded into the instruction register
- IDCODE instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain
- USERCODE instruction mode is used to examine the user electronic signature within the device along an IEEE Std. 1149.1 chain.

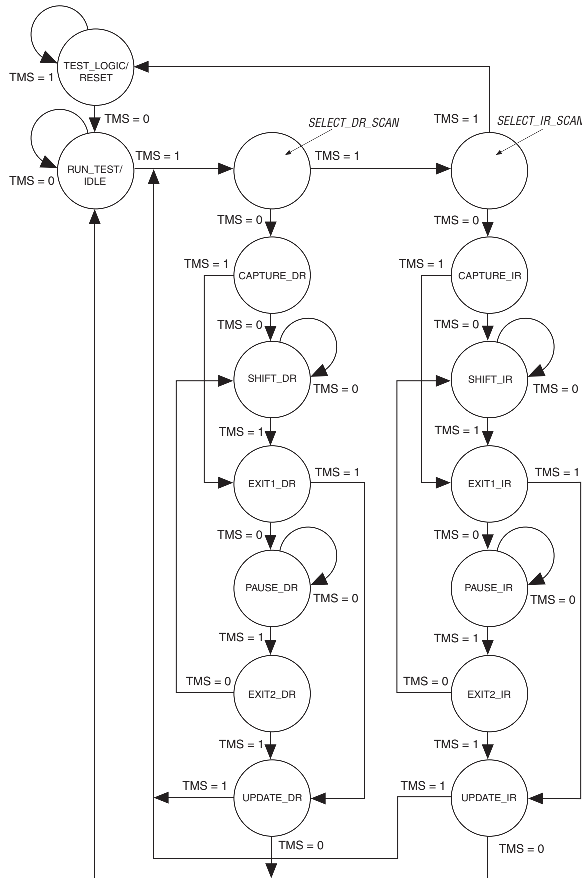
- `CLAMP` instruction mode is used to allow the state of the signals driven from the pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between the TDI and TDO ports
- `HIGHZ` instruction mode sets all of the user I/O pins to an inactive drive state

The BST instruction length is 10 bits. These instructions are described later in this chapter.

For summaries of the BST instructions and their instruction codes, refer to the *Configuration & Testing* chapter in volume 1 of the *Stratix II Device Handbook*, or the *Configuration & Testing* chapter in volume 1 of the *Stratix II GX Device Handbook*.

The IEEE Std. 1149.1 TAP controller, a 16-state state machine clocked on the rising edge of `TCK`, uses the `TMS` pin to control IEEE Std. 1149.1 operation in the device. Figure 15–5 shows the TAP controller state machine.

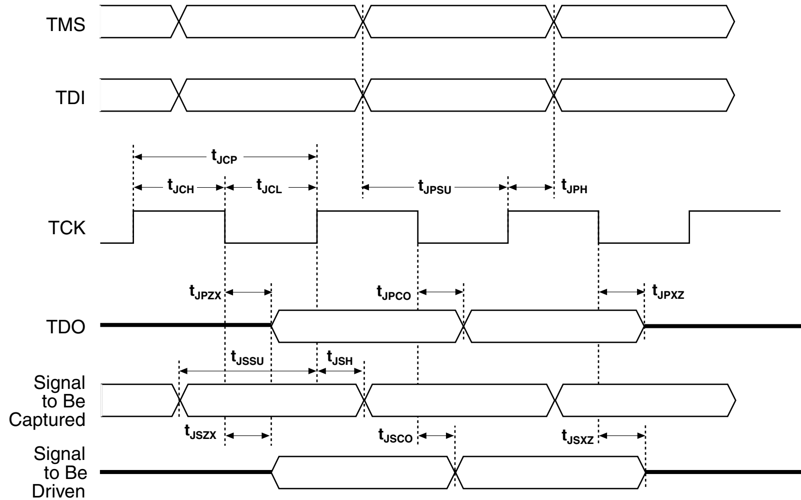
Figure 15–5. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the `TEST_LOGIC/RESET` state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with `IDCODE` as the initial instruction. At device power-up, the TAP controller starts in this `TEST_LOGIC/RESET` state. In addition, forcing the TAP controller to the `TEST_LOGIC/RESET` state is done by holding `TMS` high for five `TCK` clock cycles or by holding the `TRST` pin low. Once in the `TEST_LOGIC/RESET` state, the TAP controller remains in this state as long as `TMS` is held high (while `TCK` is clocked) or `TRST` is held low.

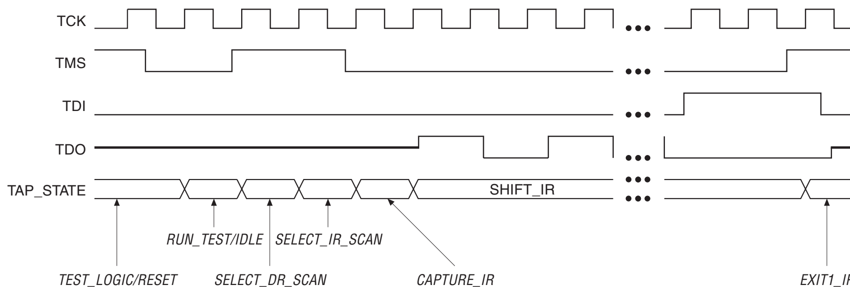
Figure 15–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 15–6. IEEE Std. 1149.1 Timing Waveforms



To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (`SHIFT_IR`) state and shift in the appropriate instruction code on the `TDI` pin. The waveform diagram in Figure 15–7 represents the entry of the instruction code into the instruction register. Figure 15–7 shows the values of `TCK`, `TMS`, `TDI`, `TDO`, and the states of the TAP controller. From the `RESET` state, `TMS` is clocked with the pattern `01100` to advance the TAP controller to `SHIFT_IR`.

Figure 15–7. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code is clocked at the same time that the next state, EXIT1_IR, is activated. Set TMS high to activate the EXIT1_IR state. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of three modes. The three serially shift test data instruction modes are discussed on the following pages:

- "SAMPLE/PRELOAD Instruction Mode" on page 15–11
- "EXTEST Instruction Mode" on page 15–13
- "BYPASS Instruction Mode" on page 15–15

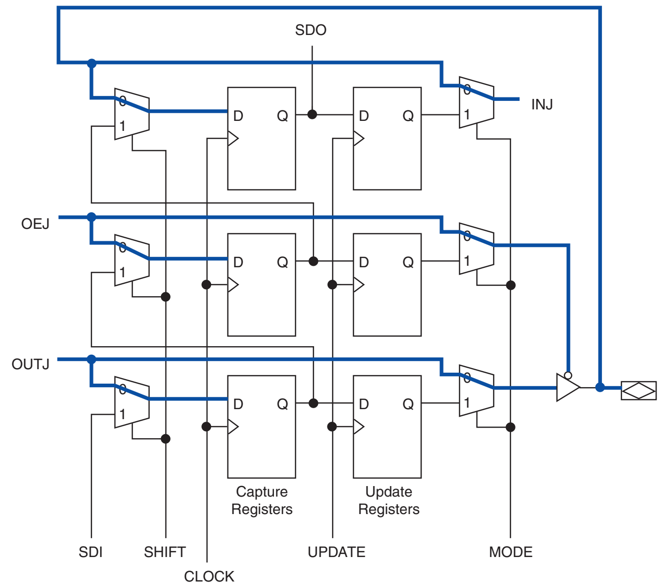
SAMPLE/PRELOAD Instruction Mode

The SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. However, this instruction is most often used to preload the test data into the update registers prior to loading the EXTEST instruction. Figure 15–8 shows the capture, shift, and update phases of the SAMPLE/PRELOAD mode.

Figure 15–8. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode

Capture Phase

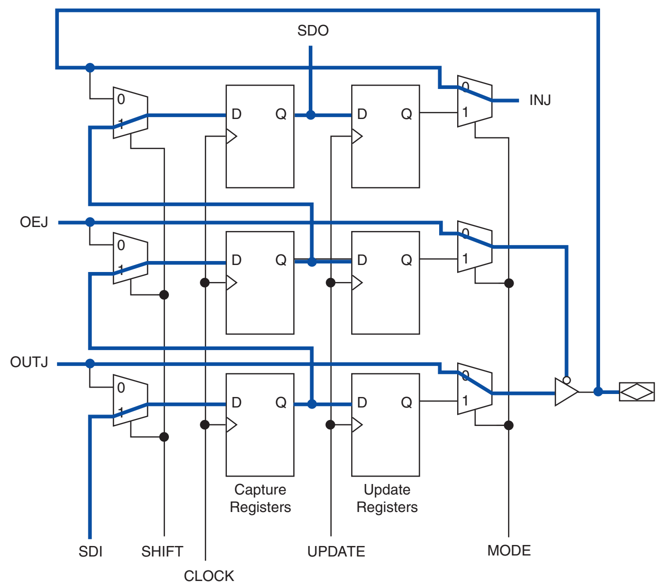
In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals is supplied by the TAP controller's CLOCKDR output. The data retained in these registers consists of signals from normal device operation.



Shift and Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

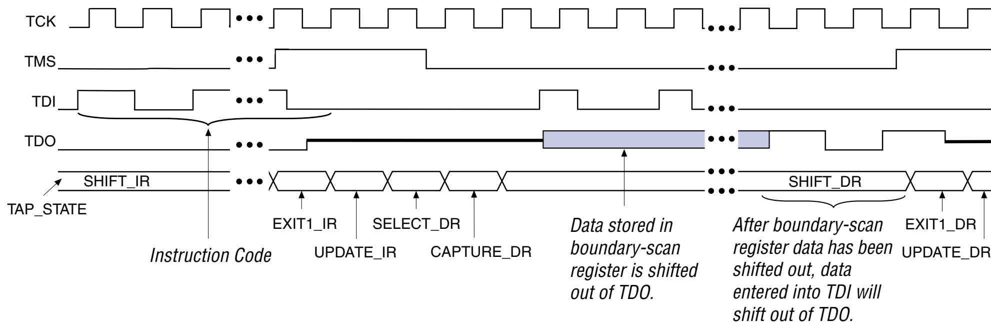
In the update phase, data is transferred from the capture to the UPDATE registers using the UPDATE clock. The data stored in the UPDATE registers can be used for the EXTEST instruction.



During the capture phase, multiplexers preceding the capture registers select the active device data signals. This data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. The device can simultaneously shift new test data into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. Refer to "EXTEST Instruction Mode" on page 15–13 for more information.

Figure 15–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data that was present in the capture registers after the capture phase is shifted out of the TDO pin. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 15–9 shows that the instruction code at TDI does not appear at the TDO pin until after the capture register data is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 15–9. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

The EXTEST instruction mode is used primarily to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

Figure 15–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 15–10. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals is supplied by the TAP controller's CLOCKDR output. Previously retained data in the update registers drive the PIN_IN, INJ, and allows the I/O pin to tri-state or drive a signal out.

A "1" in the OEJ update register tri-states the output buffer.

Shift and Update Phases

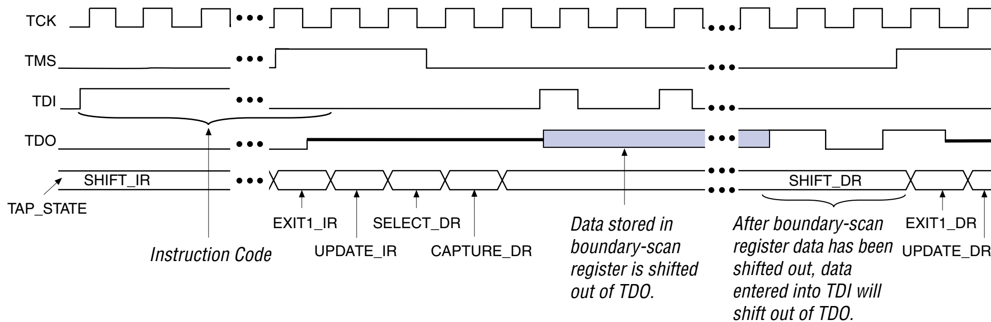
In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The update registers then drive the PIN_IN, INJ, and allow the I/O pin to tri-state or drive a signal out.

EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the output and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data. Thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The EXTEST waveform diagram in Figure 15–11 resembles the SAMPLE/PRELOAD waveform diagram, except for the instruction code. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

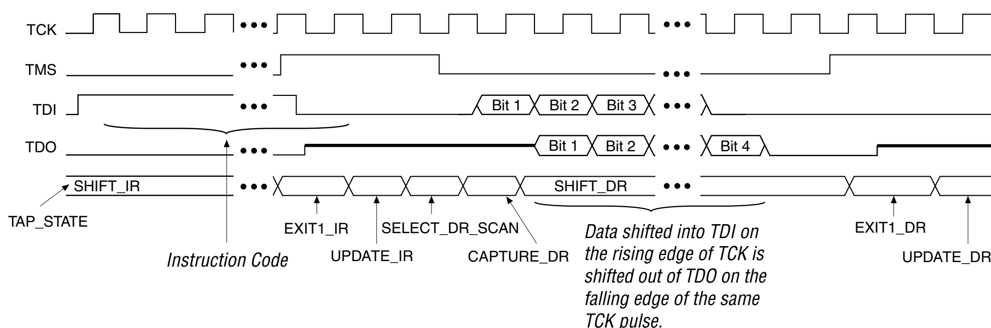
Figure 15–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS mode is activated when an instruction code of all ones is loaded in the instruction register. The waveforms in Figure 15–12 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 15–12. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

The IDCODE instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code. The device ID register is connected between the TDI and TDO ports, and the device IDCODE is shifted out.

For more information on the IDCODE for Stratix II and Stratix II GX devices refer to the *Configuration & Testing* chapter in volume 1 of the *Stratix II Device Handbook*, or the *Configuration & Testing* chapter in volume 1 of the *Stratix II GX Device Handbook.*

USERCODE Instruction Mode

The USERCODE instruction mode is used to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the TDI and TDO ports. The user-defined UES is shifted into the device ID register in parallel from the 32-bit USERCODE register. The UES is then shifted out through the device ID register.

The UES value is not user defined until after the device is configured. Before configuration, the UES value is set to the default value.

CLAMP Instruction Mode

The CLAMP instruction mode is used to allow the state of the signals driven from the pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between the TDI and TDO ports. The state of all signals driven from the pins are completely defined by the data held in the boundary-scan register.

If you are testing after configuring the device, the programmable weak pull-up resister or the bus hold feature overrides the CLAMP value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The HIGHZ instruction mode sets all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the TDI and TDO ports.

If you are testing after configuring the device, the programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin.

I/O Voltage Support in JTAG Chain

The JTAG chain supports several devices. However, you should use caution if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. The TDI pin is powered by V_{CCPD} (3.3 V). For Stratix II and Stratix II GX devices, the V_{CCIO} power supply of bank 4 powers the TDO pin. Table 15–3 shows board design recommendations to ensure proper JTAG chain operation.

You can interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, you should build the JTAG chain in such a way that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter is used only to shift the TDO level to a level acceptable to the JTAG tester. Figure 15–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

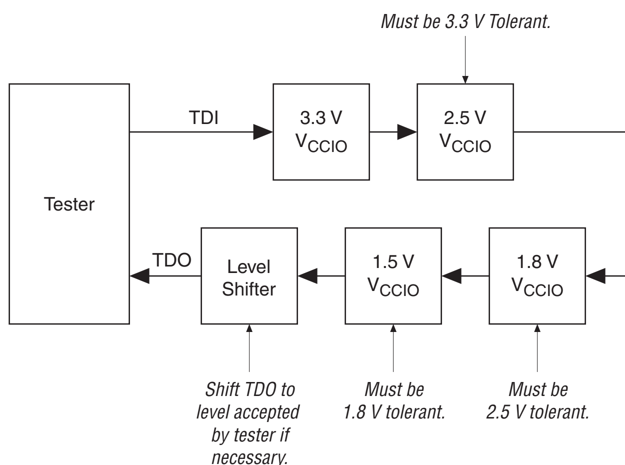
Table 15–3. Supported TDO/TDI Voltage Combinations

Device	TDI Input Buffer Power	Stratix II and Stratix II GX TDO V_{CCIO} Voltage Level in I/O Bank 4			
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V
Stratix II and Stratix II GX	Always V_{CCPD} (3.3V)	✓ (1)	✓ (2)	✓ (3)	level shifter required
Non-Stratix II	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓

Notes to Table 15–3:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

Figure 15–13. JTAG Chain of Mixed Voltages



Using IEEE Std. 1149.1 BST Circuitry

Stratix II and Stratix II GX devices have dedicated JTAG pins and the IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. Not only can you perform BST on Stratix II and Stratix II GX FPGAs before and after, but also during configuration. Stratix II and Stratix II GX FPGAs support the BYPASS, IDCODE and SAMPLE instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the CONFIG_IO instruction.

The CONFIG_IO instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Stratix II or the Stratix II GX FPGA or you can wait for the configuration device to complete configuration. Once configuration is interrupted and JTAG BST is complete, you must reconfigure the part via JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Stratix II and Stratix II GX devices do not affect JTAG boundary-scan or configuration operations. Toggling these pins does not disrupt BST operation (other than the expected BST behavior).

When you design a board for JTAG configuration of Stratix II or Stratix II GX devices, you need to consider the connections for the dedicated configuration pins.

For more information on using the IEEE Std.1149.1 circuitry for device configuration, refer to the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

BST for Configured Devices

For a configured device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. You cannot sample on the configured device output pins with the default BSDL file when the input buffers are turned off. You can set the Quartus II software to always enable the input buffers on a configured device so it behaves the same as an unconfigured device for boundary-scan testing, allowing sample function on output pins in the design. This aspect can cause slight increase in standby current because the unused input buffer is always on. In the Quartus II software, do the following:

1. Choose **Settings** (Assignments menu).

2. Click **Assembler**.

3. Turn on **Always Enable Input Buffers**.

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Stratix II and Stratix II GX devices is enabled upon device power-up. Because the IEEE Std. 1149.1 BST circuitry is used for BST or in-circuit reconfiguration, you must enable the circuitry only at specific times as mentioned in, "Using IEEE Std. 1149.1 BST Circuitry" on page 15–19.

If you are not using the IEEE Std. 1149.1 circuitry in Stratix II or Stratix II GX, then you should permanently disable the circuitry to ensure that you do not inadvertently enable when it is not required.

Table 15–4 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Stratix II and Stratix II GX devices.

Table 15–4. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*	Connection for Disabling
TMS	V_{CC}
TCK	GND
TDI	V_{CC}
TDO	Leave open
TRST	GND

Note to Table 15–4:

(1) There is no software option to disable JTAG in Stratix II or Stratix II GX devices. The JTAG pins are dedicated.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the "10..." pattern does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller did not reach the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.

- Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.

- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when you enter the EXTEST mode. If the OEJ update register contains a 0, the data in the OUTJ update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST testing during ICR. This instruction is supported before or after ICR, but not during ICR. Use the CONFIG_IO instruction to interrupt configuration and then perform testing, or wait for configuration to complete.
- If performing testing before configuration, hold nCONFIG pin low.
- After configuration, any pins in a differential pin pair cannot be tested. Therefore, performing BST after configuration requires editing of BSC group definitions that correspond to these differential pin pairs. The BSC group should be redefined as an internal cell.

Refer to the Boundary-Scan Description Language (BSDL) file for more information on editing.

For more information on boundary scan testing, contact Altera Applications Group.

Boundary-Scan Description Language (BSDL) Support

The Boundary-Scan Description Language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, and failure diagnostics.

For more information, or to receive BSDL files for IEEE Std. 1149.1-compliant Stratix II and Stratix II GX devices, visit the Altera web site at www.altera.com.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Stratix II and Stratix II GX devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. *Boundary-Scan Test: A Practical Approach*. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE Std 1149.1-2001). New York: Institute of Electrical and Electronics Engineers, Inc., 2001.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Referenced Documents

This chapter references the following documents:

- *Configuration & Testing* chapter in volume 1 of the *Stratix II Device Handbook*
- *Configuration & Testing* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *Configuring Stratix II & Stratix II GX Devices chapter in volume 2 of the Stratix II Device Handbook*
- *Configuring Stratix II & Stratix II GX Devices chapter in volume 2 of the Stratix II GX Device Handbook*

Document Revision History

Table 15–5 shows the revision history for this chapter.

Table 15–5. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
October 2007, v3.3	Added "Referenced Documents" section.	—
	Minor text edits.	—
No change	For the *Stratix II GX Device Handbook* only: Formerly chapter 14. The chapter number changed due to the addition of the *Stratix II GX Dynamic Reconfiguration* chapter. No content change.	—
February 2007 v3.2	Added the "Document Revision History" section to this chapter.	—
April 2006, v3.1	Chapter updated as part of the *Stratix II Device Handbook* update.	—

Table 15–5. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
No change	Formerly chapter 13. Chapter number change only due to chapter addition to Section I in February 2006; no content change.	—
October 2005 v3.0	Added chapter to the *Stratix II GX Device Handbook*.	—