Section VII. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Stratix® II GX devices. These chapters contain the required PCB layout guidelines and package specifications.

This section contains the following chapters:

- Chapter 16, Package Information for Stratix II & Stratix II GX Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

16. Package Information for Stratix II & Stratix II GX Devices

SII52010-4.3

Introduction

This chapter provides package information for Altera® Stratix® II and Stratix II GX devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Tables 16–1 and 16–2 show which Altera Stratix II and Stratix II GX devices, respectively, are available in FineLine BGA® (FBGA) packages.

Table 16–1. Stratix II Devices in FBGA Packages

Device	Package	Pins
EP2S15	Flip-chip FBGA	484
	Flip-chip FBGA	672
EP2S30	Flip-chip FBGA	484
	Flip-chip FBGA	672
EP2S60	Flip-chip FBGA	484
	Flip-chip FBGA	672
	Flip-chip FBGA	1,020
EP2S90	Flip-chip FBGA	484
	Flip-chip FBGA	780
	Flip-chip FBGA	1,020
	Flip-chip FBGA	1,508
EP2S130	Flip-chip FBGA	780
	Flip-chip FBGA	1,020
	Flip-chip FBGA	1,508
EP2S180	Flip-chip FBGA	1,020
	Flip-chip FBGA	1,508

Table 16–2. Stratix II GX Devices in FBGA Packages		
Device	**Package**	**Pins**
EP2SGX30	Flip-chip FBGA	780
EP2SGX60	Flip-chip FBGA	780
	Flip-chip FBGA	1,152
EP2SGX90	Flip-chip FBGA	1,152
	Flip-chip FBGA	1,508
EP2SGX130	Flip-chip FBGA	1,508

Thermal Resistance

Thermal resistance values for Stratix II devices are provided for a board that meets JDEC specifications and for a typical board. The following values are provided:

- θ_{JA} (°C/W) still air—Junction-to-ambient thermal resistance with no air flow when a heat sink is not used.
- θ_{JA} (°C/W) 100 ft./min.—Junction-to-ambient thermal resistance with 100 ft./min. airflow when a heat sink is not used.
- θ_{JA} (°C/W) 200 ft./min.—Junction-to-ambient thermal resistance with 200 ft./min. airflow when a heat sink is not used.
- θ_{JA} (°C/W) 400 ft./min.—Junction-to-ambient thermal resistance with 400 ft./min. airflow when a heat sink is not used.
- θ_{JC}—Junction-to-case thermal resistance for device.
- θ_{JB}—Junction-to-board thermal resistance for device.

Tables 16–3 provides θ_{JA} (junction-to-ambient thermal resistance), θ_{JC} (junction-to-case thermal resistance), and θ_{JB} (junction-to-board thermal resistance) values for Stratix II devices on a board meeting JEDEC specifications for thermal resistance calculation. The JEDEC board specifications require two signal and two power/ground planes and are available at **www.jedec.org**.

Table 16–3. Stratix II Device Thermal Resistance for Boards Meeting JEDEC Specifications (Part 1 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S15	484	FBGA	13.1	11.1	9.6	8.3	0.36	4.19
	672	FBGA	12.2	10.2	8.8	7.6	0.36	4.09
EP2S30	484	FBGA	12.6	10.6	9.1	7.9	0.21	3.72
	672	FBGA	11.7	9.7	8.3	7.1	0.21	3.35

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S60	484	FBGA	12.3	10.3	8.8	7.5	0.13	3.38
	672	FBGA	11.4	9.4	7.8	6.7	0.13	2.95
	1,020	FBGA	10.4	8.4	7.0	5.9	0.13	2.67
EP2S90	484	Hybrid FBGA	12.0	9.9	8.3	7.1	0.07	3.73
	780	FBGA	10.8	8.8	7.3	6.1	0.09	2.59
	1,020	FBGA	9.2	8.2	6.8	5.7	0.10	2.41
	1,508	FBGA	9.3	7.4	6.1	5.0	0.10	2.24
EP2S130	780	FBGA	10.1	8.7	7.2	6.0	0.07	2.44
	1,020	FBGA	9.5	8.1	6.7	5.5	0.07	2.24
	1,508	FBGA	8.6	7.3	6.0	4.8	0.07	2.08
EP2S180	1,020	FBGA	9.0	7.9	6.5	5.4	0.05	2.10
	1,508	FBGA	8.1	7.1	5.8	4.7	0.05	1.94

Table 16–3. Stratix II Device Thermal Resistance for Boards Meeting JEDEC Specifications (Part 2 of 2)

Table 16–4 provides θ_{JA} (junction-to-ambient thermal resistance), θ_{JC} (junction-to-case thermal resistance), and θ_{JB} (junction-to-board thermal resistance) values for Stratix II devices on a board with the information shown in Table 16–5.

Table 16–4. Stratix II Device Thermal Resistance for Typical Board (Part 1 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S15	484	FBGA	12.6	9.9	8.1	6.7	0.36	2.48
	672	FBGA	11.4	8.8	7.2	5.9	0.36	2.41
EP2S30	484	FBGA	12.3	9.6	7.8	6.4	0.21	2.02
	672	FBGA	11.1	8.5	6.9	5.6	0.21	1.95
EP2S60	484	FBGA	12.1	9.4	7.6	6.3	0.13	1.74
	672	FBGA	10.9	8.3	6.6	5.4	0.13	1.56
	1,020	FBGA	9.6	7.1	5.6	4.5	0.13	1.33
EP2S90	484	Hybrid FBGA	11.2	8.9	7.2	5.9	0.07	2.48
	780	FBGA	10.0	7.6	6.1	4.9	0.09	1.22
	1,020	FBGA	9.2	6.9	5.5	4.4	0.10	1.16
	1,508	FBGA	8.2	6.0	4.7	3.7	0.10	1.15

Table 16–4. Stratix II Device Thermal Resistance for Typical Board (Part 2 of 2)								
Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S130	780	FBGA	9.3	7.5	6.0	4.8	0.07	1.12
	1,020	FBGA	8.5	6.8	5.3	4.2	0.07	1.03
	1,508	FBGA	7.5	5.8	4.6	3.6	0.07	1.02
EP2S180	1,020	FBGA	8.0	6.7	5.3	4.2	0.05	0.93
	1,508	FBGA	7.1	5.7	4.5	3.5	0.05	0.91

Table 16–5. Board Specifications *Notes (1), (2)*				
Pin Count	Package	Signal Layers	Power/Ground Layers	Size (mm)
1,508	FBGA	12	12	100 × 100
1,020	FBGA	10	10	93 × 93
780	FBGA	9	9	89 × 89
672	FBGA	8	8	87 × 87
484	FBGA	7	7	83 × 83

Notes to Table 16–5:

(1) Power layer Cu thickness 35 um, Cu 90%.

(2) Signal layer Cu thickness 17 um, Cu 15%.

Table 16–6 provides θ_{JA} (junction-to-ambient thermal resistance) and θ_{JC} (junction-to-case thermal resistance) values for Stratix II devices.

Table 16–6. Stratix II GX Device Thermal Resistance							
Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)
EP2SGX30	780	FBGA	11.1	8.6	7.2	6.0	0.24
EP2SGX60	780	FBGA	10.9	8.4	6.9	5.8	0.15
	1,152	FBGA	9.9	7.5	6.1	5.0	0.15
EP2SGX90	1,152	FBGA	9.6	7.3	5.9	4.9	0.11
	1,508	FBGA	9.0	6.7	5.4	4.4	0.11
EP2SGX130	1,508	FBGA	8.3	6.6	5.3	4.3	0.10

Package Outlines

The package outlines are listed in order of ascending pin count. Altera package outlines meet the requirements of *JEDEC Publication No. 95.*

484-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 16–7 and 16–8 show the package information and package outline figure references, respectively, for the 484-pin FBGA packaging.

Table 16–7. 484-Pin FBGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAJ-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	5.8 g
Moisture sensitivity level	Printed on moisture barrier bag

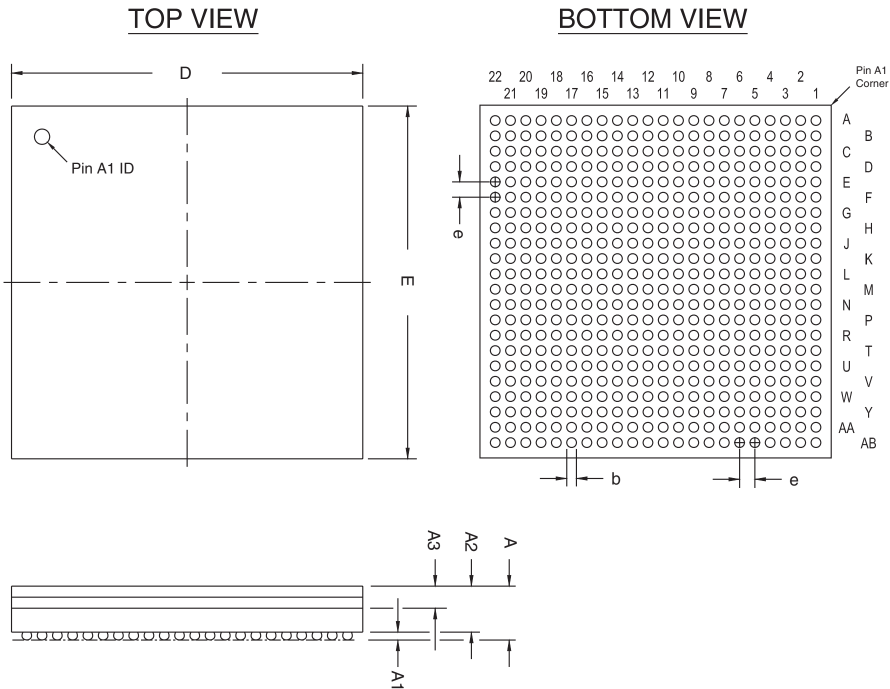
Table 16–8. 484-Pin FBGA Package Outline Dimensions (Part 1 of 2)

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	23.00 BSC		
E	23.00 BSC		

Table 16–8. 484-Pin FBGA Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 16–1 shows a package outline for the 484-pin FineLine BGA packaging.

Figure 16–1. 484-Pin FBGA Package Outline



672-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 16–9 and 16–10 show the package information and package outline figure references, respectively, for the 672-pin FBGA packaging.

Table 16–9. 672-Pin FBGA Package Information

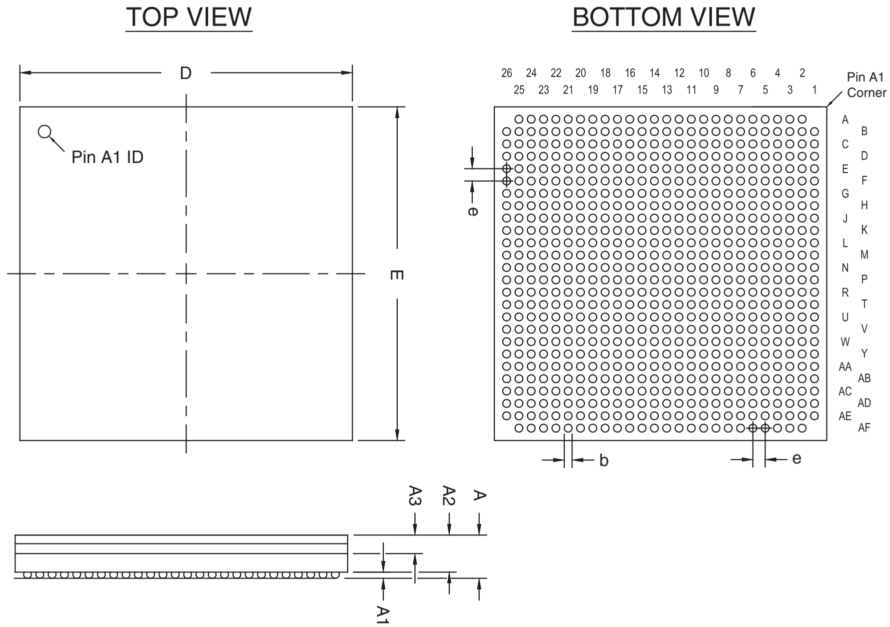
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAL-1
Maximum Lead coplanarity	0.008 inches (0.20 mm)
Weight	7.7 g
Moisture Sensitivity level	Printed on moisture barrier bag

Table 16–10. 672-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	27.00 BSC		
E	27.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 16–2 shows a package outline for the 672-pin FineLine BGA packaging.

Figure 16–2. 672-Pin FBGA Package Outline



780-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 16–11 and 16–12 show the package information and package outline figure references, respectively, for the 780-pin FBGA packaging.

Table 16–11. 780-Pin FBGA Package Information

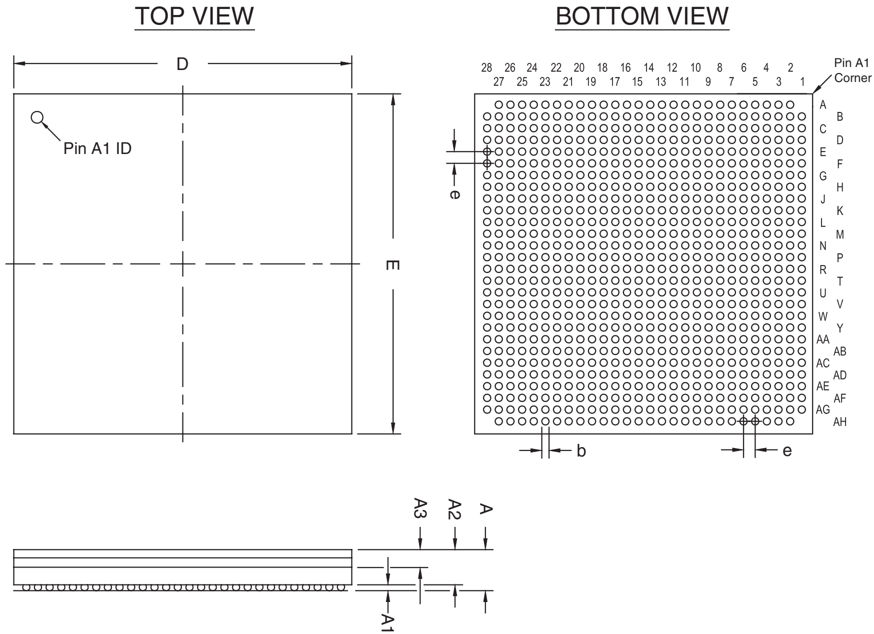
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAM-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	8.9 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 16–12. 780-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	29.00 BSC		
E	29.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 16–3 shows a package outline for the 780-pin FineLine BGA packaging.

Figure 16–3. 780-Pin FBGA Package Outline



1,020-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 16–13 and 16–14 show the package information and package outline figure references, respectively, for the 1,020-pin FBGA packaging.

Table 16–13. 1,020-Pin FBGA Package Information

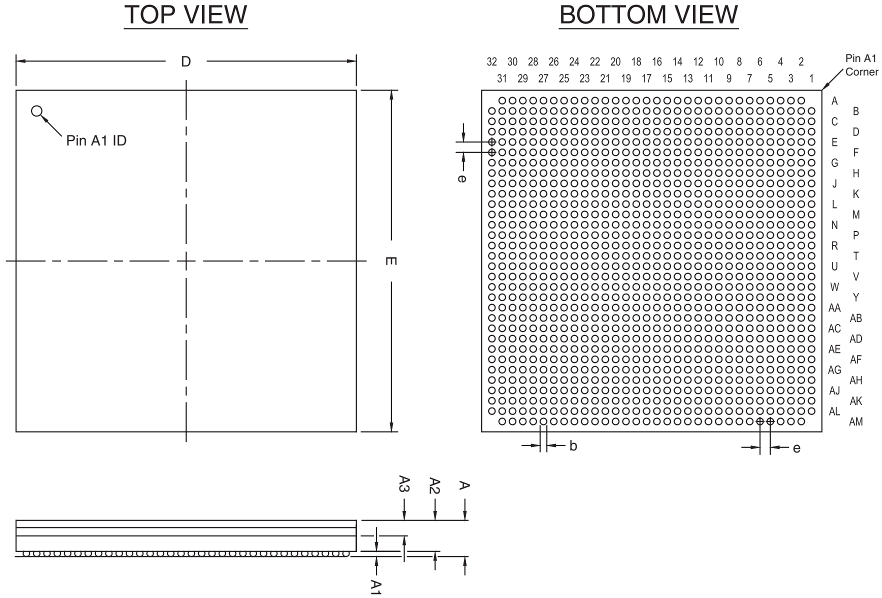
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAP-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	11.5 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 16–14. 1,020-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	33.00 BSC		
E	33.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 16–4 shows a package outline for the 1,020-pin FineLine BGA packaging.

Figure 16–4. 1,020-Pin FBGA Package Outline



1,152-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 16–15 and 16–16 show the package information and package outline figure references, respectively, for the 1,152-pin FBGA packaging.

Table 16–15. 1,152-Pin FBGA Package Information

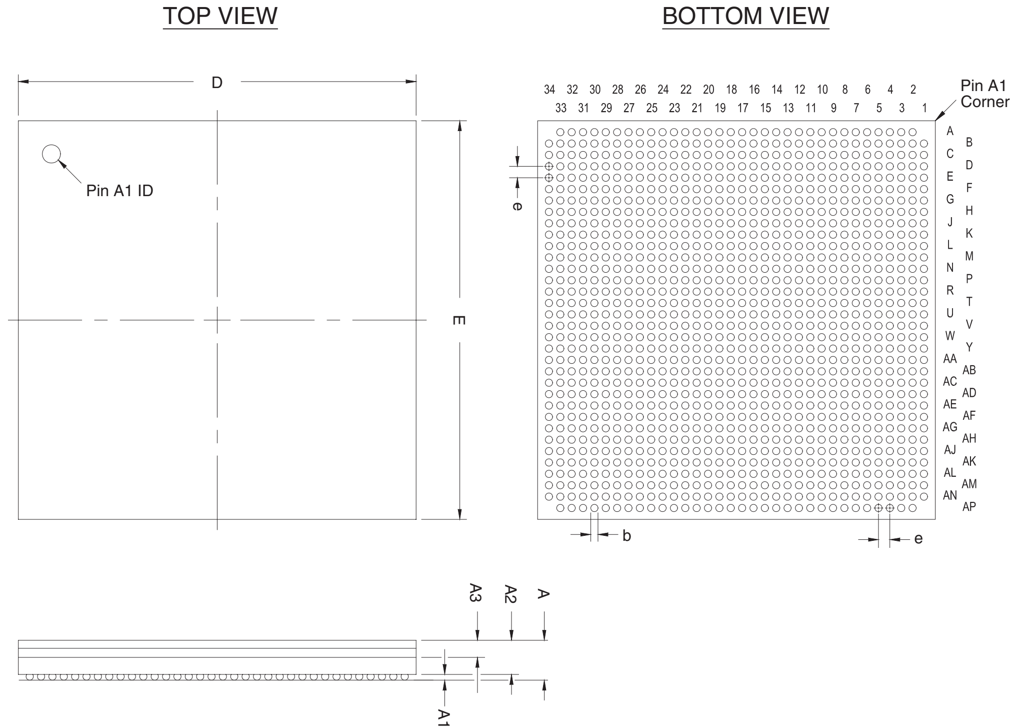
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAR-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	12.0 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 16–16. 1,152-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	35.00 BSC		
E	35.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 16–5 shows a package outline for the 1,152-pin FineLine BGA packaging.

Figure 16–5. 1,152-Pin FBGA Package Outline



1,508-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 16–17 and 16–18 show the package information and package outline figure references, respectively, for the 1,508-pin FBGA packaging.

Table 16–17. 1,508-Pin FBGA Package Information

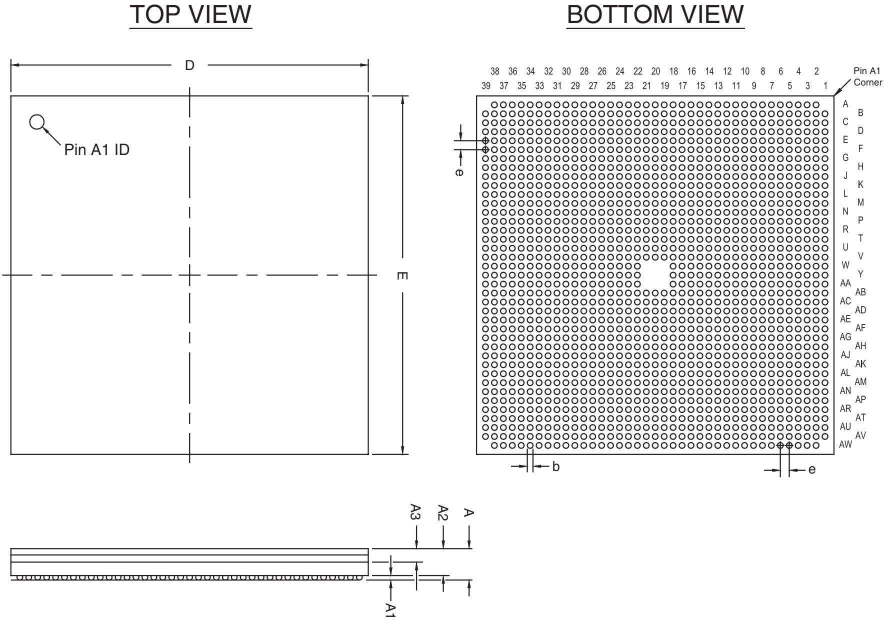
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 Variation: AAU-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	14.6 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 16–18. 1,508-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	40.00 BSC		
E	40.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 16–6 shows a package outline for the 1,508-pin FineLine BGA packaging.

Figure 16–6. 1,508-Pin FBGA Package Outline



Document Revision History

Table 16–19 shows the revision history for this chapter.

Table 16–19. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
No change	For the *Stratix II GX Device Handbook* only: Formerly chapter 15. The chapter number changed due to the addition of the *Stratix II GX Dynamic Reconfiguration* chapter. No content change.	—
May 2007, v4.3	Minor change to Table 16–3.	—
February 2007 v4.2	Added the "Document Revision History" section to this chapter.	—
No change	Formerly chapter 14. Chapter number change only due to chapter addition to Section I in February 2006; no content change.	—
December 2005, v4.1	Chapter updated as part of the *Stratix II Device Handbook* update.	—
October 2005 v4.0	Added chapter to the *Stratix II GX Device Handbook*.	—