

Introduction

The Stratix® III device family offers up to 1.6-Gbps differential I/O capabilities to support source-synchronous communication protocols such as Utopia, Rapid I/O™, XSBI, SGMII, SFI, and SPI.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog PLLs (located on left and right sides of the device)

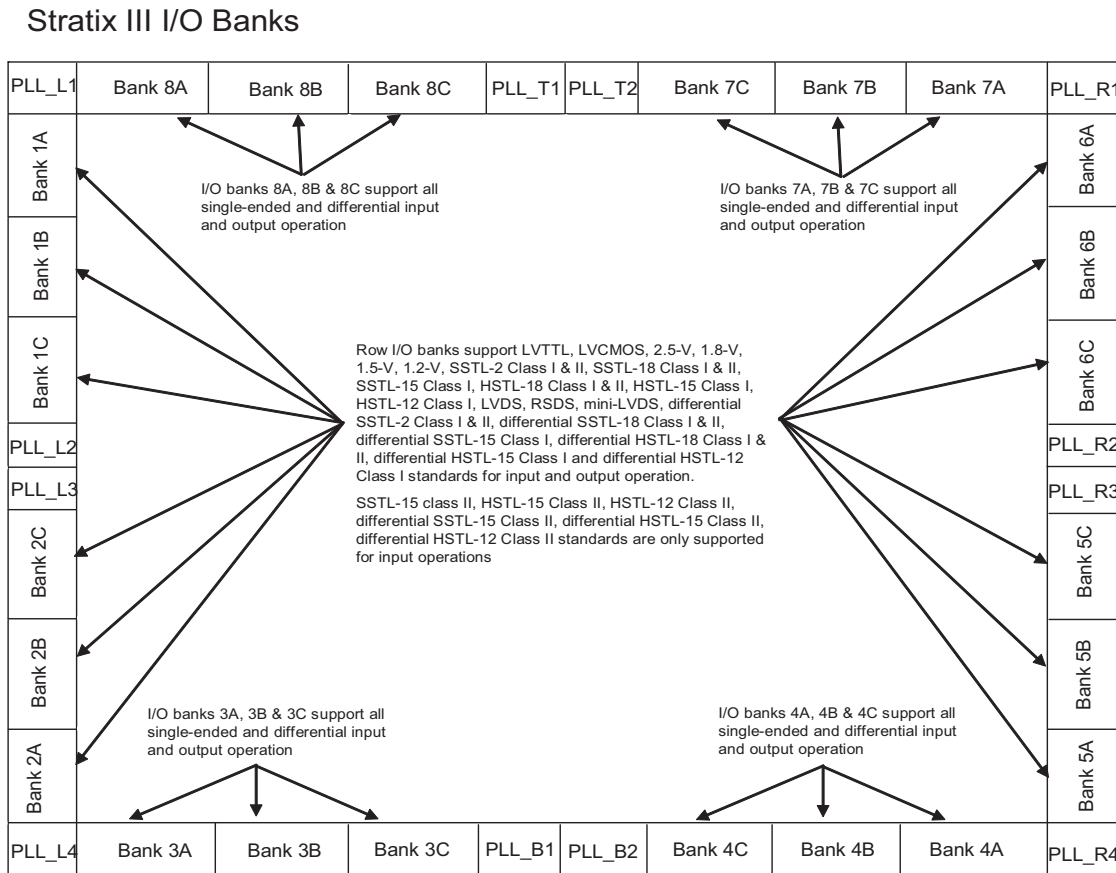
For high-speed differential interfaces, Stratix III devices support the following differential I/O standards:

- Low voltage differential signaling (LVDS)
- Mini-LVDS
- Reduced swing differential signaling (RSDS)
- HSTL
- SSTL

HSTL and SSTL I/O standards can be used only for PLL clock inputs and outputs in differential mode.

I/O Banks

The Stratix III I/Os are divided into 16 to 24 I/O banks. The dedicated circuitry that supports high-speed differential I/Os is located in banks in the right side and left side of the device. [Figure 9-1](#) shows the different banks and the I/O standards supported by the banks.

Figure 9-1. I/O Banks in Stratix III (Note 1), (2), (3), (4), (5), (6)**Notes to Figure 9-1:**

- (1) Figure 9-1 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only. Refer to the pin list and Quartus II software for exact locations.
- (2) Differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted to support differential I/O operations.
- (3) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip differential OCT support.
- (4) Column I/O supports LVDS outputs using SE buffers and external resistor networks.
- (5) Row I/O supports PCI/PCI-X without on-chip clamping diodes.
- (6) The PLL blocks are shown for location purposes only and are not considered additional banks. The PLL input and output uses the I/Os in adjacent banks.

LVDS Channels

The Stratix III device supports LVDS on both side I/O banks and column I/O banks. There are true LVDS input and output buffers at side I/O banks. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Table 9-1 shows the LVDS channels supported in Stratix III device side I/O banks.

Table 9-1. LVDS Channels Supported in Stratix III Device Side I/O Banks (Note 1),(2),(3)

Device	484-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA	1780-Pin FineLine BGA
EP3SL50	48Rx/eTx + 48Tx/eTx	56Rx/eTx + 56Tx/eTx	—	—	—
EP3SL70	48Rx/eTx + 48Tx/eTx	56Rx/eTx + 56Tx/eTx	—	—	—
EP3SL110	—	56Rx/eTx + 56Tx/eTx	88Rx/eTx + 88Tx/eTx	—	—
EP3SL150	—	56Rx/eTx + 56Tx/eTx	88Rx/eTx + 88Tx/eTx	—	—
EP3SL200	—	56Rx/eTx + 56Tx/eTx (4)	88Rx/eTx + 88Tx/eTx	112Rx/eTx + 112Tx/eTx	—
EP3SL340	—	—	88Rx/eTx + 88Tx/eTx (5)	112Rx/eTx + 112Tx/eTx	132Rx/eTx + 132Tx/eTx
EP3SE50	48Rx/eTx + 48Tx/eTx	56Rx/eTx + 56Tx/eTx	—	—	—
EP3SE80	—	56Rx/eTx + 56Tx/eTx	88Rx/eTx + 88Tx/eTx	—	—
EP3SE110	—	56Rx/eTx + 56Tx/eTx	88Rx/eTx + 88Tx/eTx	—	—
EP3SE260	—	56Rx/eTx + 56Tx/eTx (4)	88Rx/eTx + 88Tx/eTx	112Rx/eTx + 112Tx/eTx	—

Notes to Table 9-1:

- (1) Rx = true LVDS input buffers.
- (2) Tx = true LVDS output buffers.
- (3) eTx = emulated-LVDS output buffers, either LVDS_E3R or LVDS_E1R.
- (4) The EP3SL200 and EP3SL260 FPGAs are offered in the H780 package, instead of the F780 package.
- (5) The EP3SL340 FPGA is offered in the H1152 package, instead of the F1152 package.

Table 9-2 shows the LVDS channels (Emulated) supported in Stratix III device column I/O banks.

Table 9-2. LVDS Channels (Emulated) Supported in Stratix III Device Column I/O Banks (3),(4)

Device	484-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA	1780-Pin FineLine BGA
EP3SL50	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SL70	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SL110	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SL150	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SL200	—	64Rx/eTx + 64eTx (1)	96Rx/eTx + 96eTx	128Rx/eTx + 128eTx	—
EP3SL340	—	—	96Rx/eTx + 96eTx (2)	128Rx/eTx + 128eTx	144Rx/eTx + 144eTx
EP3SE50	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SE80	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SE110	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SE260	—	64Rx/eTx + 64eTx (1)	96Rx/eTx + 96eTx	128Rx/eTx + 128eTx	—

Notes to Table 9-2:

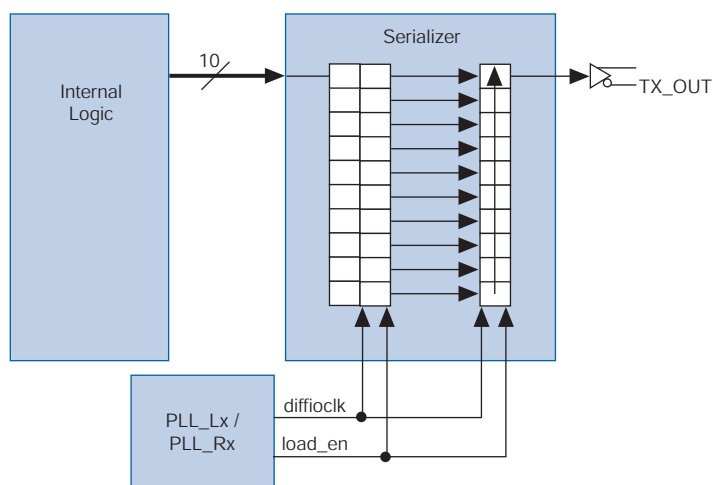
- (1) The EP3SL200 and EP3SE260 FPGAs are offered in the H780 package, instead of the F780 package.
- (2) The EP3SL340 FPGA is offered in the H1152 package, instead of the F1152 package.
- (3) Rx = true LVDS input buffers without on-chip differential input termination.
- (4) eTx = emulated LVDS output buffers, either LVDS_E3R or LVDS_E1R.

Differential Transmitter

The Stratix III transmitter has dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared analog PLL (left/right PLL). The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The serializer takes up to 10-bits wide parallel data from the FPGA core, clocks it into the load registers, and serializes it using shift registers clocked by the left/right PLL before sending the data to the differential buffer. The most significant bit (MSB) of the parallel data is transmitted first.

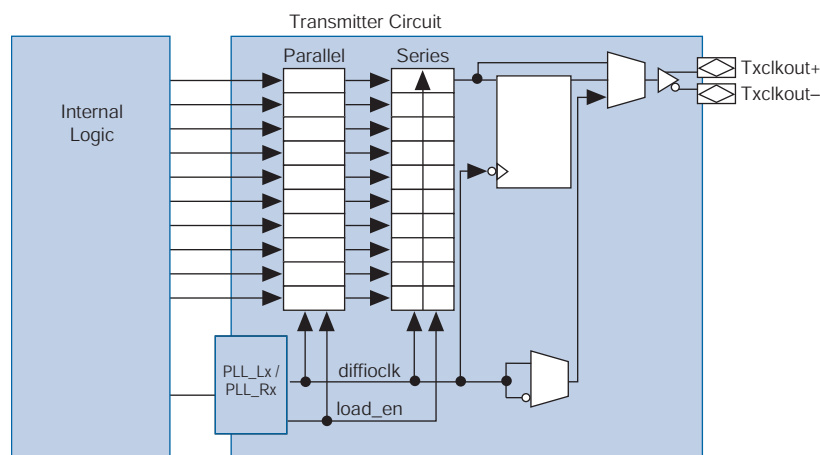
The load and shift registers are clocked by the load enable (`load_en`) signal and the `diffioclck` (clock running at serial data rate) signal generated from PLL_Lx (left PLL) or PLL_Rx (right PLL). The serialization factor can be statically set to $\times 4$, $\times 6$, $\times 7$, $\times 8$, or $\times 10$ using the Quartus® II software. The load enable signal is derived from the serialization factor setting. Figure 9-2 is a block diagram of the Stratix III transmitter.

Figure 9-2. Stratix III Transmitter Block Diagram



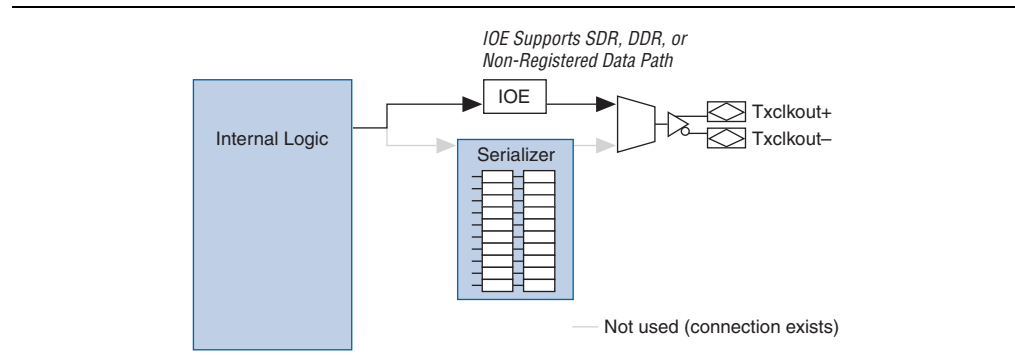
Any Stratix III transmitter data channel can be configured to generate a source synchronous transmitter clock output. This flexibility allows placing the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock-to-data alignments or specific data rate to clock rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 800 MHz. The output clock can also be divided by a factor of 2, 4, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at 0° or 180° (edge or center aligned). The left and right PLLs (PLL_Lx/PLL_Rx) provide additional support for other phase shifts in 45° increments. These settings are made statically in the Quartus II MegaWizard® software. Figure 9-3 shows the Stratix III transmitter in clock output mode.

Figure 9-3. Stratix III Transmitter in Clock Output Mode



The Stratix III serializer can be bypassed to support DDR ($\times 2$) and SDR ($\times 1$) operations to achieve a serialization factor of 2 and 1, respectively. The I/O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left/right PLL (PLL_Lx/PLL_Rx) or from the top/bottom (PLL_Tx/PLL_Bx) PLL. Figure 9-4 shows the serializer bypass path.

Figure 9-4. Stratix III Serializer Bypass



Differential Receiver

The Stratix III device has dedicated circuitry to receive high-speed differential signals. Figure 9-5 shows the block of the Stratix III receiver. The receiver has a differential buffer, a shared PLL_Lx/PLL_Rx, dynamic phase alignment (DPA) block, synchronization FIFO buffer, data realignment block, and a deserializer. The differential buffer can receive LVDS, mini-LVDS, and RSDS signal levels, which are statically set in the Quartus II software assignment editor. The PLL receives the external source clock input that is transmitted with the data and generates different phases of the same clock. The DPA block chooses one of the clocks from the left/right PLL and aligns the incoming data on each channel.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment block. If necessary, the data realignment circuit can insert a single bit of latency in the serial bit stream to align to the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic. The data path in the Stratix III receiver is clocked by either a `dffioclk` signal or the DPA recovered clock. The deserialization factor can be statically set to 4, 6, 7, 8, or 10 by using the Quartus II software. The left/right PLLs (PLL_Lx/PLL_Rx) generate the load enable signal, which is derived from the deserialization factor setting.

The Stratix III deserializer can be bypassed in the Quartus II MegaWizard to support DDR ($\times 2$) or SDR ($\times 1$) operations. The DPA and the data realignment circuit cannot be used when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left/right PLLs or from the top/bottom PLLs.

Figure 9-5. Receiver Block Diagram

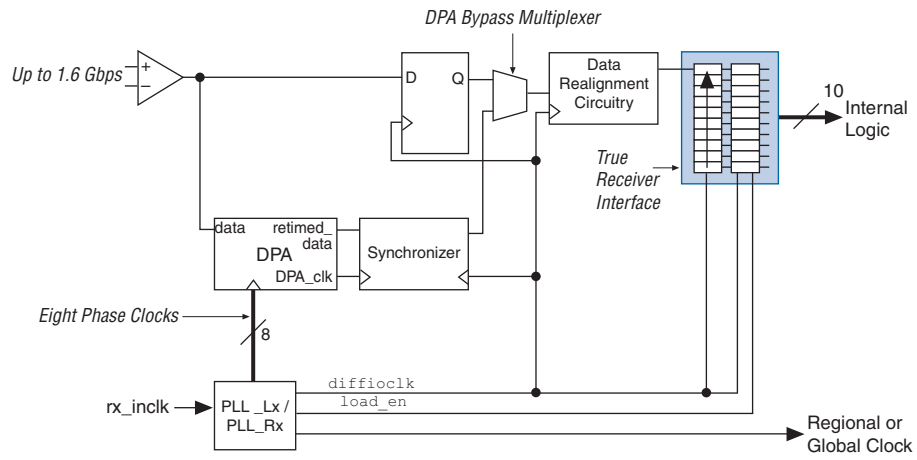
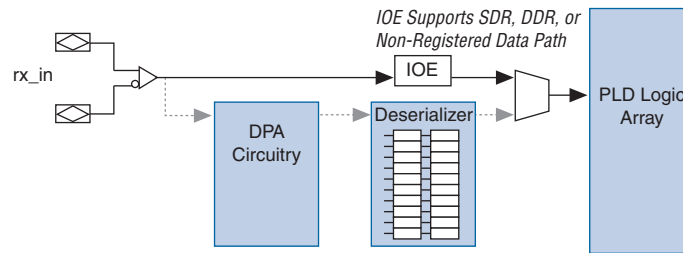


Figure 9-6 shows the deserializer bypass data path.

Figure 9-6. Stratix III Deserializer Bypass



Receiver Data Realignment Circuit (Bit Slip)

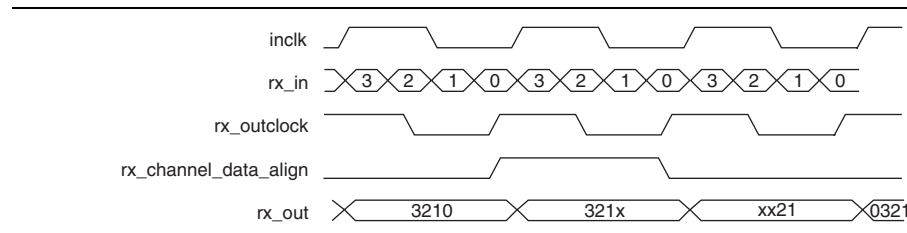
Skew in the transmitted data along with skew added by the link causes channel-to-channel skew on the received serial data streams. If DPA is enabled, the received data is captured with different clock phases on each channel. This may cause the received data to be misaligned from channel to channel. To compensate for this channel-to-channel skew and establish the correct received word boundary at each channel, each receiver channel has a dedicated data realignment circuit that realigns the data by inserting bit latencies into the serial stream.

An optional `RX_CHANNEL_DATA_ALIGN` port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit for every pulse on the `RX_CHANNEL_DATA_ALIGN`. The following are requirements for the `RX_CHANNEL_DATA_ALIGN` signal:

- The minimum pulse width is one period of the parallel clock in the logic array
- The minimum low time between pulses is one period of parallel clock
- There is no maximum high or low time
- Valid data is available two parallel clock cycles after the rising edge of `RX_CHANNEL_DATA_ALIGN`

Figure 9-7 shows receiver output (`RX_OUT`) after one bit slip pulse with the deserialization factor set to 4.

Figure 9-7. Data Realignment Timing

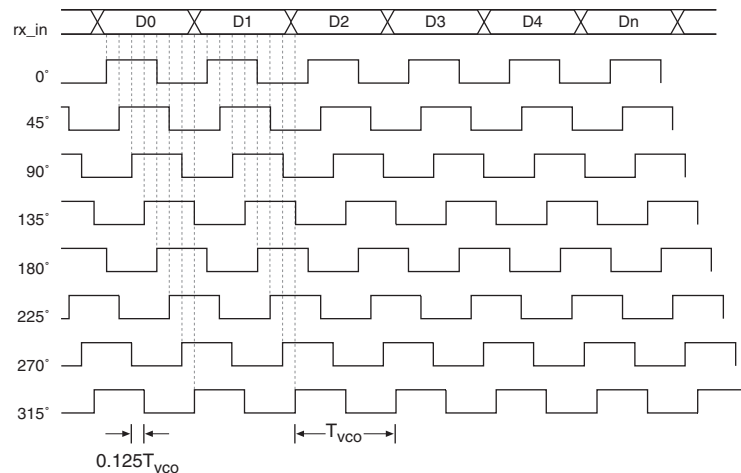


The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times, independent of the deserialization factor. An optional status port, `RX_CDA_MAX`, is available to the FPGA from each channel to indicate when the preset rollover point is reached.

Dynamic Phase Aligner (DPA)


The DPA block takes in high-speed serial data from the differential input buffer and selects one of the eight phase clocks from the left/right PLL to sample the data. The DPA chooses the phase closest to the phase of the serial data. The maximum phase offset between the received data and the selected phase is $1/8$ UI, which is the maximum quantization error of the DPA. The eight phases of the clock are equally divided, giving a 45° resolution. Figure 9-8 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 9-8. DPA Clock Phase to Serial Data Timing Relationship



The DPA block continuously monitors the phase of the incoming serial data and selects a new clock phase if needed. You can prevent the DPA from selecting a new clock phase by asserting the optional `RX_DPLL_HOLD` port, which is available for each channel.

The DPA circuitry does not require a fixed training pattern to lock to the optimum phase out of the 8 phases. After reset or power up, the DPA circuitry requires transitions on the received data to lock to the optimum phase. The `ALTLVDS` megafunction provides an optional output port, `rx_dpa_locked` to indicate if the DPA has locked to the optimum phase. Once the DPA locks to the optimum phase, the `rx_dpa_locked` signal always stays high unless you assert the `rx_reset` signal of the associated LVDS channel or the `p11_areset` signal of the receiver PLL providing the 8 DPA clock phases.

 The `rx_dpa_locked` signal only indicates an initial DPA lock condition to the optimum phase after power up or reset. You must not use the `rx_dpa_locked` signal to validate the integrity of the LVDS link. Use error checkers, for example cyclical redundancy check (CRC) and diagonal interleave parity (DIP4), to validate the integrity of the LVDS link.

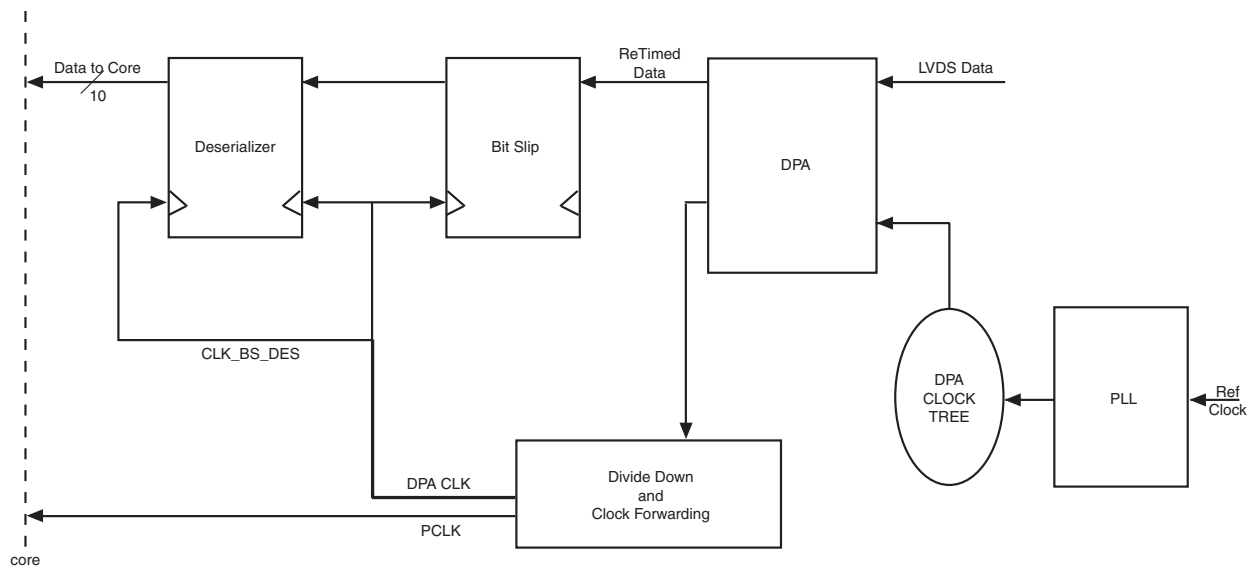
An independent reset port, `RX_RESET`, is available to reset the DPA circuitry. The DPA circuitry must be retrained after reset.

Soft-CDR Mode

The Stratix III LVDS channel offers the soft-CDR mode to support the Gigabit Ethernet/SGMII protocols. Clock-data recovery (CDR) is required to extract the clock out of the clock-embedded data to support SGMII. In Stratix III devices, the CDR circuit is implemented in soft-logic as an IP.

In soft-CDR mode, the DPA circuitry selects an optimal DPA clock phase to sample the data and carry on the bit-slip operation and deserialization. The selected DPA clock is also divided down by the deserialization factor, and then forwarded to the PLD core along with the deserialized data. The LVDS block has an output called DIVCLKOUT (`rx_divfwdclk` port of ALTLVDS megafunction) for the forwarded clock signal. This signal is put on the newly introduced PCLK (periphery clock) network. When using soft-CDR mode, the `rx_reset` port should not be asserted once the `rx_dpa_lock` is asserted because the DPA will continually choose new phase taps from the PLL to track PPM differences between the reference clock and incoming data. In Stratix III, every LVDS channel can be used in soft-CDR mode and can drive the core via the PCLK network. Figure 9-9 shows the path enabled in soft-CDR mode.

Figure 9-9. Soft-CDR Data and Clock Path



Note that the synchronizer FIFO is bypassed in soft-CDR mode. The reference clock frequency must be suitable for the PLL to generate a clock that matches the data rate of the interface. The DPA circuitry can track PPM differences between the reference clock and the data stream.

Synchronizer

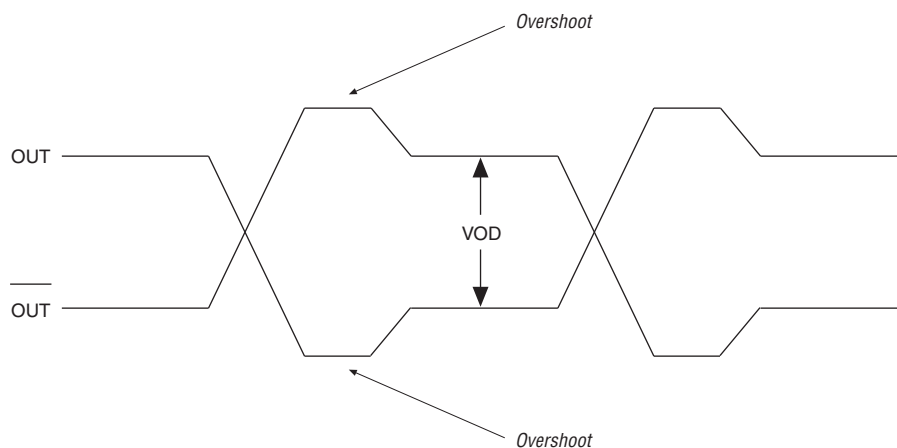
The synchronizer is a 1-bit \times 6-bit deep FIFO buffer that compensates for the phase difference between the recovered clock from the DPA circuit and the `diffioclk` that clocks the rest of the logic in the receiver. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's INCLK.

An optional port, `RX_FIFO_RESET`, is available to the internal logic to reset the synchronizer. Altera® recommends using `RX_FIFO_RESET` to reset the synchronizer once after the `RX_DPA_LOCKED` signal gets asserted and before valid data is received.

Programmable Pre-Emphasis and Programmable VOD

Stratix III LVDS transmitters support programmable pre-emphasis and programmable VOD. Pre-emphasis increases the amplitude of the high frequency component of the output signal, and thus helps compensate for the frequency dependent attenuation along the transmission line. Figure 9-10 illustrates an LVDS output with pre-emphasis. The overshoot is produced by pre-emphasis. This overshoot should not be included in the VOD voltage. The definition of VOD is also shown in Figure 9-10.

Figure 9-10. Programmable VOD



Pre-emphasis is an important feature for high-speed transmission. Without pre-emphasis, the output current is limited by the VOD setting and the output impedance of the driver. At high frequency, the slew rate may not be fast enough to reach the full VOD before the next edge, producing a pattern dependent jitter.

With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate. The overshoot introduced by the extra current happens only during switching and does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis needed depends on the attenuation of the high-frequency component along the transmission line.

Stratix III pre-emphasis is programmable to create the right amount of overshoot at different transmission conditions. There are four settings for pre-emphasis: zero, low, medium, and high. The default setting is low. In the Quartus II assignment editor, pre-emphasis settings are represented in numbers with 0 (zero), 1 (low), 2 (medium) and 3 (high). For a particular design, simulation with an LVDS buffer and transmission line can be used to determine the best pre-emphasis setting.

The VOD is also programmable with four settings: low, medium low, medium high, and high. The default setting is medium low. In the Quartus II assignment editor, programmable VOD settings are represented in numbers with 0 (low), 1 (medium low), 2 (medium high) and 3 (high).

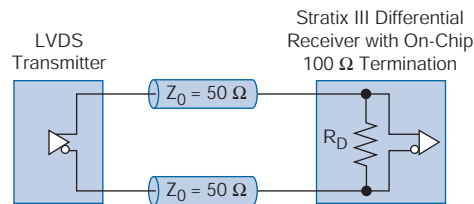
Differential I/O Termination

Stratix III devices provide a 100 Ω , on-chip differential termination option on each differential receiver channel for LVDS standards. On-chip termination saves board space by eliminating the need to add external resistors on the board. You can enable on-chip termination in the Quartus II software Assignment editor.

On-chip differential termination is supported on all row I/O pins and SERDES block clock pins: CLK [0, 2, 9, and 11]. It is not supported for column I/O pins, high speed clock pins CLK [1, 3, 8, 10], or the corner PLL clock inputs.

Figure 9-11 illustrates device on-chip termination.

Figure 9-11. On-Chip Differential I/O Termination



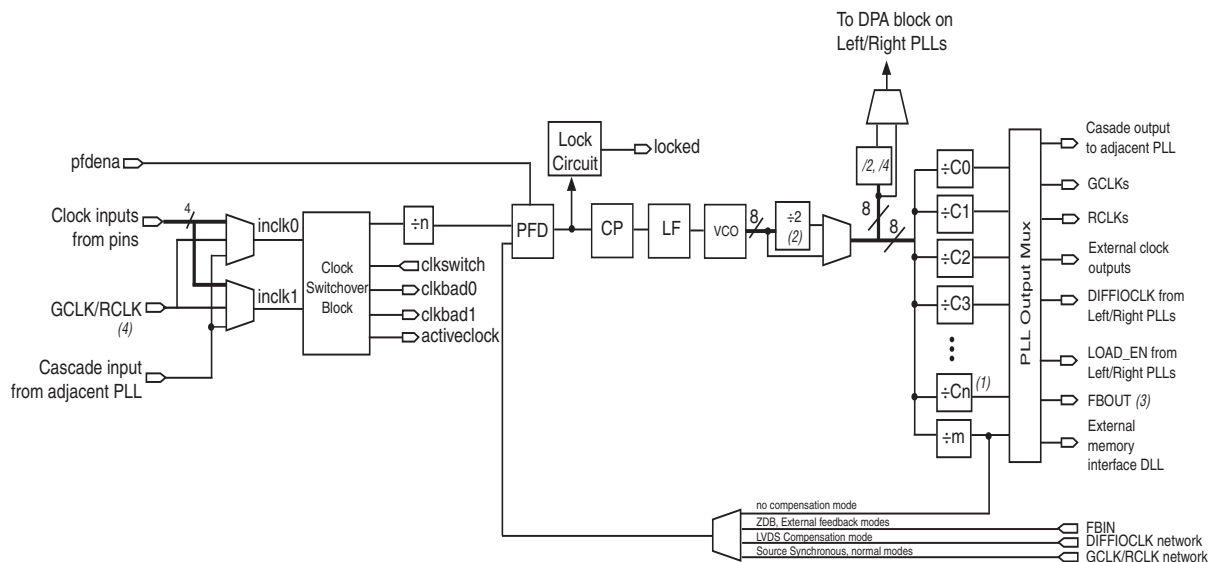
Left/Right PLLs (PLL_Lx/ PLL_Rx)

Stratix III devices contain up to eight left/right PLLs, with up to four PLLs located on the left side and four on the right side of the device. The left PLLs can support high-speed differential I/O banks on the left side and the right PLLs can support banks on the right side of the device. The high-speed differential I/O receiver and transmitter channels use these left/right PLLs to generate the parallel global clocks (rx- or tx-clock) and high-speed clocks (diffioclk). Figure 9-1 shows the locations of the left/right PLLs. The PLL VCO operates at the clock frequency of the data rate. Each left/right PLL offers a single serial data rate support, but up to two separate serialization and/or deserialization factors (from the C0 and C1 left/right PLL clock outputs). Clock switchover and dynamic left/right PLL reconfiguration is available in high-speed differential I/O support mode.

 For more details, refer to the *Clock Network and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Figure 9-12 shows a simplified block diagram of the major components of the Stratix III PLL.

Figure 9-12. PLL Block Diagram

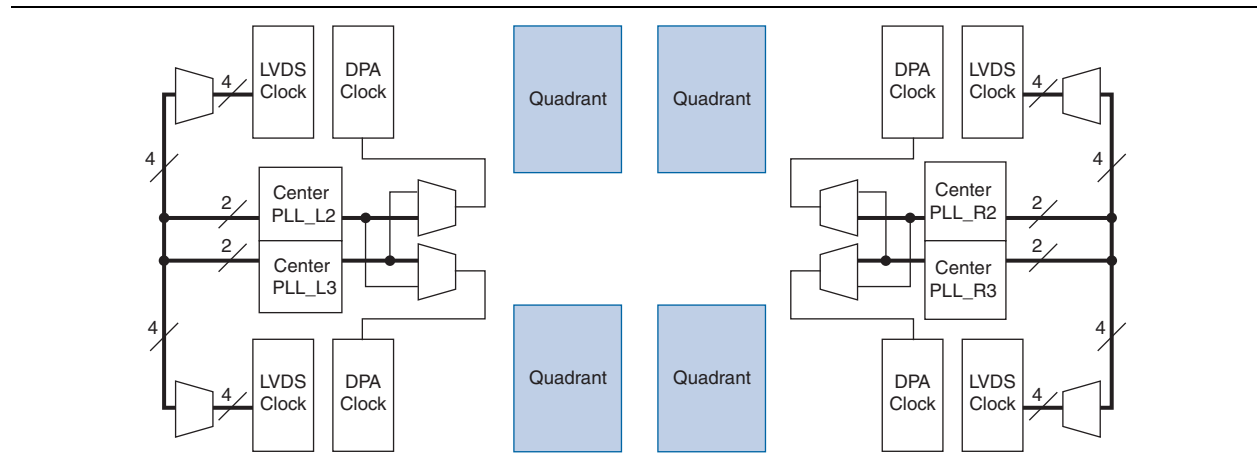
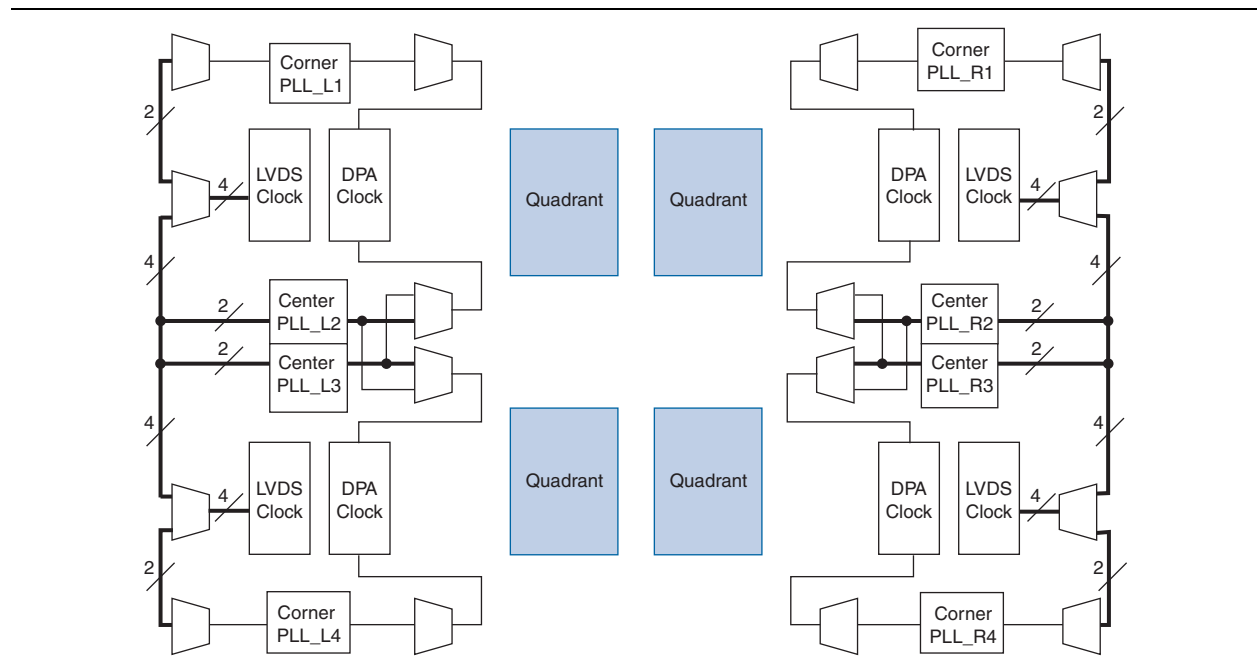


Notes to Figure 9-12:

- (1) $n = 6$ for Left/Right PLLs; $n = 9$ for Top/Bottom PLLs.
- (2) This is the VCO post-scale counter κ .
- (3) The FBOUT port is fed by the M counter in Stratix III PLLs.
- (4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal or general purpose I/O pin cannot drive the PLL.

Clocking

The left/right PLLs feed into the differential transmitter and receive channels through the LVDS and DPA clock network. The center left/right PLLs can clock the transmitter and receive channels above and below them. The corner left/right PLLs can drive I/Os in the banks adjacent to them. Figure 9-13 and Figure 9-14 show center and corner PLL clocking in Stratix III devices. More information on PLL clocking restrictions can be found in “Differential Pin Placement Guidelines” on page 9-18.

Figure 9-13. LVDS/DPA Clocks in Stratix III Devices with Center PLLs**Figure 9-14.** LVDS/DPA Clocks in Stratix III Devices with Center and Corner PLLs

Source-Synchronous Timing Budget

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix III devices. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

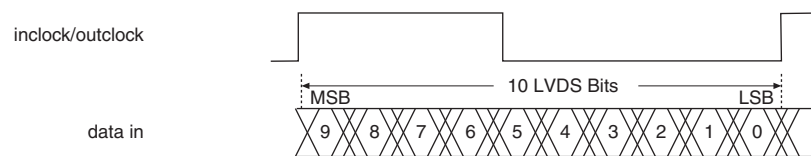
Rather than focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix III devices, and how to use these timing parameters to determine a design's maximum performance.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For an operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock.

Figure 9-15 shows the data bit orientation of the $\times 10$ mode.

Figure 9-15. Bit Orientation in Quartus II Software



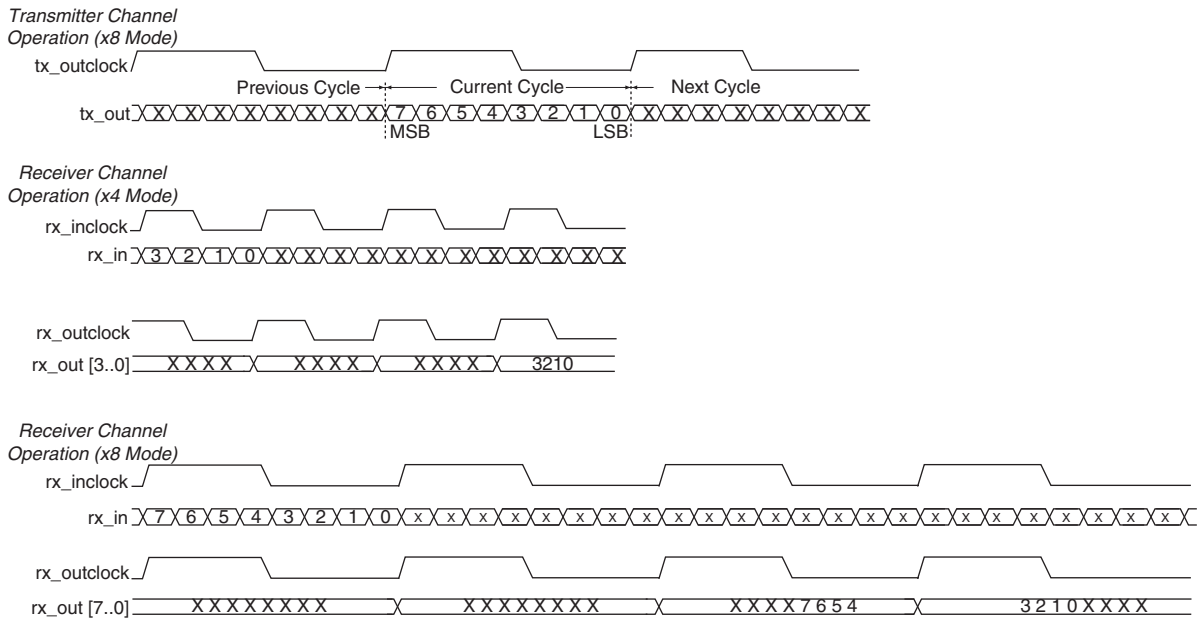
Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 9-16 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools and find the bit position within the word. The bit positions after deserialization are listed in Table 9-3.

Figure 9-16. Bit-Order and Word Boundary for One Differential Channel (Note 1)



Note to Figure 9-16:

(1) These are only functional waveforms and are not intended to convey timing information.

Table 9-3 shows the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 9-3. Differential Bit Naming (Part 1 of 2)

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88
13	103	96
14	111	104
15	119	112

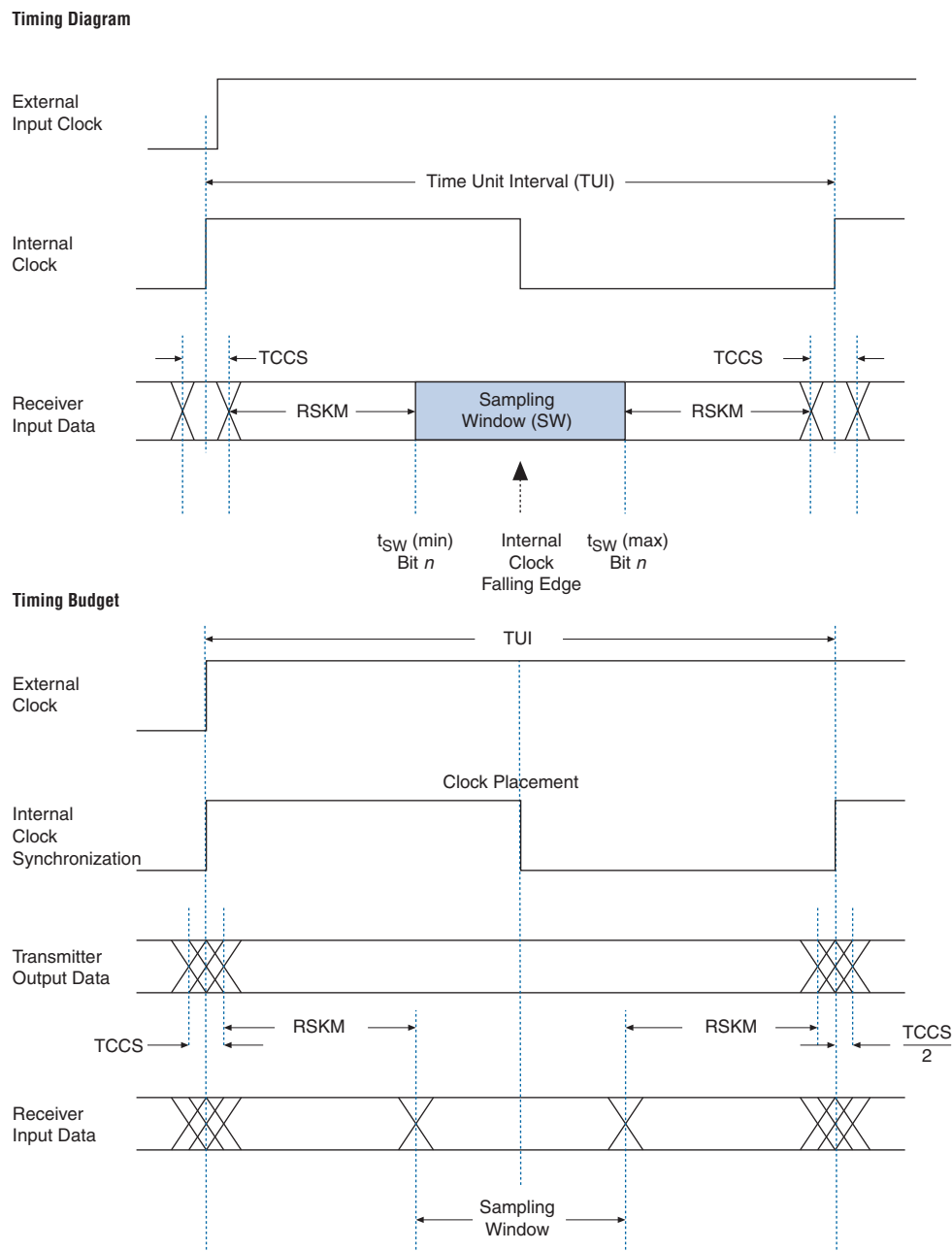
Table 9-3. Differential Bit Naming (Part 2 of 2)

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
16	127	120
17	135	128
18	143	136

Receiver Skew Margin for Non-DPA

Changes in system environment, such as temperature, media (cable, connector, or PCB) loading effect, the receiver's setup and hold times, and internal skew, reduce the sampling window for the receiver. The timing margin between the receiver's clock input and the data input sampling window is called receiver skew margin (RSKM). [Figure 9-17](#) shows the relationship between the RSKM and the receiver's sampling window.

Transmit channel-to-channel skew (TCCS), RSKM, and the sampling window specifications are used for high-speed source-synchronous differential signals without DPA. When using DPA, these specifications are exchanged for the simpler single DPA jitter tolerance specification. For instance, the receiver skew is why each input with DPA selects a different phase of the clock, thus removing the requirement for this margin. In the timing diagram, TSW represents time for the sampling window.

Figure 9-17. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA

Differential Pin Placement Guidelines

To ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and issues an error message if they are not met.

Since DPA usage adds some constraints on the placement of high-speed differential channels, this section is divided into pin placement guidelines with and without DPA usage.

Guidelines for DPA-Enabled Differential Channels

The Stratix III device has differential receivers and transmitters in I/O banks on the left and right sides of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When DPA-enabled channels are used in differential banks, you must adhere to the guidelines listed in the following sections.

DPA-Enabled Channels and Single-Ended I/Os

When there is a DPA channel enabled in a bank, both single-ended I/Os and differential I/O standards are allowed in the bank.

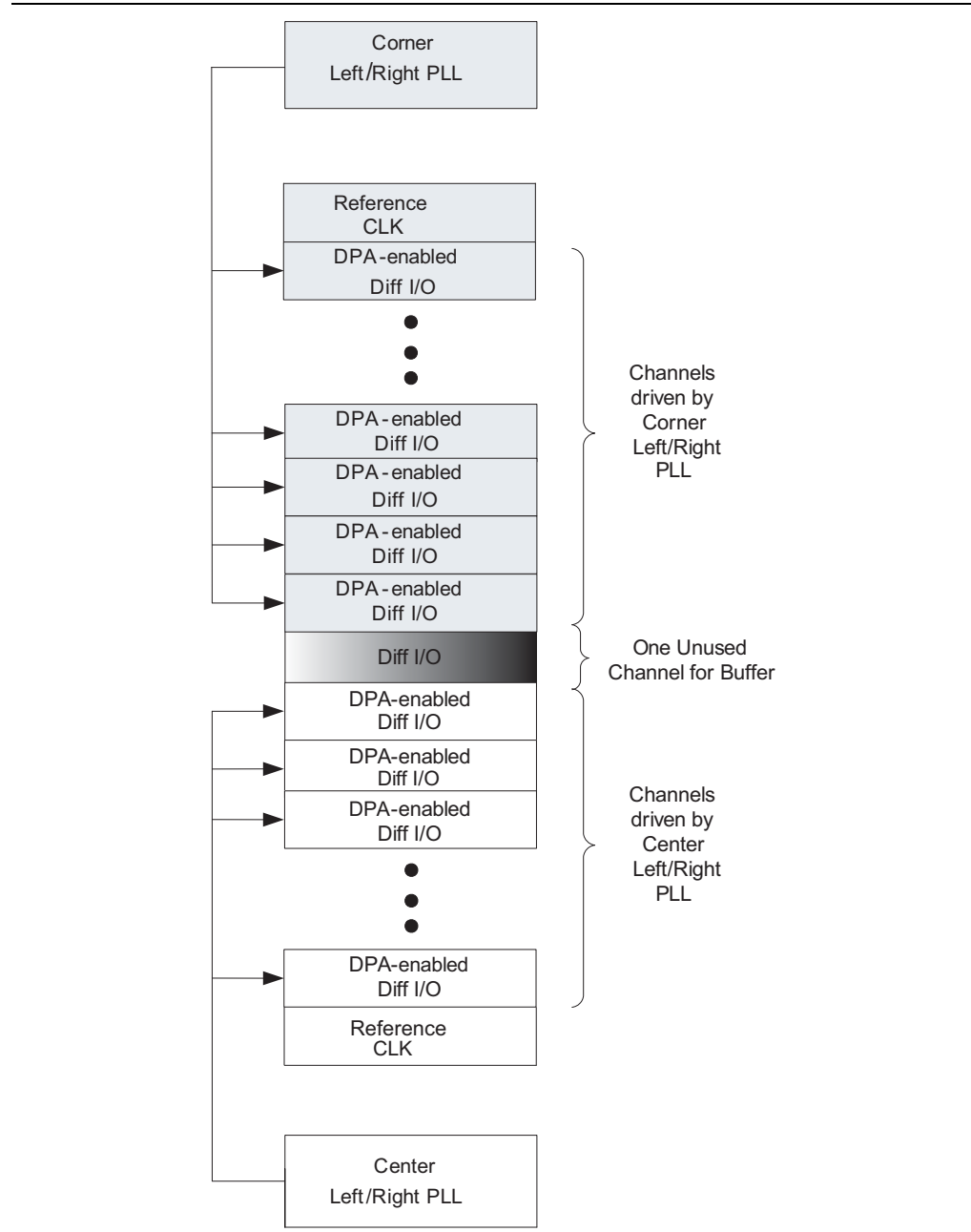
- Single-ended I/Os are allowed in the same I/O bank as long as the single-ended I/O standard uses the same VCCIO as the DPA-enabled differential I/O bank.

DPA-Enabled Channel Driving Distance

- If the number of DPA channels driven by each left/right PLL exceeds 25 LAB rows, Altera recommends implementing data realignment (bit-slip) circuitry for all the DPA channels.

Using Corner and Center Left/Right PLLs

- If a differential bank is being driven by two left/right PLLs, where the corner left/right PLL is driving one group and the center left/right PLL is driving another group, there must be at least one row of separation between the two groups of DPA-enabled channels (see [Figure 9-18](#)). The two groups can operate at independent frequencies.
- No separation is necessary if a single left/right PLL is driving DPA-enabled channels as well as DPA-disabled channels.

Figure 9-18. Corner and Center Left/Right PLLs Driving DPA-Enabled Differential I/Os in the Same Bank**Using Both Center Left/Right PLLs**

- Both center left/right PLLs can be used to drive DPA-enabled channels simultaneously, as long as they drive these channels in their adjacent banks only, as shown in [Figure 9-19](#).
- If one of the center left/right PLLs drive the top and bottom banks, the other center left/right PLL cannot be used to drive the differential channels, as shown in [Figure 9-19](#).

- If the top PLL_L2/PLL_R2 drives DPA-enabled channels in the lower differential bank, the PLL_L3/PLL_R3 cannot drive DPA-enabled channels in the upper differential banks and vice versa. In other words, the center left/right PLLs cannot drive cross-banks simultaneously, as shown in Figure 9-20.

Figure 9-19. Center Left/Right PLLs Driving DPA-Enabled Differential I/Os

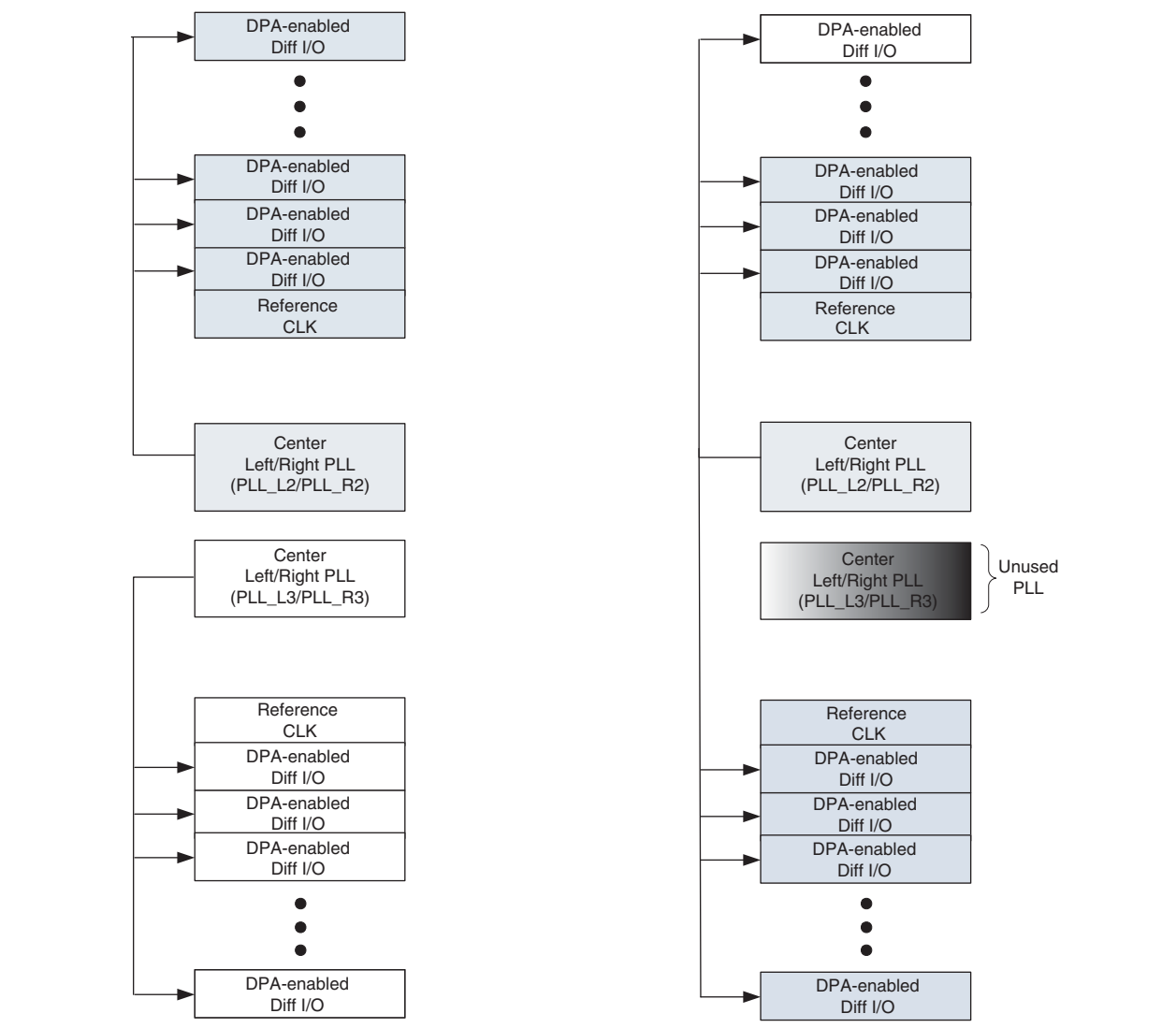
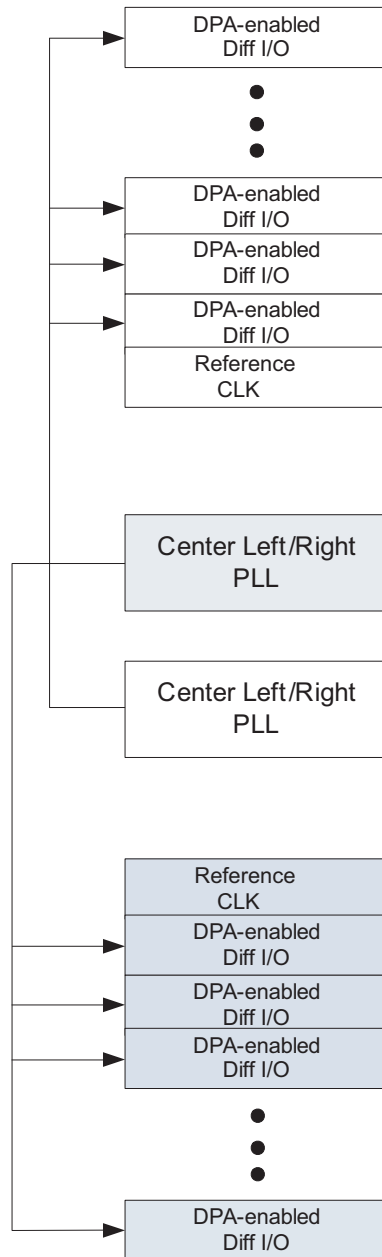


Figure 9-20. Invalid Placement of DPA-Enabled Differential I/Os Driven by Both Center Left/Right PLLs



Guidelines for DPA-Disabled Differential Channels

When DPA-disabled channels are used in the left and right banks of a Stratix III device, you must adhere to the guidelines in the following sections.

DPA-Disabled Channels and Single-Ended I/Os

The placement rules for DPA-disabled channels and single-ended I/Os are the same as those for DPA-enabled channels and single-ended I/Os.

DPA-Disabled Channel Driving Distance

Each left/right PLL can drive all the DPA-disabled channels in the entire bank.

Using Corner and Center Left/Right PLLs

- A corner left/right PLL can be used to drive all transmitter channels and a center left/right PLL can be used to drive all DPA-disabled receiver channels within the same differential bank. In other words, a transmitter channel and a receiver channel in the same LAB row can be driven by two different PLLs, as shown in [Figure 9-21](#).
- A corner left/right PLL and a center left/right PLL can drive duplex channels in the same differential bank as long as the channels driven by each PLL are not interleaved. No separation is necessary between the group of channels driven by the corner and center left/right PLLs. See [Figure 9-21](#) and [Figure 9-22](#).

Figure 9-21. Corner and Center Left/Right PLLs Driving DPA-Disabled Differential I/Os in the Same Bank

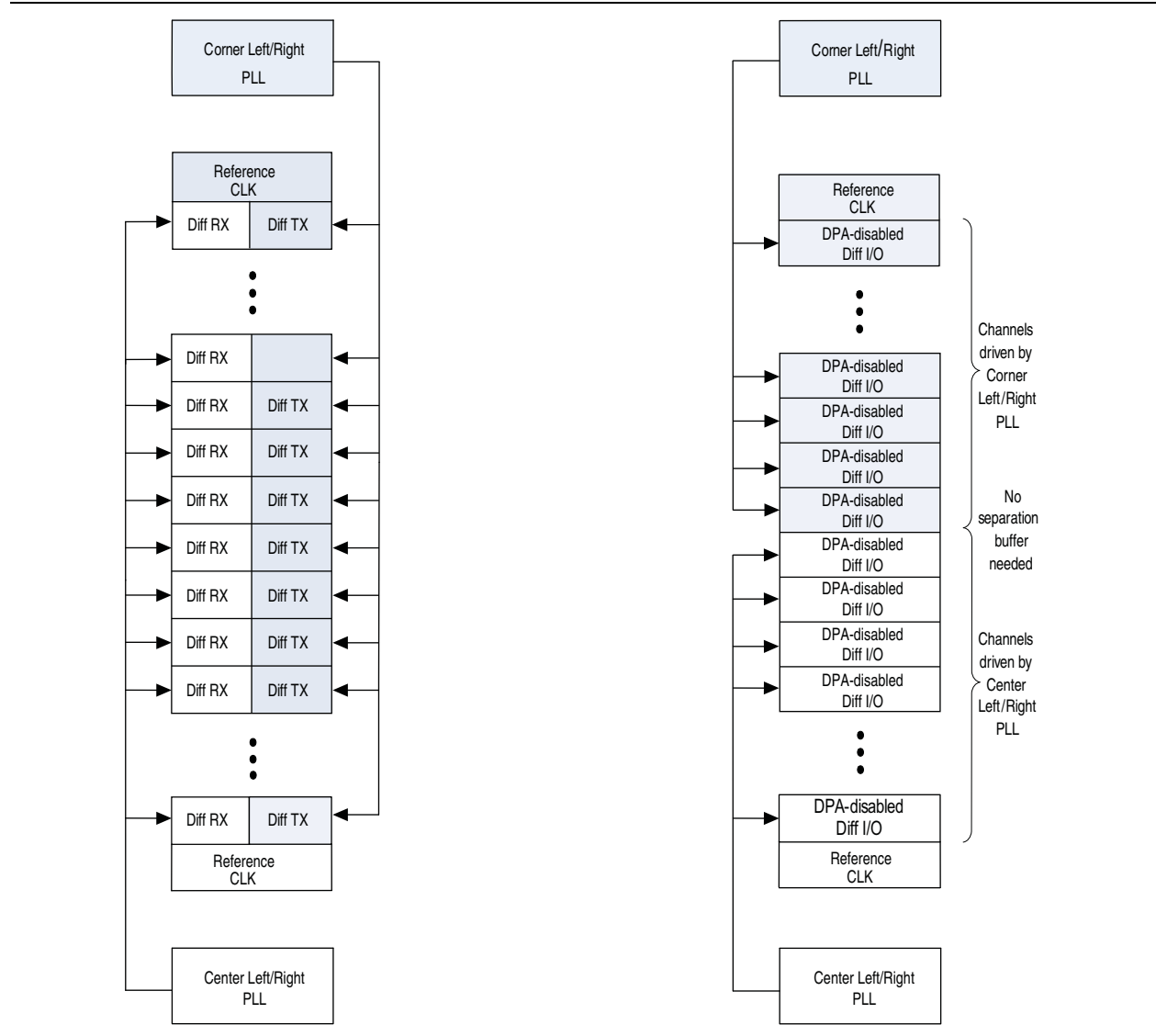
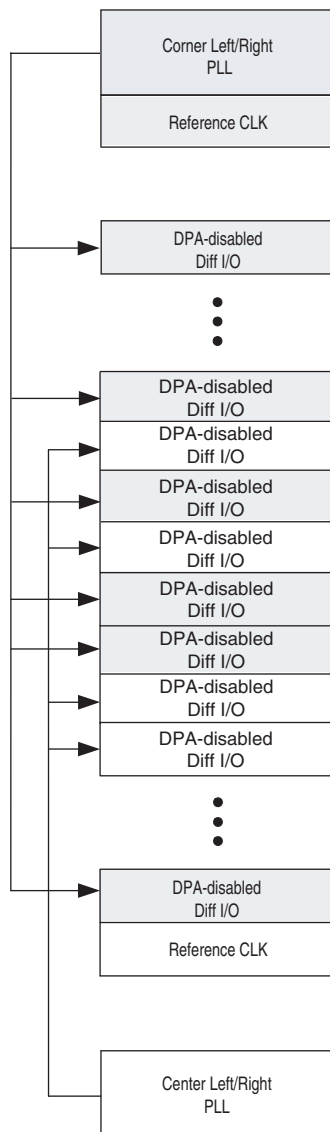


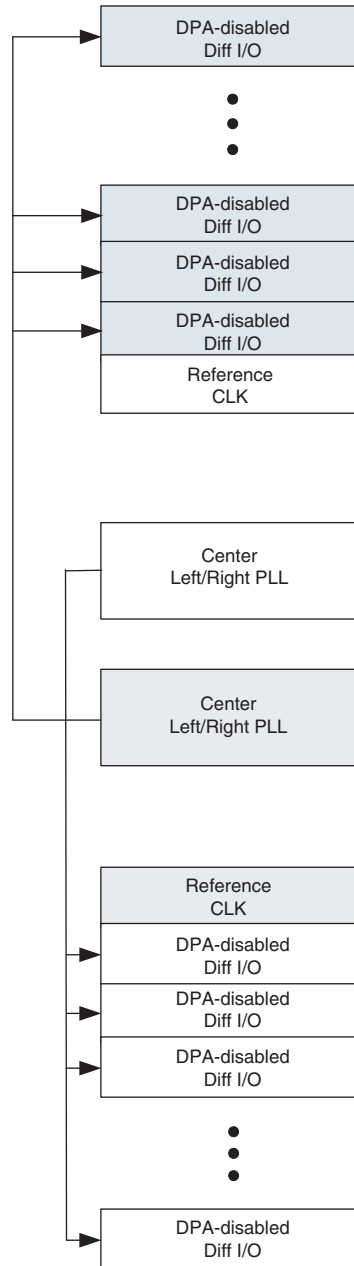
Figure 9-22. Invalid Placement of DPA-Disabled Differential I/Os Due to Interleaving of Channels Driven by the Corner and Center Left/Right PLLs



Using Both Center Left/Right PLLs

- Both center left/right PLLs can be used simultaneously to drive DPA-disabled channels on upper and lower differential banks. Unlike DPA-enabled channels, the center left/right PLLs can drive cross-banks. For example, the upper center left/right PLL can drive the lower differential bank at the same time the lower center left/right PLL is driving the upper differential bank and vice versa, as shown in [Figure 9-23](#).

Figure 9-23. Both Center Left/Right PLLs Driving Cross-Bank DPA-Disabled Channels Simultaneously



Chapter Revision History

Table 9-4 shows the revision history for this document.

Table 9-4. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
May 2009, version 1.7	<ul style="list-style-type: none"> ■ Updated Table 9-1 and Table 9-2. ■ Updated Figure 9-5. ■ Updated “DPA-Enabled Channels and Single-Ended I/Os” section. 	—
February 2009, version 1.6	<ul style="list-style-type: none"> ■ Updated “DPA-Enabled Channels and Single-Ended I/Os” section. ■ Updated Table 9-2. ■ Removed “Reference Documents” section. 	—
October 2008, version 1.5	<ul style="list-style-type: none"> ■ Updated “Introduction”, “Differential Receiver”, and “Synchronizer” sections. ■ Updated Figure 9-5. ■ Updated New Document Format. 	—
May 2008, version 1.4	<ul style="list-style-type: none"> ■ Updated “Soft-CDR Mode”, “Dynamic Phase Aligner (DPA)”, “Programmable Pre-Emphasis and Programmable VOD”, and “Guidelines for DPA-Enabled Differential Channels” sections. ■ Updated Table 9-1 and Table 9-2. ■ Removed “Figure 9-19. Left/Right PLL Driving Distance for DPA-Enabled Channels”. 	—
November 2007, version 1.3	Updated Table 9-1 and Table 9-2 .	Minor updates.
October 2007, version 1.2	<ul style="list-style-type: none"> ■ Added material to “DPA-Enabled Channels and Single-Ended I/Os” on page 9-21 and removed material from “DPA-Disabled Channels and Single-Ended I/Os” on page 9-29. ■ Added new sections “Programmable Pre-Emphasis and Programmable VOD” on page 9-12, “Soft-CDR Mode”, and “Referenced Documents”. ■ Added live links for references. ■ Added Figure 9-10. ■ Minor edits to “DPA-Enabled Channel Driving Distance” section. 	Added new written material, shifted location of some existing written material, added a new figure.
May 2007, version 1.1	<ul style="list-style-type: none"> ■ Minor changes to second paragraph of the section “Differential I/O Termination”. ■ Added Table 9-1 and Table 9-2. 	—
November 2006, version 1.0	Initial Release.	—

