

## 2D FEC IP Core

### General Features

- > 9.3dB net coding gain at 10<sup>-15</sup> output BER – 1 dB of gain higher than standardized EFEC such as the G.975.1 Annexes
- 40G and 100G rates and variable rates in between
- Generic CPU interface for control and monitoring

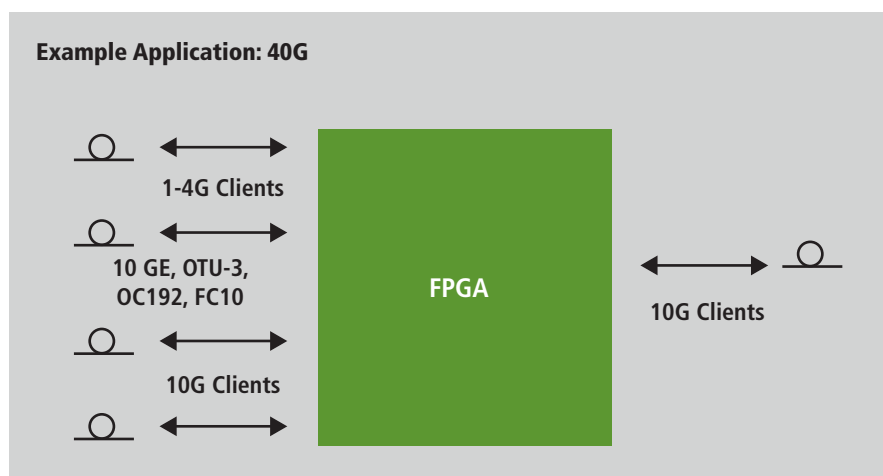
### Statistics:

- corrected bits
- corrected ones
- corrected zeros
- corrected codes
- uncorrectable codes

### Key Features

- High gain EFEC ideal for 40G and 100G applications
- Higher gain and smaller size than standardized EFEC such as the G.975.1 Annexes
- Support for ASIC and FPGA implementations

### Application Diagrams



## Related Products

For additional information regarding Altera FPGA products and NTC OTN IP solution visit [www.altera.com](http://www.altera.com).

## Want to Dig Deeper?

For more information about our 2D FEC IP core, please contact your Altera® sales representative or FAE, or visit [www.altera.com](http://www.altera.com).

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