



EFEC20 100G IP Core

100G Dual-BCH Turbo Product Code EFEC Encoder/Decoder IP core with 20% Overhead

EFEC20 is a multi-dimensional, Turbo Product Code (TPC), Enhanced Forward Error Correction (EFEC) for 100G applications. Providing greater than 10dB Net Electrical Coding Gain (NECG) with standard 20% overhead, the EFEC20 100G IP core, with its flexible FPGA implementation, is smaller in size than existing 100G EFECs in the market today.

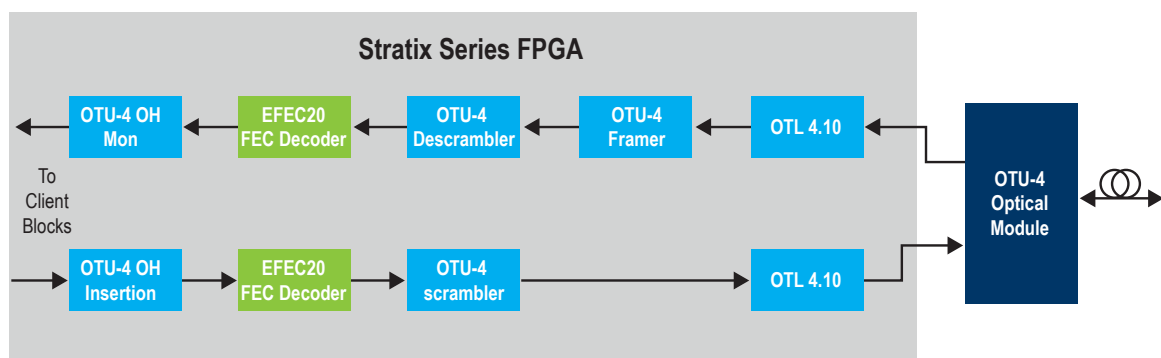
General Features

- Supports G.709 OTU-4
- > 10dB net coding gain at 10-15 output BER with 20% OTN overhead
- Generic CPU interface for control and monitoring
- Available statistics:
 - Corrected bits
 - Corrected ones
 - Corrected zeros
 - Final iteration uncorrectable codes

Key Features

- Smallest available 100G EFEC in the market
- Allows for increased transmission distance or lower transmission power
- Supported by Altera Stratix® IV and Stratix V FPGAs

100G EFEC Application



The EFEC20 IP core provides EFEC for any OTU-4 line signal.

In the receive direction, the frame-aligned and descrambled OTU-4 signal is received by the EFEC20 decoder where the signal FEC is decoded and errors corrected before handoff to the OTU-4 overhead processor.

In the transmit direction, the OTU-4 signal is received at the EFEC20 encoder, where the FEC is calculated and added to the OTU-4 FEC OH. The OTU-4 signal with EFEC is then scrambled and forwarded to the optical module for transmission.

Related Products

For additional information regarding Altera OTN IP products visit www.altera.com.

Want to Dig Deeper?

For more information about our EFEC20, please contact your Altera® sales representative or FAE, or visit www.altera.com.

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