



Spend less. Do more. Get there first.

TIME is the driving force: time to knowledge, time to market, time *in* market, and, of course, time to profit.

With today's competitive pressures and short product life cycles, you need to innovate quickly to win in your marketplace. You face an increasing number of competitors, and need to differentiate your product to reach numerous markets. **TIME** is the driving force: time to knowledge, time to market, time *in* market, and, of course, time to profit.

The ideal development solution would allow you to:

- Get your products to market six to nine months earlier than with a standard cell technology flow
- Create your first product at a fraction of the traditional development cost
- Introduce multiple variations of a product—customized to different markets—at the same time
- Move from prototype to low-cost production quickly, while minimizing cost and engineering effort
- Migrate seamlessly to a structured ASIC for a fast path to production (turnaround time in weeks) with up-front non-recurring engineering (NRE) costs at a fraction of ASIC NRE costs ►



Design Without Compromise

The perfect scenario uses a high-density FPGA as a low-risk prototyping platform that provides the flexibility to test-market your product so you choose the right features before finalizing your design. When you're ready for volume production, you can seamlessly migrate to a structured ASIC that costs up to 90 percent less than the FPGA. And all this is possible with a US\$2,000 development software tool.

Altera is the only company that offers this complete prototype-to-production platform to both system and semiconductor companies. With Altera's solution, you can create your designs using existing development tools, including standard EDA tools, then verify the design in-system with an FPGA. You can demonstrate your technology to customers and change your design on the fly, customizing your products for the marketplace and even bringing multiple variations to different markets at the same time. Because you don't have to commit to an NRE cost, risk and investment is minimal, giving you a competitive advantage. And, to protect your designs against

Demonstrate your technology to customers and change your design on the fly, customizing your products for the marketplace...bringing multiple variations to different markets at the same time.

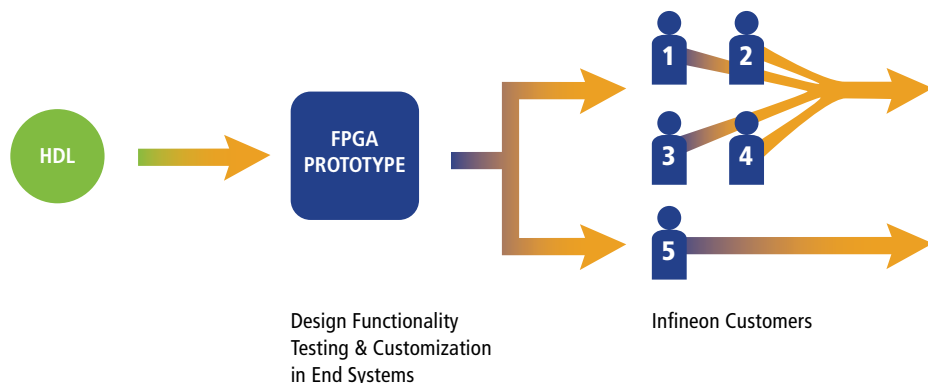
Innovative ASSP Development Model

COMPANY: Infineon Technologies, Communication Group

APPLICATION: MetroMapper 622 ASSP chip, a mapper/framer capable of mapping datacom traffic into SONET/SDH transport payloads

Entering a new market, the Infineon group faced time-to-market pressures, limited engineering resources, limited funding, and multiple customers each looking for customization. Unwilling to risk the time and millions needed for standard cell ASIC development, the Infineon group chose Altera's HardCopy

Infineon Design Flow
Infineon prototyped and tested their design in an FPGA, then created two HardCopy structured ASICs: one was customized for a single customer's requirements, and the other for a broader range of customer needs.



You'll get guaranteed, fully operational structured ASICs in record time, minimizing risk and helping you get to market as quickly as possible.

intellectual property theft, Altera® FPGAs also include built-in, non-volatile encryption.

Once the design is finalized, Altera takes over and migrates it to a pin-compatible, functionally equivalent HardCopy® structured ASIC for mid- to high-volume production. There's no need to re-spin the board. You'll get guaranteed, fully operational structured ASICs in record time, minimizing risk and helping you get to market as quickly as possible.

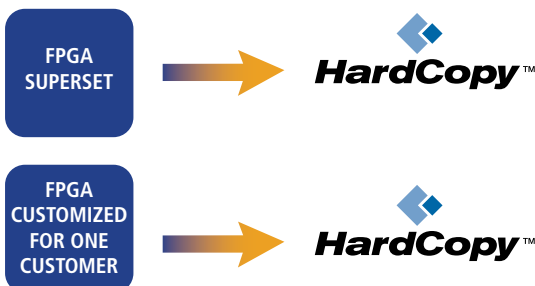
HardCopy Development Flow

The seamless prototype-to-production flow available with Altera's HardCopy devices simplifies design. Engineers simply create and optimize their design for the FPGA and verify the design in-system, then create an archive file to hand off to the Altera HardCopy Design Center. ASIC prototypes are delivered in record time.



structured ASICs. Infineon sent Stratix® FPGA development boards to various customers for design input and created two FPGA supersets, ultimately making a number of customers happy. After in-system validation, the Infineon design was migrated to two HardCopy structured ASICs by Altera.

This unique design methodology allowed the Infineon group to uniquely customize the designs for end customers at a fraction of the cost of ASIC development. The fast turnaround time for HardCopy prototypes enabled Infineon to beat their competition to market.



For more information, visit www.altera.com/hardcopy

Ask the experts.

Get to production in *record* time.

- Q How does a structured ASIC differ from a standard cell ASIC?**
- A** With ASICs, all silicon layers are customized. In contrast, structured ASICs start with standard, pre-tested base layers of logic and hard intellectual property (IP), and the proprietary design is then implemented on the top few metal layers. This process saves development time and costs considerably less, but can be risky if you don't verify the design in-system before committing to silicon. Altera offers the only solution with an FPGA front-end, minimizing cost and risk, improving flexibility, and speeding time-to-market.
- Q Are HardCopy series structured ASICs pin-compatible with their FPGA counterparts?**
- A** Yes. HardCopy structured ASICs are pin- and footprint-compatible with their FPGA counterparts, eliminating the need to respin the board.
- Q How much power reduction can I expect when moving from an FPGA to a HardCopy II structured ASIC?**
- A** HardCopy II structured ASICs can consume less than half the core power of their FPGA counterparts (dynamic and static) because the HardCopy II die is significantly smaller, and because only the logic used in the HardCopy II device is powered on.
- Q What design files do I deliver to Altera for the migration process?**
- A** Using Altera's Quartus® II development software, simply generate a Quartus II Archive File (.qar) using the HardCopy Files Wizard. This file contains everything the HardCopy Design Center needs to develop a HardCopy structured ASIC. The Altera HardCopy Design Center manages the migration process.
- Q How long does it take to migrate a design to a HardCopy structured ASIC?**
- A** Once all the required design guidelines are met and Altera accepts the design, the design can be migrated to a HardCopy series structured ASIC in two to four weeks. HardCopy prototypes will generally be available within five to seven weeks after you have approved the timing results. Production units will generally be delivered within eight weeks from when the prototypes are approved.
- Q Do I need to modify my design or use additional design software to migrate from an FPGA to a HardCopy structured ASIC?**
- A** No. You can use the same Quartus II design software to migrate your FPGA design—including any IP that is part of the design—to a HardCopy structured ASIC.
- Q What third-party EDA software can I use to develop the design?**
- A** Altera's design flow supports standard synthesis, verification, timing analysis, and equivalency checking tools from Cadence, Mentor Graphics, Synopsys, and Synplicity in conjunction with Altera's Quartus II design environment, minimizing training time and expenses. The Quartus II software, the only design software that supports parallel FPGA and structured ASIC design and development, also supports the same basic design, register transfer level (RTL) synthesis, place-and-route, and verification flows used by ASIC designers.

For more information, visit www.altera.com/hardcopy



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