

Designing with 40-nm Stratix IV GT devices—only FPGAs with integrated 11.3-Gbps transceivers

40G/100G network applications

From Internet protocol television (IPTV) to online videos and high-definition programming, bandwidth-heavy applications are continuing to flourish. To support these demands, build your aggregated carrier and transmission systems for 40G/100G networks with 40-nm Stratix® IV GT FPGAs, the market's only FPGAs with integrated 11.3-Gbps transceivers.

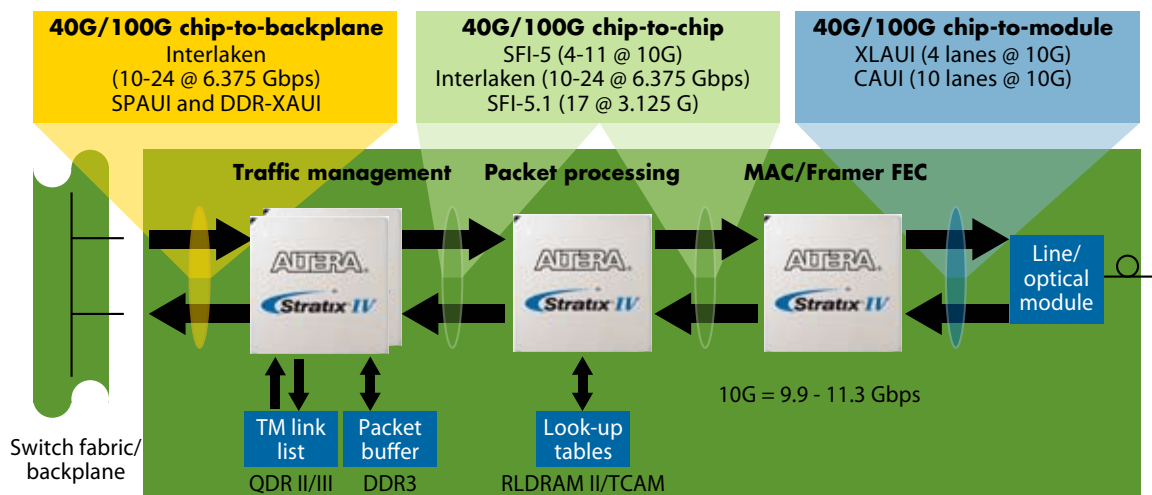
With Stratix IV GT FPGAs, you can start your next-generation designs now. Our devices are the only single-chip FPGAs capable of connecting directly to optical modules that can meet the emerging standards to implement true 100G systems. Start building your 100G systems before the IEEE specification is ratified, and have the design flexibility to easily accommodate specification shifts that might emerge.

System integration conserves power, board space

Without external transceiver components, you can apply the higher densities of a smaller process geometry. Stratix IV GT FPGAs integrate key design components into one device, saving power, board space, and, ultimately, cost. Benefits include:

- Fastest transceivers—up to 24 transceivers at 11.3 Gbps, plus LVDS at 1.6 Gbps
- Lowest system power—low 0.9V core power; Programmable Power Technology, which automatically optimizes logic, digital signal processing (DSP), and memory blocks for the lowest power at the required performance
- Best-in-class signal integrity—with noise filtering, on-die and on-packing decoupling
- Fastest memory interfaces—1,067 Mbps (533 MHz) DDR3
- Highest density—up to 530K logic elements (LEs)

40G/100G line card with Stratix IV GT FPGAs



Only Stratix IV GT FPGAs offer direct 10G chip-to-chip and chip-to-optical module connections

Feature-rich transceivers

Featuring transceiver counts aligned with 40G/100G system requirements, Stratix IV GT FPGAs are ideal for a variety of existing and emerging protocols, making them a cost-effective bridging device.

The transceivers include a physical coding sublayer (PCS) and a physical media attachment (PMA) sublayer. The PMA is an embedded macro that's dedicated to receiving and transmitting high-speed serial data streams. The PMA channel is comprised of full duplex transmit and receive paths with I/O buffers, programmable output voltage, pre-emphasis and equalization, clock data recovery (CDR), and serializer/deserializer (SERDES) blocks.

With dynamically reconfigurable transmit pre-emphasis and receiver equalization, you can drive a 50-inch backplane on FR-4 at 6.375 Gbps. Plug & Play Signal Integrity—comprised of our adaptive dispersion compensation engine (ADCE) and hot socketing—allows you to change the position of backplane cards on the fly, without manually configuring backplane equalization settings.

Stratix IV GT device family

Device	LEs	Transceivers 11.3 Gbps (Total)	LVDS	I/Os	Memory (Mbits)	Package
40G devices						
EP4S40G2	230K	12 (36)	44	636	13.9	F1517
EP4S40G5	530K	12 (36)	44	636	20.3	H1517
100G devices						
EP4S100G2	230K	24 (36)	44	636	13.9	F1517
EP4S100G3	290K	24 (48)	44	754	13.3	F1932
EP4S100G4	360K	24 (48)	44	754	17.7	F1932
EP4S100G5	530K	24 (48)	44	754	20.3	F1932

Time-to-market advantages

Enjoy the productivity benefits of designing with Quartus® II design environment, which features 3X faster compile times than competitive design software, efficient resource utilization, and additional compile time reductions through incremental compilation.

Third-party intellectual property (IP) cores

IP core	Provider	Description
40G/100G MAC and PCS	MoreThanIP	Full MAC layer and reconciliation sub-layer solution; complete 40G Base-R or 100G Base-R PCS solution
40G/100G MAC and PCS	Sarance Technologies	Full MAC layer and reconciliation sub-layer solution; complete 40G Base-R or 100G Base-R PCS solution
Interlaken	Sarance Technologies	Compliant to Interlaken specification R.1.1 with 1 to 24 Interlaken lanes, up to 120G throughput, 3.125 to 6.375 Gbps, and internal 64-/128-/256-/512-bit bus
Interlaken	Altera	Compliant to Interlaken specification R.1.1 with 1 to 24 Interlaken lanes, up to 120G throughput, 3.125 to 10.3125 Gbps, and internal 128-, 256-, 512-bit buses
40G SFI-5	Avalon Microelectronics	40G SDH/SONET; SFI-5 interface to optics; supports channelized (to STS-1) and concatenated traffic; optional packet over SDH/SONET support

Want to dig deeper?

For more information about how Altera's 40-nm Stratix IV GT FPGAs can support your 40G/100G network applications, contact your local sales representative or FAE, or visit www.altera.com/stratix and click on the "Stratix IV (E and GX)" link on the left.

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1494 602000

Altera Japan Ltd.
Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
Unit 11- 18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2 945 7000
www.altera.com.cn

