

## HardCopy ASICs

Electronic systems design is growing more challenging, with a narrowing range of technology options that are becoming less attractive over time. Standard-cell ASICs are too risky and expensive to design, as shown by the significant reduction in worldwide design starts over the last few years. ASSPs leave products undifferentiated versus your competition. And processor-based solutions are just not optimized enough for most applications.

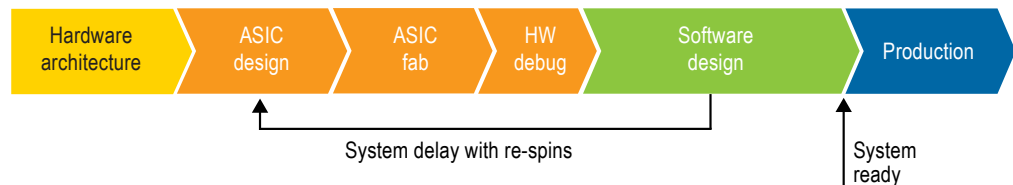
FPGAs, by contrast, are getting more and more capable as they ride Moore's Law further down the process curve, though there remain cost and power consumption concerns for high-end, high-volume applications. This is where Altera's HardCopy® ASICs can give you the advantage.

### HardCopy system development methodology

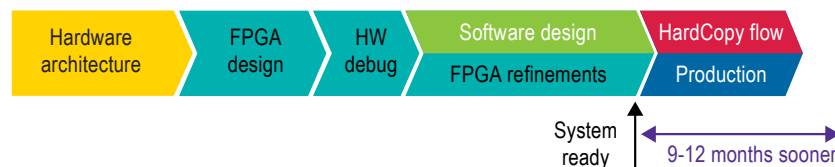
HardCopy ASICs enable a system design process with the flexibility of FPGAs and the lower power and cost of ASICs for your power-sensitive and/or high-volume applications. Because HardCopy series ASICs and our Stratix® series FPGAs share the same hard intellectual property (IP) cores, they are truly interchangeable. Use a seamless prototyping process to design and verify your system hardware and software once, at-speed with a Stratix series FPGA, and deliver your system to market sooner with HardCopy ASICs.

#### Faster system development with HardCopy ASIC

System development with traditional ASIC



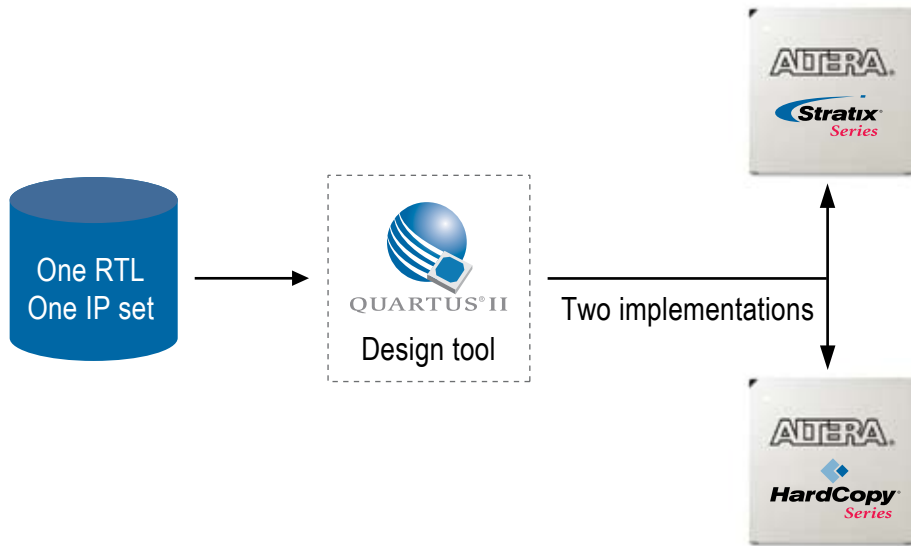
System development with HardCopy ASIC



## Design once for guaranteed success

Building upon three generations of HardCopy ASICs, Altera has developed a true “design once” flow for both HardCopy ASICs and their prototyping FPGAs. At the front end, before design handoff, use one design, one IP set, one methodology, and one tool to create two device implementations. Get your system ready for production with an FPGA prototype, and Altera guarantees a functional equivalent and pin-/footprint-compatible HardCopy ASIC as a drop-in replacement for volume production.

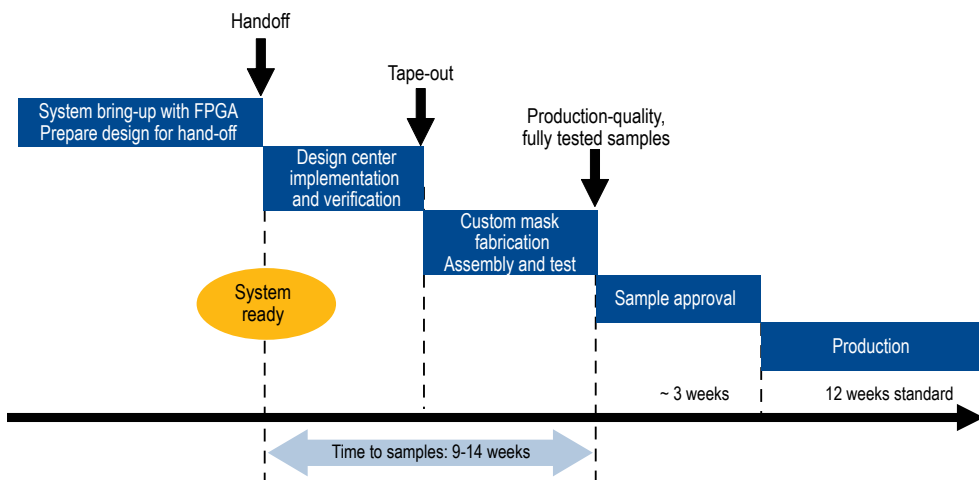
### One design, one RTL, one IP set, two implementations



## Fast and predictable turnaround time

When your system is ready, you can perform market testing or initial production with Stratix series FPGAs. If for power, single event upset (SEU), performance, and/or cost reasons, production requires HardCopy ASICs, Altera’s HardCopy Design Center provides a fast, predictable, turnkey process that includes full test insertion. You’ll have a fully tested, production-quality sample in as little as nine weeks, with no design-for-test effort from your own team.

### HardCopy series design timeline



## Customers tell us

Our customers report that HardCopy ASICs bring:

- **Reduced risk** – Completely validate systems with the FPGA before switching to the HardCopy device.
- **Reduced total cost** – Experience a low NRE compared with standard-cell ASICs, and dramatically reduced total development cost from factors including a smaller engineering team, faster design and verification time, and inexpensive development tooling cost.
- **Faster time to market** – Use the FPGA's flexibility to speed system verification and software development, and get your system completely ready for initial production with Stratix series FPGAs prior to ASIC handoff.
- **Faster time to profit** – Get your system to market sooner and, with the fast and predictable turn-around time to produce a HardCopy ASIC, quickly turn market share into high-volume profit.

### HardCopy ASICs

	Packages <sup>5</sup>					FPGA prototype	6.5+G <sup>2</sup> SERDES	I/O pins	Memory bits (Mbits) <sup>4</sup>	18x18 Multipliers	PLLs	ASIC gates <sup>3</sup>		
	Device <sup>1</sup>	F484	F672	F780	F1152								F1517	
HardCopy IV GX ASICs	HC4GX1YZ			L			EP4SGX70	8	372	6.3	384	3	2.8M	
	HC4GX2YZ			L	L,F		EP4SGX110 EP4SGX180	8/16/24/36	372 – 564	6.3 – 11.0	512 – 920	3/4/6	3.8 – 6.7M	
	HC4GX3YZ			L	L,F	L,F	EP4SGX180 EP4SGX230	8/16/24/36	372 – 744	8.9 – 13.9	920 – 1,288	3/6/8	6.7 – 9.2M	
	HC4GX4YZ			L	L,F	L,F	EP4SGX290	8/16/24/36	257 – 744	9.2 – 13.3	832	2/4/6/8	7.7M	
	HC4GX5YZ			L	L,F	L,F	EP4SGX360	8/16/24/36	257 – 744	9.2 – 17.7	1,040	2/4/6/8	9.4M	
	HC4GX6YZ				F	L,F	EP4SGX530	24/36	564 – 744	13.3 – 20.3	1,024	6/8	11.5M	
HardCopy IV E ASICs	HC4E2YZ	W,F		W,F			EP4SE110	-	296 – 488	8.1	512	4	3.8M	
	HC4E3YZ	W,F		W,F			EP4SE230	-	296 – 488	10.7	1,288	4	9.2M	
	HC4E4YZ			W,F	L,F	L,F	EP4SE290	-	392 – 880	12.1 – 13.3	832	4/8/12	7.7M	
	HC4E5YZ				L,F	L,F	EP4SE360	-	736 – 880	17.7	1,040	8/12	9.4M	
	HC4E6YZ				L,F	L,F	EP4SE530	-	736 – 880	18	1,024	8/12	11.5M	
	HC4E7YZ				L,F	L,F	EP4SE680	-	736 – 880	18.4	1,360	8/12	15.0M	
HardCopy III ASICs	HC31YZ	W,F		W,F			EP3SL110	-	296 – 488	4.1	288	4	2.7M	
	HC32YZ	W,F		W,F	L,F		EP3SL150	-	296 – 744	5.4	384	4/8	3.6M	
	HC33YZ	W,F		W,F	L,F		EP3SE110	-	296 – 744	5.4 – 7.9	896	4/8	5.8M	
	HC35YZ	W,F		W,F	L,F	L,F	EP3SL200	-	296 – 880	5.4 – 9.2	576	4/8/12	5.3M	
	HC36YZ	W,F		W,F	L,F	L,F	EP3SE260	-	296 – 880	5.4 – 14.3	768	4/8/12	6.9M	
	HC37YZ	W,F		W,F	L,F	L,F	EP3SL340	-	296 – 880	12.1 – 15.9	576	4/8/12	7.0M	
F484 F672 F780 F1020 F1508														
HardCopy II ASICs	HC210W	W					EP2S30 EP2S60 EP2S90	-	285 – 308	.65 – .86	64-192	4	1M	
	HC210	F						-	308 – 334	.65 – .86	64-192	4	1M	
	HC220W		W	W			EP2S60 EP2S90 EP2S130	-	442 – 444	2.3 – 3.0	144-252	4	1.9M	
	HC220		F	F				-	492 – 494	2.3 – 3.0	144-252	4	1.9M	
	HC230				F			EP2S90 EP2S130 EP2S180	-	698	4.1 – 6.2	192-384	8	2.9M
	HC240				F	F		EP2S180	-	742-951	8.6	384	12	3.6M

Notes:

1. Y = I/O count, Z = package type
2. Subject to increase pending characterization
3. ASIC gates calculated as 12 gates per LE; plus 5,000 gates per 18x18 multiplier
4. HardCopy III and IV ASICs support MLAB memories that are not included in the count
5. F=performance-optimized flip chip; L=cost-optimized flip chip; W=wire bond

### Highly integrated, ASIC-strength design tool

Our Quartus® II design software works with our FPGAs and ASICs to provide a design environment that is easy to use and generates results quickly. The software provides Synopsys Design Constraint (SDC-) based synthesis, placement and routing, and static timing analysis.

	Quartus II software
RTL synthesis	√
Physical synthesis	√
Simulation	√
STA (front end)	√
Detailed placement	√
Global routing	√
Incremental compile	√
Formal verification	√
Pin planning	√
Power estimation	√

## More HardCopy ASIC benefits

HardCopy ASICs also deliver:

- **Low power** – Low levels of power, like that of standard-cell ASICs. For low leakage current, we've removed all unused blocks—RAMs, logic, global clocks, and phase-locked loops (PLLs)—from the power rail. For low dynamic power, we've implemented hard-wired routing and clocking circuitry in the devices. HardCopy ASICs can deliver 50 percent or greater power reduction from the prototyping FPGAs.
- **SEU immunity** - HardCopy ASICs are built using an array of fine-grained HCell blocks that are configured and grouped together by via programming to construct the FPGAs combinational and sequential logic functions and digital signal processing (DSP) blocks. The connections between HCells are hard-wired after via programming. The inherent high SEU tolerance of HardCopy ASICs is not only a result of the hard-wiring, but also due to an improved sequential elements architecture.
- **Higher performance** - HardCopy ASICs can provide up to 2X core logic performance improvement over the FPGA prototype device, due to:
  - Removal of programmable switching multiplexers in the FPGA
  - Shorter routing from a much smaller die compared to the FPGA
  - Fewer logic levels for certain combinatorial logic paths
  - Flexibility in HCell macro placement
- **Better security** – With no device configuration, HardCopy ASIC designs are secure from tampering.
- **Instant-on** – This capability supports designs that must power up, ready to go.

## Want to dig deeper?

For more information about designing with HardCopy ASICs, contact your local Altera sales representative or FAE, or visit [www.altera.com/hardcopy](http://www.altera.com/hardcopy).

## Getting started with HardCopy ASICs

Systems architected for HardCopy ASICs enable true hardware and software co-design and tremendously reduce system time to market and time to profit. The simplicity of using Altera's Quartus II design software tool, combined with IP from Altera and our partners, allows you to design both the FPGA and ASIC simultaneously. Simply select the appropriate Stratix series FPGA and HardCopy companion device in the Quartus II software and start your design—it's that easy.

**Altera Corporation**  
101 Innovation Drive  
San Jose, CA 95134  
USA  
[www.altera.com](http://www.altera.com)

**Altera European Headquarters**  
Holmers Farm Way  
High Wycombe  
Buckinghamshire  
HP12 4XF  
United Kingdom  
Telephone: (44) 1 94 602 000

**Altera Japan Ltd.**  
Shinjuku i-Land Tower 32F  
6-5-1, Nishi-Shinjuku  
Shinjuku-ku, Tokyo 163-1332  
Japan  
Telephone: (81) 3 3340 9480  
[www.altera.co.jp](http://www.altera.co.jp)

**Altera International Ltd.**  
Unit 11-18, 9/F  
Millennium City 1, Tower 1  
388 Kwun Tong Road  
Kwun Tong  
Kowloon, Hong Kong  
Telephone: (852) 2945 7000

