

DDR, DDR2, QDR II and RLD RAM II

Complete high-performance memory interface design solutions

Get the highest levels of memory bandwidth while accelerating your time-to-market.

You'll finish your next design in record time with Altera's high-performance FPGAs, customizable IP functions, easy-to-use design software with fast timing closure, development kits, and structured ASICs reference designs. Our products help you integrate a wide range of memory devices into your high-speed networking, wireless, computing, storage, or test and measurement system designs.

Advanced device architecture

- Stratix®, Cyclone®, and HardCopy® series
- High-performance logic arrays that support high-speed clock frequencies and data rates
- Multiple I/O standards (SSTL, HSTL, and more)
- Dedicated data strobe (DQS) phase shift circuitry
- Phase-locked loops (PLLs) and advanced clock networks

High-performance external memory support

Memory technology	I/O standard	Maximum clock speed	Maximum data rate
DDR SDRAM	SSTL-2	200 MHz	400 Mbps
DDR2 SDRAM	SSTL-18	333 MHz	667 Mbps
QDR II SRAM	1.8-V HSTL	300 MHz	1,200 Mbps ¹
QDR II+	1.5-V HSTL	300 MHz	1,200 Mbps ¹
RLDRAM II	1.8-V HSTL	300 MHz	600 Mbps

¹For both read and write ports.

Memory controller MegaCore® function support



View documentation

Customize for your system requirements

Generate design and timing constraints

Set up cycle-accurate simulation

Generate final MegaCore function variation

Customizable memory controller IP functions

- Fully hardware-verified memory controller IP functions—DDR, DDR2, QDR II, and RLD RAM II
- Self-calibrating circuits perform PVT compensation for higher performance
- Automatically generated constraint files and simulation models
- Free evaluation using OpenCore® Plus
- Step-by-step graphical user interface for easy instantiation of your memory interface designs in Quartus® II design software
- Comprehensive design flow to manage timing, clock, simulation, synthesis, and integration
- Complete documentation

TimeQuest static timing analysis tool

- ASIC-strength static timing analysis tool designed with high speed memory interfaces in mind
- Built for higher performance and faster timing closure
- Comprehensive native Synopsys design constraints (SDC) support (an FPGA industry first!)
- Powerful, easy-to-use GUI for analysis

Development kits and hardware reference platforms

- Complete reference designs developed with industry-leading memory suppliers
- Board design files: schematic, layout, and Gerber files
- IBIS and SPICE simulation models
- Signal integrity and termination recommendations, high-speed PCB design guidelines, and application notes

Hardware-verified memory interface solutions

Stratix II memory reference platform for
DDR & RDRAM II



Stratix II memory reference platform for
QDR II & DDR2



Stratix II high-speed development board for DDR2



Stratix II GX PCI Express board for QDR II, DDR2



On line memory solutions center

Get all the information you need at the Memory Solutions Center on Altera's website.

To learn more about Altera's complete memory solutions, please contact your Altera sales representative for a demo or visit www.altera.com/memory.

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