Market-leading GFLOPS/Watt performance

Altera's floating-point solutions for military applications

Equal sustained and peak performance

Benchmark tests show that Altera® FPGAs deliver sustained performance that nearly equals peak performance.

More and more advanced sensor applications such as radar and electronic warfare, both in the front and back end, require floating-point calculations. FPGAs deliver a powerful mix of fixed- and floating-point performance—with superior giga floating-point operations per second (GFLOPS)/Watt compared to other technologies.

Advanced sensors rely on finding the maximum absolute value of a function. This function results from the cross-correlation of a sent signal with the received signal. Such a function can be computed using fast Fourier transform (FFT) techniques. Floating point is greatly helpful when computing large FFTs, and there are no drawbacks to using a floating-point function within an FPGA. What's more, power is not a major issue when using advanced 40-nm FPGAs in the latest advanced sensor applications.

Altera offers some of the highest density, lowest power FPGAs in the market. Our 65-nm Stratix® III FPGAs and new 40-nm Stratix IV FPGAs are equipped with many multipliers per hardened digital signal processing (DSP) block, which reduces routing and logic for larger multipliers. In a recent National Science Foundation benchmark, a Stratix IV FPGA delivered 171 GFLOPS, and was the clear overall leader in highest GFLOPs/Watt.

Floating-point multiplier capabilities for select Stratix III FPGAs

Device	Adaptive logic modules (ALMs)	18x18 multipliers	36x36 multipliers	54x54 multipliers	Memory (Kbits)
EP3SE110	42,600	896	224	89	8,055
EP3SL200	79,560	576	144	57	7,668
EP3SE260	101,760	768	192	76	14,688
EP3SL340	135,200	576	144	57	16,272

Floating-point multiplier capabilities for select Stratix IV FPGAs

Device	Adaptive logic modules (ALMs)	18x18 multipliers	36x36 multipliers	54x54 multipliers	Memory (Kbits)
EP4SGX230	182,400	1,288	322	128	14,283
EP4SGX360	282,880	1,040	260	104	18,144
EP4SGX530	212,480	1,024	256	102	20,736
EP4SE680	272,440	1,360	340	136	22,977

Matrix operators 3–7 GFLOPs/Watt—single precision

Matrix multiply core examples	Vector size	Logic usage					Giga floating-point operations per second (GFLOPS)	Performance (Stratix IV FPGA)	Power (mW)			
		Adaptive logic modules (ALMs)	18x18 multipliers	M9K blocks	M144K	Memory (Kbits)			Static	Dynamic	I/O	Total
(36x112)x(112x36)	8	4,604	32	43	2	576	4	291 MHz	2,008	1,063	300	3,334
(36x224)x(224x36)	16	7,882	64	77	4	1,102	9	291 MHz	2,045	1,821	300	4,165
(36x448)x(448x36)	32	14,257	128	137	8	2,153	18	291 MHz	2,110	3,448	300	5,858
(64x64)x(64x64)	32	13,154	128	41	8	1,333	18	292 MHz	2,112	2,604	306	5,023
(128x128)x(128x128)	64	25,636	256	141	16	3,173	37	293 MHz	2,244	5,384	306	7,934

IEEE 754-compliant floating-point megafunctions

Altera provides the largest library of IEEE 754-compliant floating-point megafunctions. Ideal for single-precision and double-precision output, these megafunctions can be used in any Altera device. They also can be parameterized in a variety of ways to fine-tune GFLOP performance for your specific military application. Key megafunctions include:

Basic

- Addition/subtraction [altfp_add_sub]
- Multiplication [altfp_mult]
- Division [altfp_div]
- Square root [altfp_sqrt]
- Compare [altfp_compare]
- Conversion

Altera unique

- Matrix multiplier [altfp_matrix_mult]
- Logarithm [altfp_log]
- Exponential [altfp_exp]
- Inverse [altfp_inv]
- Inverse square root [altfp-inv_sqrt]

New and available soon

- Matrix inversion
- Trigonometric functions
- Floating-point datapath optimizer

Want to dig deeper?

For more information about how Altera solutions can support your floating-point requirements, contact your local Altera sales representative or FAE, or visit **www.altera.com/dsp**.

Arithmetic logic unit (ALU) and multiplier cores

Double-precision cores

Core	ALUTs	Registers	18x18 multipliers	Latency	Performance (Stratix IV FPGA)
ALU (area)	956	1,459	–	14	269 MHz
ALU (speed)	1,060	1,506	–	14	409 MHz
Multiplier	383	706	10	11	386 MHz

Single-precision cores

Core	ALUTs	Registers	18x18 multipliers	Latency	Performance (Stratix IV FPGA)
ALU (area)	541	611	–	14	497 MHz
ALU (speed)	601	678	–	14	499 MHz
Multiplier	150	391	4	11	431 MHz

Library functions

Double-precision cores

Core	ALUTs	Registers	18x18 multipliers	Latency	Performance (Stratix IV FPGA)
Divider (low latency)	681	1,072	44	10	142 MHz
Divider	5,119	7,360	–	61	273 MHz
SQRT	2,089	3,767	–	57	375 MHz
Inverse	1,041	1,524	48	27	192 MHz
Inverse SQRT	1,332	1,947	78	36	208 MHz

Single-precision cores

Core	ALUTs	Registers	18x18 multipliers	Latency	Performance (Stratix IV FPGA)
Divider (low latency)	215	304	16	6	150 MHz
Divider	1,624	2,074	–	33	316 MHz
SQRT	503	932	–	28	478 MHz
Inverse	440	683	16	20	401 MHz
Inverse SQRT	485	705	22	26	401 MHz

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