



### Flexible, scalable Altera FPGA-based platform

## Packet processing solutions for broadband access applications

Need to quickly and cost-effectively differentiate your wireline access infrastructure? Facing new protocols, access methods, and evolving system architectures? Have to constantly scale system bandwidth? Altera® FPGAs are equipped to provide a packet processing platform that meets all of these challenges hands down.

From our low-cost Cyclone® series FPGAs to our high-performance Stratix® series devices, Altera programmable solutions can be implemented in flexible, scalable building blocks or as part of a customized system. You can either develop your differentiated network processing unit (NPU) in-house or buy a pre-built, customizable processor. Either way, working with Altera and our partners will help you to develop your ideal architecture quickly, cost effectively, and without any worries of component obsolescence.

#### FPGAs demonstrate advantages over ASSPs

Packet processing requirements	Altera FPGA-based packet processing platform	Traditional ASSP-based NPU
Development speed*	Fast <ul style="list-style-type: none"> <li>• Three months for "shrink-wrapped" NPU on FPGA</li> <li>• Nine months or less for custom FPGA-based NPU</li> </ul>	Slow <ul style="list-style-type: none"> <li>• Six to nine months in software development for NPU application on ASSP</li> </ul>
Acquisition and development cost	Low <ul style="list-style-type: none"> <li>• Simple design methodology and tools</li> <li>• Ease of design change</li> <li>• Many choices</li> </ul>	High <ul style="list-style-type: none"> <li>• Complex design methodology and tools</li> <li>• Difficult to change/debug</li> <li>• Very few choices</li> </ul>
Maintenance and upgrade	Low <ul style="list-style-type: none"> <li>• Easy to debug and port</li> </ul>	High <ul style="list-style-type: none"> <li>• Difficult to debug and port</li> </ul>
Flexibility in adding new features	Fully flexible due to hardware and software reprogrammability	Limited, as the design can only be reprogrammed at the software level
Silicon roadmap/sustainability**	High <ul style="list-style-type: none"> <li>• Total available market (TAM) for FPGAs over \$3 billion</li> <li>• Two dominant players</li> </ul>	Low <ul style="list-style-type: none"> <li>• Small TAM of less than \$200 million***</li> <li>• Many players</li> </ul>

\*Estimates based on customer experiences

\*\*Many NPU vendors have exited the market due to bankruptcy or acquisition

\*\*\*According to industry estimates

#### Control your design destiny

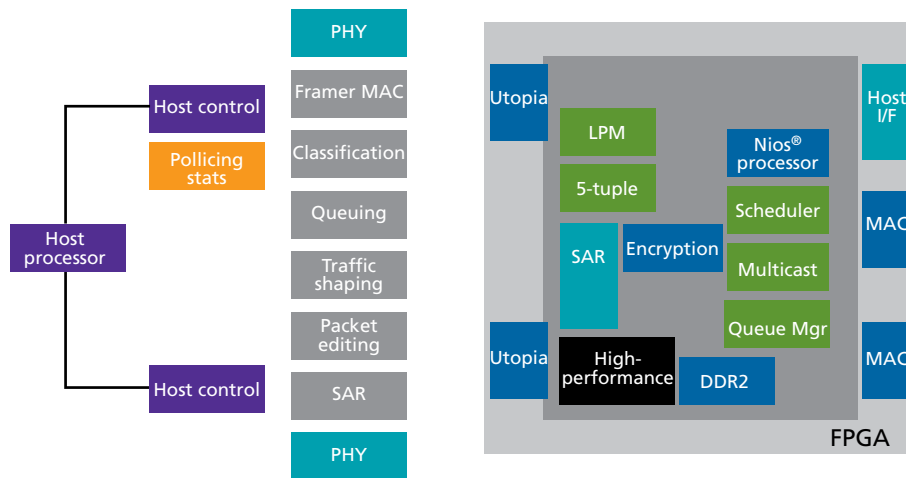
Currently available ASSP-based NPU development options come with a host of drawbacks. Multi-core processing solutions suffer from software complexity and fixed resources. General-purpose CPUs are not able to deliver the performance requirements desired of data-path processing elements. ASICs try to address some of these limitations; however, they usually end up being costly in terms of time and money.

Whether you want to develop in-house using Altera FPGAs or use pre-built NPU solutions on our FPGAs, you gain time-to-market and cost advantages and lowered risk. Programmability at the hardware and software layers gives you flexibility when you need to

adapt your solution. Intellectual property (IP) cores reduce development time and costs. You also gain continuous access to leading-edge silicon technologies with sustained roadmaps.

For faster product availability, prototype in a high-performance Stratix series FPGA and migrate seamlessly to a low-cost HardCopy® series structured ASIC for volume production. For a low-cost packet processing system, look to our Cyclone series FPGAs and, if you need integrated serializer/deserializer (SERDES) for Gigabit Ethernet backplane, consider our transceiver-based Arria™ GX FPGAs.

## Customizable packet processing architecture



*A flexible packet processing architecture based on programmable technology lets you support custom requirements.*

## Deliver more with less

### Develop your own FPGA-based custom NPU

- Packet processing modules and framework from Altera, including Stratix series FPGAs, Cyclone series FPGAs, and Nios II embedded processors
- Design environment and reference designs from Octera Technology Solutions or AimCom BV

### Buy your “shrink-wrapped” NPU on an FPGA

- Pre-built access solutions from Ethernity Networks
- Custom-built classification, search, content addressable memory (CAM) replacement, and traffic policing and IP cores from Sarance Technologies

## Example applications

- DSLAM packet processing
- xPON (passive optical network) packet processing
- TDMoEthernet/pseudowire/CES

## Want to dig deeper?

If you have packet processing system design questions or ideas to share, please contact your local Altera FAE or sales representative, or visit [www.altera.com/wireline](http://www.altera.com/wireline).

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