

Feature rich, easy to use, and low power

PCI Express hard intellectual property solutions from Altera

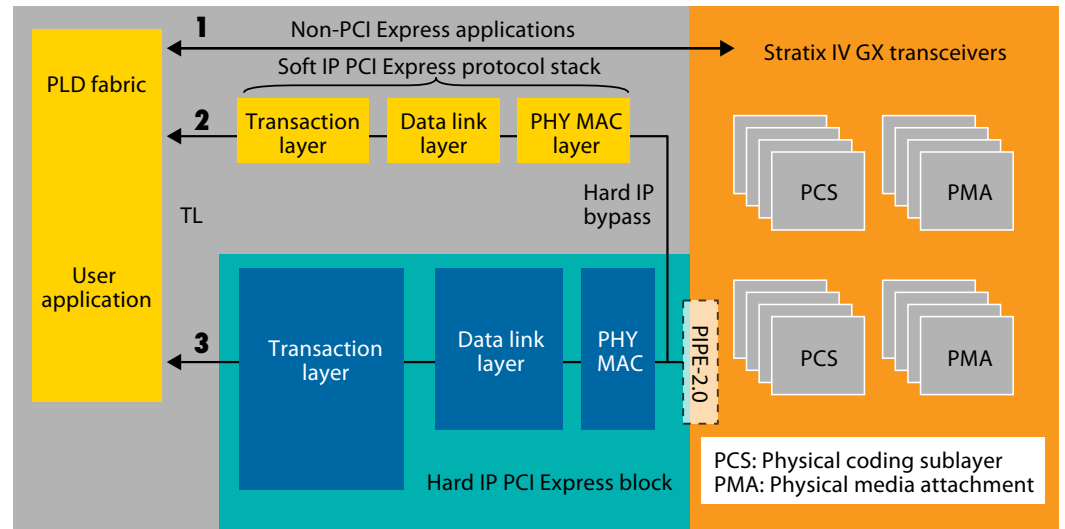
With low or even no cost, ease of use, and low power, Altera’s PCI Express hard intellectual property (IP) solutions enable you to create high-value, high-bandwidth transceiver-based applications. Our new 40-nm devices—Stratix® IV FPGAs and HardCopy® IV ASICs—are equipped with PCI Express support.

Stratix IV FPGAs provide up to four hard IP blocks for PCI Express Gen1 and Gen2, supporting x1, x2, x4, and x8 lane configurations. You’ll be able to support end-point and root-port applications with blocks that implement the PHY-MAC, data-link, and transaction layer functionalities. With a seamless migration path to HardCopy IV ASICs, you can prototype your design in Stratix IV devices and move to HardCopy IV ASICs when you’re ready for volume production.

Key PCI Express hard IP advantages

- Close to zero logic elements (LEs) used
- \$0 list price
- Easy migration from soft IP-based solution
- No licensing required
- Timing closed block
- Faster design and compile times
- Substantial power savings compared to soft IP core with equivalent functionality

Hard IP architecture



1. Non-PCI Express cores e.g. XAUI, GbE, SRIO
2. Soft PCI Express IP protocol stack
3. Gen1 and Gen2 hard IP protocol stack

Soft logic PCI Express hard IP PCS/PMA

In above block diagram, the transceivers on the right can also be used for non-PCI Express applications. The interface to the hard IP block supports a PIPE 2.0-compliant interface. The hard IP PCI Express block offers support for end-point and root-port applications, and implements a complete protocol stack.

Stratix IV FPGA hard IP benefits and features

Advantages	Services
High-performance applications	<ul style="list-style-type: none">- PCI Express Gen1/Gen2-compliant protocol stack- x1, x4, and x8 initial link width configurations- Guaranteed timing closure across all targeted modes- Two to four hard IP cores per device- Low latency, cut through transmit path
No/low cost	<ul style="list-style-type: none">- ~Zero LEs used- No memory buffers used- No list price
Flexible and option rich	<ul style="list-style-type: none">- x2 mode supported through down configuration- 125- or 250-MHz application layer clock rate supported- Configurable maximum payload size (128, 256, 512, 1,024, and 2,048 bytes)- One or two virtual channels- 64-bit interface to application logic in all modes- Additional 128-bit interface in Gen1 x8 and Gen2 x4 and x8 modes
High-reliability applications	<ul style="list-style-type: none">- End-to-end cyclical redundancy check (ECRC) protection through entire protocol stack- Optional advanced error reporting- Extensive interrupt support

Want to dig deeper?

For more information about Altera's PCI Express hard IP solutions, please contact your local Altera sales representative or FAE, or visit www.altera.com/pciexpress. You can also download the user guide from our website.

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