

Altera wireless solutions

Simplify your RF card design cycle

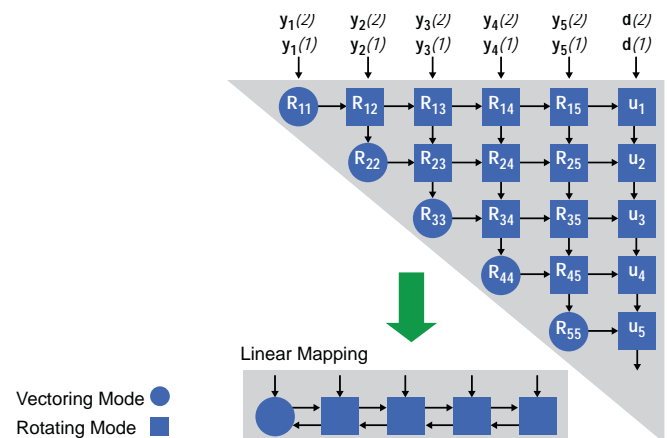
By integrating Altera® programmable logic devices (PLDs) into the core of your radio frequency (RF) cards, you gain flexibility and high performance, plus a risk-free migration path to low-cost structured ASIC technology. Ready for the rigors of digital signal processing (DSP), Altera programmable solutions along with our reference designs, intellectual property (IP) functions, and expertise can help you create your digital radio design from the ground up.

QR decomposition reference design

Altera supplies the reference design as clear-text VHDL, including a MATLAB bit-accurate simulation model

- Includes QR decomposition and back substitution
- Supports complex inputs with both fixed and floating point support
- Supports user defined matrix sizes
- Applications include matrix inversion, multiple-input multiple-output (MIMO) decoding, and digital predistortion
- Highly optimized design targeting efficient use of Stratix® II and Stratix III FPGA resources

QR decomposition

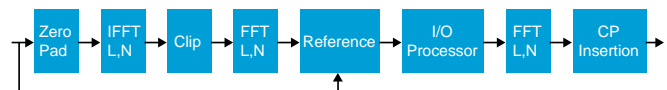


Crest factor reduction (CFR) reference design for OFDM

Altera supplies the reference design as clear-text VHDL, including a MATLAB bit-accurate simulation model.

- Support for orthogonal frequency division multiplexing (OFDM)-based systems including WiMAX and 3GPP Long-Term Evolution (LTE)
- Additional functionality includes OFDMA symbol modulation, digital upconverter (DUC) (4x interpolation), and cyclic prefix insertion
- Programmable mask for any environment
- Programmable error vector magnitude (EVM) budget
- Programmable channel bandwidths including 10 and 20 MHz
- Up to 5db peak-to-average power ratio (PAPR) improvement
- No receiver-side modification required

CFR



OBSAI and CPRI IP cores

Altera's wireless ecosystem partner offers Open Base Station Architecture Initiative (OBSAI) and Common Public Radio Interface (CPRI) IP cores based on the latest specifications of the standards.

Features

- OBSAI RP3-01 IP supports WCDMA, CDMA2000, and WiMAX end points, as well as remote radio head configuration
- CPRI IP is fully compatible with serial rates at 614.4 Mbps, 1.2288 Gbps, and 2.4576 Gbps
- Both OBSAI and CPRI IP cores are based on Stratix II GX FPGAs

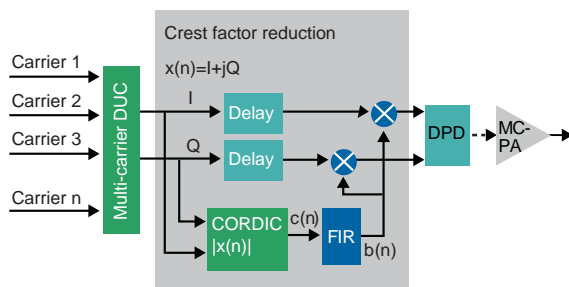
CFR reference design for CDMA systems

Altera's crest factor reduction (CFR) reference design for Code Division Multiple Access (CDMA) systems is the industry's lowest-cost solution to reduce the peak-to-average ratio of signals and improve power amplifier (PA) efficiency.

Features

- Parameterizable design with a DSP Builder-based-Simulink interface, enabling tradeoffs between EVM and ACLR
- Hardware-tested solution for CDMA2000 and W-CDMA signals
- Up to 5.5 dB peak-to-average ratio (PAR) reduction with 12 percent EVM degradation
- Consumes only 3,000 LEs and four 9x9 multipliers

Peak windowing-based CFR reference design



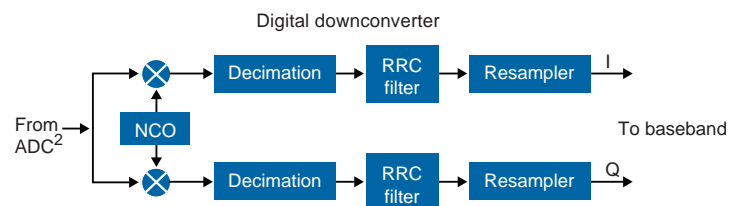
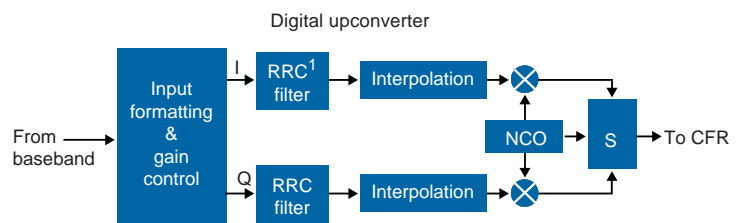
Digital upconverter and downconverter solutions

DSP Builder-based multi-channel and multi-antenna DUC and digital downconverter (DDC) reference designs for CDMA2000, WCDMA, and WiMAX systems demonstrate the lowest cost-per-channel implementations with Cyclone® III and Stratix III FPGAs.

Features

- Significantly reduced development time using DSP Builder design methodology and highly parameterizable IP MegaCore® functions
- Cost effectiveness through multi-channel filter design techniques
- Support for multiple transmit and receive antenna configurations
- Support for scalable channel bandwidths

Altera digital upconverter and downconverter solutions



¹ RRC = Root-raised cosine

² ADC = Analog to digital converter

Want to dig deeper?

To learn more about how Altera can help with your RF card design, contact your local Altera sales representative or FAE, or visit www.altera.com/wireless.

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