

# Arria GX FPGA Family Backgrounder

## Introduction

With the convergence of communications and computing technologies driving the adoption of 3-Gbps serial protocols in cost-sensitive markets, there is a growing need for low-cost FPGA solutions with transceivers for bridging endpoint applications. Until now, designers of cost-sensitive applications either had to use an application-specific standard product (ASSP) or a low-cost FPGA connected to an external PHY, and try to make those dissimilar devices communicate with each other. As a result, they'd face longer than required design times, unnecessary device costs, and additional board space requirements.

With the Arria™ GX family, Altera delivers a solution that enables a simplified transceiver-based design process for applications requiring serial I/O connectivity from 600 Mbps up to 3.125 Gbps. Additionally, the static power of Arria GX is reduced by up to 20 percent. Arria GX FPGAs allow designers to develop next-generation systems in the communications, broadcast, storage, computer, and industrial markets.

Arria GX FPGAs are backed by Altera's success and expertise in transceiver technology as well as a comprehensive portfolio of software tools, characterization reports, reference designs and verified intellectual property (IP) cores that meet compliance and interoperability. For system designers, this means minimized risk, faster development (and time-to-market), and a lower total cost-of-ownership.

## Arria GX FPGAs

The Arria GX family's embedded transceivers are based on the same transceiver technology used in the Stratix® II GX family, which means designers have access to proven transceiver technology with superior signal integrity characteristics. Signal integrity is extremely important in targeted Arria GX applications such as when a single device with integrated transceivers is needed for bridging several protocols, driving a network interface, or connecting to fast-switching parallel buses. Arria GX FPGAs utilize flip-chip packaging technology that provides superior signal integrity compared to wire-bond packages.

In the seven years since Altera introduced the industry's first FPGA with embedded transceivers, the company has built an unmatched support infrastructure to ensure that designers can take their ideas to production in the time and budget allocated. Hundreds of knowledgeable high-speed transceiver experts in Altera's field applications engineering (FAE) organization help integrate Altera® transceiver technology into customers' platforms seamlessly.

## Protocol Support

As part of the Arria GX family offering, Altera provides protocol solutions that simplify the design process and reduce time-to-market. The physical coding sublayer (PCS) blocks built into the Arria GX transceivers make designing for these protocols straightforward because they save valuable logic resources and simplify design. Each transceiver block includes dedicated circuitry to support PCI Express, SDI, Gigabit Ethernet, Serial RapidIO™, CPRI, OBSAI and XAUI. Altera also provides soft IP for protocols including PCI Express, SDI, Serial RapidIO standard, SerialLite II, and the ability to develop proprietary serial-based IP using Basic mode. Arria GX devices contain built-in word detection and alignment circuitry and built-in 8b/10b encoder/decoders, (which are bypassable when not required) making these devices suitable for both proprietary and protocol-based applications. Altera also provides protocol-specific design software, development boards, reference designs, and technical collateral (including board layout guidelines, characterization reports, and user guides).

Protocol	Data Rates (Gbps)
PCI Express Rev 1.1 (x1, x2, x4)	2.5
3G Basic (use for proprietary)	Up to 3.125
Serial RapidIO (x1, x4)	1.25, 2.5, 3.125
XAUI (IEEE 802.3ae)	3.125
Gigabit Ethernet (IEEE 802.3az)	1.25
CPRI/OBSAI	2.45 and 3.072
Standard and High-Definition Serial Digital Interface (SD and HD SDI)	0.27, 1.5, 3.0

## Transceiver Functions

Beyond support for a broad range of protocols, Arria GX transceivers also enable customers to develop solutions for backplane connections with channel equalization settings. Arria GX transceivers and software enable users to take advantage of the many transmit pre-emphasis and receive equalizations settings that allow developers to drive a 40-inch backplane.

## Applications

The combination of features, signal integrity, and support for key protocols in Arria GX devices enables the family to be used in a variety of wireless, wireline, broadcast, computer and storage, and industrial applications. For example:

*Wireline:* Arria GX FPGAs enable designers to connect new control-plane PCI Express-based processors to legacy modules and devices. Arria GX FPGAs also allow for 10-Gigabit Ethernet connections with the XAUI interface for pre-processing of Ethernet frames and connection to non-Gigabit Ethernet-ready devices.

*Wireless:* Digital signal processing (DSP) blocks are often incapable of supporting all of the computing power required by baseband modems that use newer orthogonal frequency division multiplexing (OFDM)-based standards like WiMAX. In these instances, only FPGAs provide a cost-effective way to complement DSP blocks. With the standardized Serial RapidIO interface found on Arria GX devices, it is easy to connect an FPGA fabric to a DSP block.

*Broadcast:* Arria GX FPGAs can be used as a connection for broadcast equipment by using transceiver support for triple-rate SDI up to 3 Gbps. Broadcast system builders can take advantage of the excellent signal integrity in the Arria GX transceivers to build solutions today.

*Computer and storage:* Arria GX FPGAs can be used to bridge devices that don't natively interface with PCI Express and the broad base of PC designs that revolve around PCI Express buses. For example, most medical imaging equipment sold today uses an embedded PC platform for final processing and display of the patient examination. The scanner head usually sports a proprietary interface and the data it sends needs to be pre-processed and fed to the PC on the standard PCI Express bus.

*Industrial:* Gigabit Ethernet is becoming an interface of choice for industrial control equipment. Historically, industrial controllers were either untethered or provided simple connectivity to a central processing unit via a proprietary protocol. The ubiquity of Ethernet is now pushing industrial control companies to provide simpler ways to make existing designs network via interfaces like Gigabit Ethernet over unshielded twisted-pair cable or fiber optic. Old designs can be enhanced to talk to other Gigabit Ethernet appliances with the simple addition of the Arria GX solution.

## **Product Details**

Arria GX devices are built on TSMC's production-qualified, 1.2V, 90-nm, 9-layer-metal process technology. Arria GX devices use a low-k dielectric and are manufactured on 300-mm

wafers. The family is comprised of five members ranging from 21,580 to 90,220 logic elements (LEs), with up to 4.5 Mbits of embedded memory, up to 176 embedded 18-bit x 18-bit multipliers, and between 4 and 12 transceiver channels running up to 3.125 Gbps. The family's architecture is based on the same adaptive logic module (ALM) fabric found in Stratix II and Stratix II GX FPGAs.

### Arria GX Family Overview

Device	Transceiver Channels	Equivalent LEs	Total Memory Bits	DSP Blocks	Phase-Locked Loops (PLLs)
EP1AGX20	4	21,580	1,229,184	10	4
EP1AGX35	4	33,520	1,348,416	14	4
	8				
EP1AGX50	4	50,160	2,475,072	26	4
	8				4, 8
EP1AGX60	4	60,100	2,528,640	32	4
	8				8
	12				8
EP1AGX90	12	90,220	4,477,824	44	8

### Package and Maximum User I/O Pins

Device	F484 (23-mm) User I/O Pins	F780 (29-mm) User I/O Pins	F1152 (35-mm) User I/O Pins
EP1AGX20	246	340	
EP1AGX35	246		
		340	
EP1AGX50	238		
		344	514
EP1AGX60	238		
		344	
			538
EP1AGX90			538

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