

# Arria GX Family Press FAQ

## **What is the Arria™ GX FPGA family?**

The Arria GX family is comprised of Altera's 90-nm low cost, transceiver-based FPGAs. The devices are optimized for the mainstream serial protocols from 600 Mbps up to 3.125 Gbps. Five family members range from 21,580 to 90,220 logic elements (LEs). The Arria GX family is backed by a comprehensive portfolio of software tools, intellectual property (IP), system models and reference designs.

## **What is unique about Arria GX FPGAs?**

For cost-sensitive, transceiver-based, high-volume applications, the Arria GX FPGA family provides:

- Minimized risk with proven transceiver technology evolved from Stratix® II GX FPGAs
- A reduction in static power of up to 20 percent
- Robust flip chip technology to ensure the signal integrity requirements of the target applications are met
- Comprehensive protocol support infrastructure including software tools, characterization reports, IP, system models and reference designs

## **What are the benefits of designing with Arria GX devices?**

Arria GX devices provide the right balance of I/O and transceiver performance, a lower total cost of ownership, and support for mainstream serial protocols, PCI Express x1 and x4, Gigabit Ethernet, Serial RapidIO® standard, XAUI, SDI, CPRI, OBSAI, SerialLite II, and the ability to develop proprietary serial-based IP using Basic mode.. The Arria GX family was built to minimize risk for those applications requiring an inexpensive way to connect dissimilar devices and modules serially. It provides superior signal integrity and is backed by the vast support infrastructure built by Altera since the introduction of Mercury™ devices in 2000. Designers choosing Arria GX devices also benefit from the highest productivity and most complete set of tools available in the FPGA industry. Altera's large network of field and factory application engineers, and long history of on-time delivery for high-volume 90-nm process technology, help customers confidently get their designs to market.

## **Tell me more about the functionality of the Arria GX family.**

The Arria GX FPGA family consists of five family members supporting serial data rates of up to 3.125 Gbps. The devices come with:

- Up to 90,220 LEs
- Up to 12 transceiver channels
- Up to 4.5 Mbits of embedded memory
- Up to 44 digital signal processing (DSP) blocks
- Support for SDR, DDR, and DDR2 memory interfaces
- Three different-sized, robust flip chip packages

## **What process technology is used to manufacture Arria GX devices?**

Arria GX devices are based on a production-qualified, 1.2V, 90-nm, 9-layer-metal process technology from TSMC. Arria GX devices use a low-k dielectric and are manufactured on 300-mm wafers.

## **What protocols are supported by the Arria GX family?**

The Arria GX family has been optimized to support mainstream serial protocols: PCI Express (x1 and x4), Gigabit Ethernet, Serial RapidIO standard, XAUI, SDI, CPRI, OBSAI, Serial Lite, and Basic (for serial protocol development) protocols up to 3.125 Gbps. Arria GX FPGAs include hardware blocks for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA). Higher protocol stack layers can be implemented in the FPGA fabric simply and inexpensively with the help of Altera® megafunction IP cores.

## **Why did Altera choose to support these protocols with Arria GX FPGAs?**

### *PCI Express (x1 and x4)*

The interface of choice in many applications, driven by the PC market explosion, PCI Express is becoming pervasive in the digital design domain. Single-board computers, for example, are the foundation of numerous systems in markets such as medical imaging, storage, and industrial control.

### *Gigabit Ethernet*

Building on the ubiquitous Ethernet protocol, Gigabit Ethernet is increasingly popular in markets such as wireline and industrial. As bandwidth-demanding applications continue their surge—even appearing in the small office-home office (SOHO) market—the use of Gigabit Ethernet looks to become more widespread.

### *Serial RapidIO*

Most popular DSP devices include Serial RapidIO interfaces. As FPGAs continue to demonstrate their value in offloading complex tasks where parallel computation is critical, there will be more designs using an FPGA as a coprocessor to a DSP device. This should be especially true in markets like imaging and wireless communications.

### *XAUI*

Building on the ubiquitous Ethernet protocol and the increasing demand for 10-Gbit Ethernet, XAUI is increasingly popular in markets such as wireline. As bandwidth-demanding applications continue their surge, the use of XAUI looks to become more widespread.

### *SDI*

SDI is the interface of choice in many broadcast applications. This market explosion is driven by the need for serial interconnect. SDI is becoming pervasive in the digital design domain.

### *CPRI/OBSAI*

The wireless market for remote radio heads continues to expand, with a significant need for, robust, reliable transceivers to drive the CPRI and OBSAI interfaces. As FPGAs continue to demonstrate value by adding function integration, enabling flexibility of design, and providing excellent transceiver serial I/O signal integrity, the wireless market has realized the advantages of FPGAs. To fully support this market Arria GX device supports CPRI and OBSAI standards.

### *Basic Mode*

Building systems with serial I/O connections may require a proprietary or derivative protocol, which Arria GX device now supports. Basic mode allows customers to develop this proprietary or derivative serial protocol for their applications.

### **How did you reduce the static power by 20 percent in Arria GX?**

The static power of Arria GX is reduced by 20 percent by tightening the existing 90-nm manufacturing process. It is routine for Altera to continually refine the manufacturing process for all our products to provide benefits to our customers.

### **Will the Early Power Estimator (EPE) be updated to reflect this power reduction?**

Yes, it will be in the next release of Altera's Quartus II development software.

### **What applications do Arria GX FPGAs enable?**

Please refer to the backgrounder for examples of new applications enabled by Arria GX FPGAs.

### **Tell me more about how customers can start designing with Arria GX devices today.**

Designers can begin their Arria GX designs today by downloading and installing Quartus® II development software version 7.1. The production-qualified Arria GX devices are shipping now.

With the new version of the easy-to-use Quartus II software, Altera delivers the lowest development cost and fastest time to design completion to ensure a smooth and successful design flow. The Quartus II software also integrates seamlessly with leading third-party synthesis and simulations tools. Customers can download the Subscription Edition and free Web Edition of the Quartus II software at [www.altera.com/download](http://www.altera.com/download).

### **How does the Arria GX family compare to the Stratix II GX family?**

The Arria GX and Stratix II GX families share the transceiver technology developed by Altera over the past seven years. The Arria GX transceiver is essentially a subset of the Stratix II GX transceiver but optimized for mainstream protocols up to 3.125 Gbps. This is why only one speed grade is necessary with this family. Arria GX devices, like Stratix II GX devices, use flip chip packages to provide the signal integrity that is so critical in target applications. The family also offers smaller packages (F484) than demanded by applications where Stratix II GX devices are used and where large I/O counts are necessary. The Stratix II GX family offers additional features not available with the Arria GX family including calibrated on-chip termination and support for several other protocols.

Device Family	Arria GX FPGAs	Stratix II GX FPGAs
Logic density	21K to 90K LEs	34K to 133K LEs
Logic fabric	ALM	ALM
Performance index	1.0	1.35
Transceiver channels	4 to 12	4 to 20
Transceiver data rate	600 Mbps to 3.125 Gbps	0.27 to 6.375 Gbps
LVDS data rate	840 Mbps	1 Gbps
Total RAM bits	1.2 to 4.5 Mbits	1.4 to 6.7 Mbits
DSP blocks	10 to 44	16 to 48
18x18 multipliers	40 to 176	64 to 252

Max user I/Os	246 to 538	361 to 734
Packages	F484, F780, F1152	F780, F1152, F1508
128-bit AES design security	No	Yes

### **How does the Arria GX family compare to the Cyclone® FPGA series?**

The Cyclone III family is optimized for low cost. It provides low power and high functionality without compromising cost. Customer needs for transceiver-based designs, where signal integrity and I/O performance are key, call for a different solution, as provided by Arria GX devices. The Arria GX family offers proven support for mainstream transceiver-based protocols at the lowest price available to serve bridging and coprocessing applications.

### **What is the price for the Arria GX family?**

Prices start at US\$50 for the EP1AGX50CF484C6 device in 25K unit volume. Volume production began in the third quarter of 2007.

### **Which third-party tools support Arria GX devices?**

Synthesis and simulation tools from leading EDA vendors, including Cadence, Mentor Graphics, Synopsys, and Synplicity, support the Arria GX family, ensuring the highest quality of results in Altera devices.

### **What IP cores are available for Arria GX devices?**

Along with the popular Nios® II family of embedded processors, Altera offers off-the-shelf IP cores optimized for Arria GX devices, along with an extensive library of IP cores available for all Altera FPGAs. More information is available at the Altera IP Megastore website at [www.altera.com/products/ip](http://www.altera.com/products/ip).

### **Will Altera support migration of Arria GX devices to HardCopy® ASICs?**

The Arria GX device is a midrange FPGA with transceivers and would not realize significant cost reductions through conversion to a HardCopy ASIC.

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