

MAX IIZ Press FAQ

Product and Company

Q. What is the MAX IIZ CPLD device family?

A. MAX IIZ CPLDs are Altera's new zero-power CPLDs and are the latest addition to Altera's low-power portfolio. Targeted at portable applications, MAX IIZ CPLDs deliver significant advantages in the three critical constraints that portable applications designers care most about—power, space and price. MAX IIZ devices are available in two densities (240 LEs and 570 LEs), four packages (5x5 mm, 6x6 mm, 7x7 mm, and 11x11 mm), I/O counts from 54 to 260, and power consumption as low as 29 μ A.

Q. What is unique about MAX IIZ CPLDs?

A. Altera's new zero-power MAX IIZ CPLDs are extremely low-power versions of the MAX II low-cost CPLD devices. MAX IIZ devices break through the power, space and cost limitations of traditional macrocell-based CPLDs by combining non-volatility and instant-on performance with an innovative look-up table (LUT) logic structure. MAX IIZ devices are optimized for portable applications and enable designers to use MAX IIZ devices as replacements for low-density FPGAs, ASSPs, and standard logic devices.

Q. The MAX IIZ device has an FPGA architecture, so why is it called a CPLD?

A. Labeling the MAX IIZ devices as FPGAs would accurately describe the functionality and application of the devices. The MAX IIZ devices are an instant-on, non-volatile, low-cost, single-chip solution, which is what most designers think of as a CPLD.

Q. Tell me more about the functionality of the MAX IIZ family.

A. Altera's new MAX IIZ devices are the newest members of the low-cost MAX II CPLD family. All MAX II devices combine non-volatility and instant-on performance with an innovative LUT logic structure. The new zero-power MAX IIZ device makes all of this available at the industry's lowest power consumption. The result is that designers of low-power portable applications now have an unprecedented degree of cost-effective functionality at their disposal.

Q. What are the benefits of designing with MAX IIZ devices?

A. The zero-power MAX IIZ CPLDs bring the benefits of programmable logic—fast design times, flexibility and board-level integration—to portable application designers. The low standby power, small package size and unique features of MAX IIZ devices make them ideal for power- or space-constrained portable applications such as smart phones and other handheld devices.

Q. How do MAX IIZ devices achieve low power consumption?

A. The ultra-low power consumption of the MAX IIZ devices is a result of innovative engineering to reduce standby current of the low-voltage power on reset circuitry, and to raise the voltage threshold of the transistors, in order to reduce leakage.

Q. What process technology is used to manufacture MAX IIZ devices?

A. MAX IIZ devices are manufactured on the same process as the rest of the MAX II device family—a cost-optimized 1.8V, 0.18- μ m, 6-metal-layer flash process from Taiwan Semiconductor Manufacturing Company (TSMC).

Q. When will the first MAX IIZ devices be available?

A. Production silicon will be available in the first quarter of 2008.

Q. How do MAX IIZ devices compare to the MAX II family?

A. The MAX IIZ device is a zero-power version of MAX II CPLDs. It consists of two devices, the EPM240Z and the EPM570Z. It will be available in four MBGA packages (0.5-mm pitch): M68 (54 I/Os), M100 (80 I/Os), M144 (116 I/Os) and M256 (160 I/Os).

Q. How do MAX IIZ devices fit in the Altera product portfolio?

A. The MAX IIZ devices are part of the MAX II CPLD family and address the needs of designers looking for the lowest power consumption, smallest packages and lowest price. Altera offers a complete line of low-power solutions including Stratix[®] III and Cyclone[®] III FPGAs, HardCopy[®] structured ASICs and MAX IIZ CPLDs.

Q. What intellectual property (IP) cores will be available for MAX IIZ devices?

A. Along with the popular Nios[®] II family of embedded processors, Altera offers off-the-shelf IP cores optimized for the MAX II family, along with an extensive library of standard IP cores. Each core has been specifically optimized to take advantage of the architectural features of the MAX II family. More information is available at the Altera IP MegaStore[™] website at www.altera.com/products/ip.

In addition, over 20 design examples have been created to meet the specific needs of portable applications. More information on the portable applications design examples is available at www.altera.com/max2example.

Q. Tell me more about how customers can start designing with MAX IIZ devices today.

A. Designers can begin their MAX IIZ designs today by downloading and installing the free Quartus[®] II Web Edition software version 7.2, SP1. With this new version of the easy-to-use Quartus II software, Altera delivers the lowest development cost and fastest time to design completion to ensure a smooth and successful design flow. The Quartus II software also integrates seamlessly with all leading third-party synthesis and simulation tools. Customers can download the subscription edition and web edition of the Quartus II software at www.altera.com/download. Active Altera software subscribers will also receive the Quartus II software soon as shipments begin.

Q. What is the price for MAX IIZ devices?

A. The EPM240Z M68 will be US\$1.25 in high volumes (1M)

Q. What packages are available for the MAX IIZ devices?

A. MAX IIZ devices are available in four MBGA packages (0.5-mm pitch): M68 (54 I/Os), M100 (80 I/Os), M144 (116 I/Os), and M256 (160 I/Os).

Markets and Applications

Q. What applications do MAX IIZ CPLDs enable and how?

A. MAX IIZ CPLDs are ideal for portable applications, which have a need for low power consumption, small packages and low price. MAX IIZ CPLDs are a cost-effective, low-power solution for general-purpose functions such as GPIO pin expansion, interfacing and peripheral control. In addition, MAX IIZ CPLDs can be used as power reduction coprocessors, allowing many system tasks to be offloaded from a large power-hungry ASSP to a small, power-frugal MAX IIZ CPLD. More information on using MAX IIZ CPLDs to reduce power is available at www.altera.com/literature/wp/wp-01042-using-zero-power-cplds-to-lower-power-in-portable.pdf.

Q. What are the benefits of programmable logic in high volume applications?

A. Many high-volume applications, such as smart phones and other consumer products, have a need to create and develop the maximum number of features in the minimum amount of development time. In order to accomplish this, designers make extensive use of ASSP chipsets. However, this can make it difficult to build differentiated products, because if everyone uses the same chipsets, all products begin to look alike. MAX IIZ CPLDs provide a fast, low-risk method to customize standard chipsets, by either creating a new feature, or modifying an existing feature. More information on using MAX IIZ CPLDs in high-volume applications is available at www.altera.com/literature/po/ss-maxiizhandset.pdf.

Competition

Q. How do MAX IIZ devices compare with the competition?

A. MAX[®] IIZ devices offer up to six times the logic and three times the I/Os in the same package sizes as traditional macrocell-based CPLDs. This translates into an ability to pack more functionality into the same PCB real estate, something portable applications designers are always looking to do.