

Nios II Embedded Processor Backgrounder

Introduction

The Nios[®] II family of soft-core processors is Altera's second-generation embedded processor for FPGAs. With over 200 DMIPs of performance in designs targeting the Stratix[®] II family of high-performance FPGAs, the Nios II family delivers mainstream performance to address a broad range of embedded applications. The Nios II family consists of three members – fast, economy and standard – each optimized for a specific price and performance range. All three cores use the same instruction set architecture (ISA) and are 100% binary code compatible. Nios II processors can be added to a designer's system using the SOPC Builder system development tool now featured in the Quartus[®] II development software.

Table 1: Key features of the Nios II family members

	Nios II /f Fast	Nios II /s Standard	Nios II /e Economy
Pipeline	6 Stage	5 Stage	None
Multiplier *	1 Cycle	3 Cycle	None
Branch Prediction	Dynamic	Static	None
Instruction Cache	Configurable	Configurable	None
Data Cache	Configurable	None	None

*Uses digital signal processing (DSP) blocks in Stratix and Stratix II FPGAs

Building on Success

With more than 13,000 Nios development kits shipped since its introduction in 2000, the first-generation, 16-bit Nios processor set the standard for soft-core processors targeting FPGAs. Named by *EDN* magazine as one of its "Hot 100 Products of 2003" and ranked in CMP's annual Embedded Market Study among the top 10 16-bit processors designers are considering using in their next design, the Nios processor has proven itself many times over in applications ranging from fish finders to advanced communications sub-systems.

As part of the Nios II product definition process, Altera engaged in hundreds of interviews with software developers, hardware engineers, and systems architects around the world. Based on those interviews, Altera was able to validate and fine-tune its embedded strategy, developing a new CPU architecture to address three key customer requirements: increased processor performance, decreased logic usage, and enhanced software development tools. The resulting 32-bit Nios II embedded processor offers higher performance, world-class software development tools, and even more flexibility, while using less of the FPGA device's resources. Altera's next-generation soft processor solution allows customers to use Nios technology while maintaining their existing C language application code. The tools delivered with the Nios II development kit provide a push-button migration path for C-based designs from Nios to Nios II processors.

The Nios II family of processors can be used in Altera's Stratix and Cyclone[®] series of FPGAs. When used in low-cost Cyclone (and upcoming Cyclone II) FPGAs, designers have access to one of the industry's most cost-effective processors for a wide range of high-volume applications. For high-performance applications, the Nios II processor is optimized to take full advantage of the DSP blocks, on-chip memory, and other features of the Stratix and Stratix II families. The cost of Nios processor-based designs targeting the Stratix and Stratix II device families can be reduced for high-volume applications by migrating to Altera's HardCopy[®] structured ASICs.

Reduced Logic Usage

Many developers can benefit from a compact CPU (e.g., 500 – 800 logic elements) to provide basic control and/or housekeeping functionality. A smaller CPU is easier to fit in a low density/low-cost Cyclone FPGA and still leave enough room for other system functions. Other advantages of a smaller CPU core include:

- **Multiple Processor Implementations:** A smaller CPU makes it easier to use multiple processors in a single FPGA. Many customers have created Nios designs in which several processors are used in a single device, each assigned to a specific (and sometimes unrelated) task. Iris Technologies, for example, created a network

processor design in which up to 4 Nios processors are used to handle forwarding, header processing, traffic management, and switch fabric management.

<http://www.panapress.com/newswire.asp?code=665>

The Ultimate in Versatility

Altera’s Nios II family of soft processors enables developers to choose from an unlimited combination of system configurations to provide an exact fit for their embedded needs. Developers using Nios II processors can choose from more than 60 peripherals to get the exact processor, peripheral, and interface mix required without having to pay for silicon features they will never use. With the Nios II soft processor solution, customers can choose the size and performance of their core, select their FPGA based on cost and performance requirements, implement multiple processor cores, and accelerate instructions in hardware.

Table 2: Nios II Performance & Price Implemented Across Altera’s FPGAs

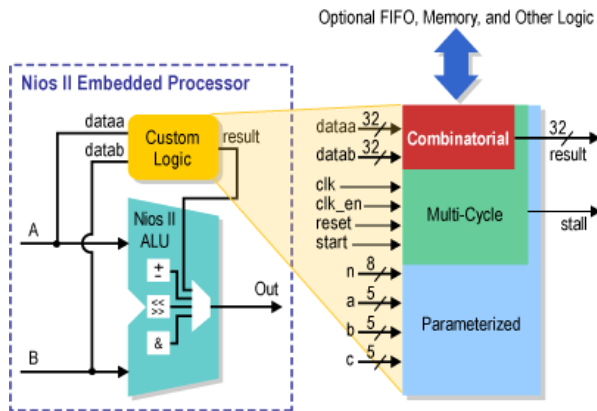
Device Family	DMIPS Performance (/e, /s, /f)	Cost of Logic (CPU)
Stratix II	31, 128, 220	\$0.90 to \$1.90
Stratix	22, 97, 165	\$1.40 to \$4.60
Cyclone	17, 54, 92	\$0.35 to \$1.60
HardCopy	24, 103, 167	\$0.36 to \$1.20

Accelerating Software Algorithms

To boost system performance, the Nios II processor supports 256 custom instructions with fixed or variable clock-cycle operations that designers can use to accelerate time-critical sections of code. These custom instructions, shown in Figure 1, allow designers to implement compute-intensive algorithms in hardware and “call” them in software just like a C language subroutine. By contrast, the original Nios processor supports 5 custom instructions, each of which must have a predetermined number of clock cycles per execution. While some ASIC-targeted processor cores provide custom instruction and/or hardware accelerators, none can deliver working, shippable, silicon as quickly or at the low

development cost as Nios II processors in an Altera® FPGA.

Figure 1: Block diagram view of custom instruction implementation in the Nios II CPU



Performance Made Easy

The Avalon™ switch fabric, used by the Nios II family, enables multiple data transactions for unmatched system throughput performance. Introduced with the first-generation Nios processor, the Avalon switch fabric provides a set of pre-defined signal types with which a user can connect any number of more than 60 available peripherals. The SOPC Builder system development tool automatically generates the Avalon switch fabric logic, which includes capabilities for data-path multiplexing, address decoding, wait-state generation, dynamic bus sizing, interrupt-priority assigning, and advanced switch fabric transfers. Users can easily integrate their own IP blocks and peripherals with the rest of their Nios II processor-based system using the SOPC Builder Import Wizard. The Avalon switch fabric requires minimal FPGA resources and provides fully synchronous operation.

Hardware Acceleration

Large blocks of data can be processed concurrently to CPU operation by adding application-specific hardware accelerators. The Avalon switch fabric provides a flexible interconnect path that allows multiple cores (e.g., CPU and accelerator) to read and write data simultaneously using dedicated data paths, dramatically boosting system throughput. For example, a hardware accelerator for calculating cyclic redundancy counts, typical in network communication, can achieve two orders of magnitude performance boost

compared with processing the data in software alone. Processing a 64-Kbyte block of data can take several million clock cycles in software, hundreds of thousands of clock cycles with a custom instruction, and tens of thousands of clock cycles using a hardware accelerator, as shown in Figure 3.

Figure 2: Hardware accelerator implementation with the Avalon switch fabric

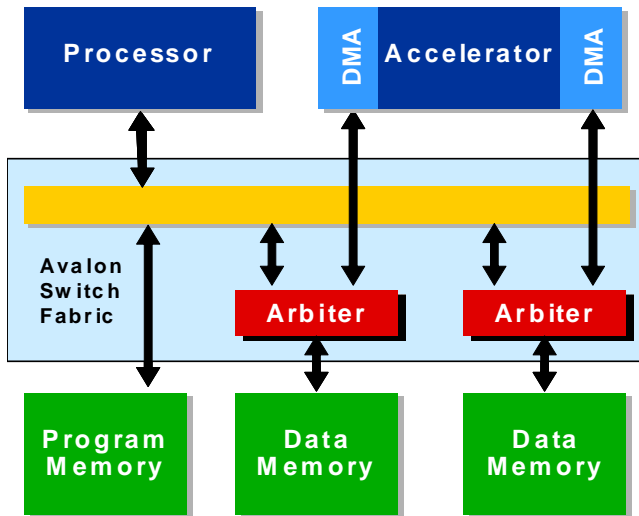
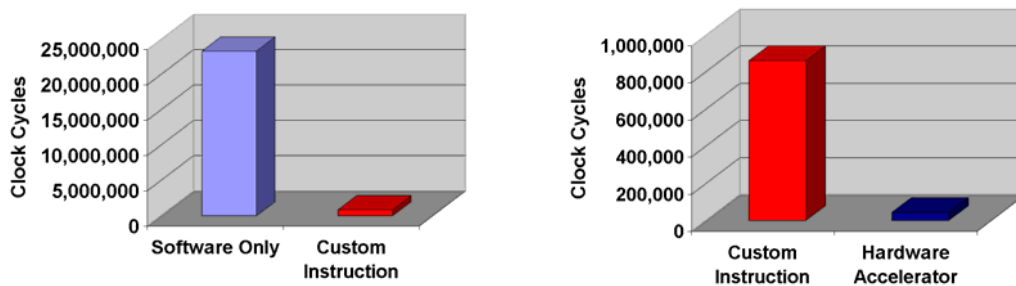


Figure 3: Reduce Clock Cycles with Hardware Accelerator



Comprehensive Development Tool Support

Nios II processors are supported by the Nios II integrated development environment (IDE), a complete set of robust development tools for software engineers. Based on the open-source Eclipse **project**—also chosen by *EDN* as a Hot 100 Product of 2003 — the Nios II IDE supports plug-in feature enhancements such as OS integration, performance analysis tools, and a complete set of development tools needed by today’s embedded designer:

- Project Manager
- Editor
- Compiler
- JTAG Debugger
- Flash Programmer

Real-Time Operating System Support: The Nios II development kits include two third-party real time operating systems (RTOSs) and a TCP/IP stack for network-based applications:

MicroC/OS-II (Micrium): This is a complete, portable, ROMable, preemptive real-time kernel that includes full source code, printed reference manual, and free developer license. MicroC/OS-II has been certified by the FAA for use in safety-critical avionics equipment. <http://ucos-ii.com/>. Customers can purchase shippers licenses for only \$2,985 which entitles them to the following:

- License for 3 developers to create as many designs as they wish for 1 year using MicroC/OS-II
- Perpetual license to support designs created during the subscription period (i.e. fix bugs, minor modifications).
- Additional subscription license seats may be purchased for \$995 per developer.

Nucleus Plus (ATI / Mentor): Nios II processors ship with an evaluation version of Accelerated Technology's source-available, royalty-free, Nucleus Plus RTOS kernel. This evaluation software lets Nios II users create Nucleus-based applications and run them on a development board (for a limited amount of time). Full developer licenses are available from ATI / Mentor Graphics. <http://www.mentor.com/nucleus/>

Lightweight IP TCP/IP Stack: Nios II development kits ship with an open-source TCP/IP stack that can be used with MicroC/OS-II applications. The software is made available, as shipped, as source code with documentation, reference designs, and support from Altera.

Developers can create RTOS-based applications from within Nios II IDE using either of the included RTOS products. Open-source software, including the μ CLinux operating system, will be available free for download from the web.

Pricing and Availability

All active Nios subscribers will automatically receive a Nios II update. Nios developers with inactive subscriptions can receive this and 12 months of updates by for only \$495. The Nios II embedded processor is royalty free when used in Altera FPGAs and HardCopy devices. An ASIC license for OEM applications is available for an additional charge. For more information, visit www.altera.com/nios2. Customers can place their orders for the Nios II development kit by contacting their local Altera sales representative.