



Stratix GX Overview

Introduction

Today's high-speed applications need a reliable data transfer technology that gets information from source to destination fast. To meet this need, Altera introduces the Stratix™ GX device family, a powerful fusion of 3.125-Gbps transceiver technology with the industry's fastest FPGA architecture. Stratix GX devices are the culmination of years of experience in high-speed digital design, giving system architects in the broad marketplace—from communications to high-end consumer electronics to mass storage systems—a low-risk path to 3.125-Gbps transceiver applications.

Carrying forward the concept of integrated transceiver technology that Altera first brought to the FPGA market with the Mercury™ device family, Stratix GX devices include up to 20 full duplex transceiver channels capable of operating at up to 3.125 Gbps while consuming minimal power. Designers seeking to implement specific interface protocols such as 10 Gigabit Ethernet XAUI or customized functions that require data rates up to 3.125 Gbps and a high-performance FPGA need look no further than Stratix GX devices.

Gigabit Transceiver Blocks

The embedded transceiver blocks in Stratix GX devices receive and transmit data using techniques common with many emerging interfaces that require clock data recovery (CDR) technology. Each transceiver block features four full-duplex channels to serialize, encode, and synchronize data for transmission between the external environment and the Stratix GX device channels. Stratix GX devices support numerous emerging protocols including 10 Gigabit Ethernet XAUI, Gigabit Ethernet, InfiniBand, and SONET/SDH. A seamless interface with the programmable logic array ensures reliable data transfer, maximized data throughput, and simplified timing analysis.

Table 1. CDR-Based Data Transmission Protocols Supported by Stratix GX Devices

Bus Transfer Protocol	Typical Number of Data Channels	Data Rates (1)
SONET/SDH	4 to 16	2.488 Gbps
10 Gigabit Ethernet XAUI	4	3.125 Gbps
Gigabit Ethernet	1	1.25 Gbps
Infiniband	1,4, or 12	2.5 Gbps
2G Fibre Channel	1	2.125 Gbps
1G Fibre Channel	1	1.0625 Gbps
RapidIO (Serial)	1	1.25, 2.5, 3.125 Gbps
PCI Express	16	2.5 Gbps
SMPTE 292M	1	1.485 Gbps
SFI-5 / SPI-5	17-18	3.125 Gbps

Note to Table 1:

1. Stratix GX devices support up to 3.125-Gbps data rates.

Dynamic Phase Alignment

Stratix GX devices are equipped with source-synchronous I/O channels capable of up to 1-Gbps performance, providing sufficient bandwidth to complement data flow from the transceiver blocks. To simplify board-level issues associated with source-synchronous signaling at these data rates, Altera incorporated dedicated dynamic phase alignment (DPA) circuitry -- a first in the FPGA industry. The DPA circuitry continuously removes channel-to-channel and clock-to-channel timing variations introduced by unmatched board trace lengths, jitter, and other skew-inducing effects. Advanced, source-synchronous bus transfer protocols such as SPI-4.2 that do not use clock data recovery (CDR) signal transmission techniques often require DPA.

Table 2. Source-Synchronous Signaling Based Protocols Supported in Stratix GX Devices

Interface Protocol	Typical Number of Data Channels	Data Rate
SPI-4 Phase 2	16	1 Gbps
HyperTransport™	2,4,8,16, or 32	800 Gbps
RapidIO™ (Parallel)	8 or 16	1 Gbps
CSIX Streaming	8 or 16	1 Gbps
10 Gigabit Ethernet XSBI	16	644 Mbps

Key Features

Offering significant performance increases over previous generation architectures and unrivaled logic and memory density, the Stratix device architecture provides the basis upon which Stratix GX devices are built. All of the same innovative features included in the Stratix device family are available in Stratix GX devices. These features include:

- Abundant TriMatrix™ memory resources for on-chip storage.
- Extensive phase-locked loops (PLLs) and clock management circuitry. With up to 8 PLLs and up to 40 unique system clocks per device, Stratix and Stratix GX devices are built to function as a central clock manager.
- DSP blocks. DSP blocks eliminate performance bottlenecks in cross bar switches and other DSP applications commonly found in multiplier-only implementations.
- Terminator™ technology. Terminator technology simplifies board design and reduces board space by minimizing the number of external resistors required on a printed circuit board (PCB).

For a complete description of the entire Stratix GX feature set, please see the Altera web site at www.altera.com.

Packaging & Availability

The Stratix GX device family includes seven members ranging in density from 10,570 to 41,250 logic elements (LEs). Up to twenty 3.125-Gbps transceiver channels are available on each Stratix GX device in each of three different speed grades. The first available device, the EP1SGX25F, includes 25,660 logic elements (LEs) and sixteen 3.125-Gbps transceiver channels and will be available in Q1 2003. All family members will be shipping in the first half of 2003.