

Stratix II Product Backgrounder

Introduction

Continuous innovation in today's electronic systems is requiring increasingly advanced, more flexible silicon solutions to meet evolving system requirements. Combined with the increasing cost of chip development, FPGAs are today quickly becoming the de facto platform for system design in the data communications, telecommunications, wireless, consumer, medical, industrial, and military markets. Unlike ASICs and ASSPs, Altera's new Stratix™ II family of devices--the industry's biggest and fastest FPGAs--deliver a low-risk and highly cost-effective means to get even the most complex design to market.

Stratix II High-Density High-Performance FPGAs

Altera's new high-density, high-performance Stratix II FPGAs are the industry's latest, most advanced FPGAs. The Stratix II family's innovative new architecture is based on a unique logic structure made up of adaptive logic modules (ALMs), dramatically increasing performance and efficiency. Built on TSMC's 90-nm, all-copper process, using low-k dielectric material on 300-mm wafers, Stratix II FPGAs allow designers to conserve device resources by packing more functionality into a smaller area. As a result, Stratix II devices offer more than double the logic density and 50 percent higher performance at 40 percent lower cost than first-generation Stratix devices.

The new logic structure allows logic to be shared among adjacent logic functions, delivering efficient logic utilization and high performance. With up to eight inputs to the combinational logic block, one ALM can implement up to two independent functions, each of varying widths, including any function of up to six inputs and certain seven-input functions. This optimized utilization significantly reduces logic resource requirements. Comprised of a unique mix of combinational, arithmetic, and register logic, an ALM is 2.5 times more powerful than the original Stratix logic element. ALMs deliver more logic capacity in a smaller physical area which equates to lower cost.

Stratix II FPGAs include all the popular and powerful system-level features, such as hard digital signal processing (DSP) blocks and TriMatrix™ memory, from the highly successful, award-winning Stratix FPGA family. Supporting internal clock frequency

rates of up to 500 MHz and typical design performances of over 250 MHz, Stratix II devices provide designers with ASIC-like performance combined with the time-to-market advantages of programmable logic. In addition, Stratix II devices include new features, such as advanced encryption standard (AES)-based design security technology, dynamic phase alignment (DPA) circuitry, and support for new external memory interfaces.

For high-volume designs, Stratix II devices will be available in Altera's HardCopy™ structured-ASIC version. HardCopy devices deliver additional increases in performance and reduced power consumption, at a significant risk reduction and cost savings. The HardCopy design methodology provides volume-driven customers with a unique prototype-to-production solution not offered by any other semiconductor company.

Key Features

Stratix II FPGAs offer several system-level features to meet the needs of the marketplace.

- **Memory Bandwidth:** Seventy-five percent of FPGA designs interface to external memory devices. As data throughput requirements grow, advanced high-performance memory devices such as DDR2 SDRAM, QDR II SRAM, and RLDRAM II devices, with their associated stringent timing budget requirements, are increasingly being incorporated in such systems. Recognizing that FPGAs will need to interface with these advanced memories, Altera specifically designed the Stratix II family to provide designers with easy-to-implement interfaces compatible with 533-Mbps DDR2 SDRAMs, 800-Mbps QDR II SRAMs, 600-Mbps RLDRAM II devices, 400-Mbps DDR SDRAMs, 668-Mbps QDR SRAMs and 166-Mbps SDR SDRAMs. This external memory interface support complements the abundant on-chip TriMatrix memory available in Stratix II devices.
- **On-Chip Memory:** Typical systems require on-chip memory capabilities for system cache, data buffering, clock domain translation, and FIFO applications. Stratix II devices offer up to 9 Mbits of on-chip memory through TriMatrix memory, which supports 512-bit M512, 4-Kbit M4K, and 512-Kbit M-RAM blocks, each of which can be configured to support a wide range of features. With up to 370-MHz

performance, TriMatrix memory provides more efficient access to stored data for applications requiring fast access times.

- **High-Speed Data Transfer:** With the evolution of high-speed transmission technologies such as SPI-4.2, 10-G Ethernet, RapidIO™, HyperTransport™, SFI-4, and NPSI, FPGAs are now required to support 1-Gbps data rates. At these higher data rates, I/O channels can become performance bottlenecks. Differential I/O standards—earlier used for backplane data transfers—are now being used for chip-to-chip data transfers as well. To eliminate these I/O bottlenecks, Stratix II devices support up to 152 receiver and 156 transmitter source-synchronous signaling channels using the LVDS or HyperTransport I/O standards, supporting 1 Gbps data transfer rates on each channel. These protocols can also be used for easy interface between Stratix II FPGAs and other components in high-speed systems.
- **Dynamic Phase Alignment (DPA):** Engineers designing systems that transfer data in the range of 1 Gbps are challenged by extremely small margins for clock-to-channel and channel-to-channel skew. To stay within these tight margins, they must use precise printed circuit board (PCB) design techniques to prevent the slight mismatches in trace lengths that can cause erroneous data transfers. To help simplify this design challenge, Altera has incorporated dynamic phase alignment (DPA) circuitry in Stratix II devices to dramatically reduce PCB design complexity and eliminate the signal alignment problems introduced by skew-inducing effects.
- **Unmatched DSP Bandwidth:** A convergence of data, audio, and video in DSP applications has led to increased performance requirements to support emerging protocols such as JPEG 2000, MPEG-4, 802.11x, CDMA2000, 1x EV DV, HSDPA, and W-CDMA. Stratix II devices contain dedicated DSP blocks optimized for commonly used DSP-intensive functions such as filtering, compression, chip-rate processing, equalization, digital IF, transforms, and modulation. Capable of running at 370 MHz, Stratix II DSP blocks deliver DSP throughput up to 288 GMACs—orders of magnitude faster than the leading-edge digital signal processors available today. Stratix II FPGAs can also be used to provide co-processor support for digital signal processors, assuming the computation-intensive DSP functions that would otherwise slow system performance. In addition, DSP block rounding and saturation support facilitates porting DSP firmware code onto FPGA designs for applications such as speech processing and voice over IP (VoIP).

- Design Security:** Stratix II devices address opportunities in new markets where IP protection is paramount. Stratix II devices incorporate advanced, non-volatile encryption technology based on the 128-bit AES to protect any on-board intellectual property (IP). Selected by the National Institute of Standards and Technology (NIST) and adopted by the United States government to protect sensitive information, AES is the most advanced encryption algorithm available today. Altera is only programmable logic vendor to offer AES-based encryption technology.

This suite of new and enhanced Stratix II features expands FPGA suitability for high-performance applications such as data storage, test equipment, and telecom infrastructure. For a complete description of Stratix II devices, please visit Altera's web site at www.altera.com/stratix2.

Table 1. Stratix II Family Overview						
Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,552	24,176	36,384	53,016	71,760
Equivalent Logic Elements	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM Blocks (512 bits + parity)	104	202	329	488	699	930
M4K RAM Blocks (4 Kbits + parity)	78	144	255	408	609	768
M-RAM Blocks (512 Kbits + parity)	0	1	2	4	6	9
Total RAM Bits	419,328	1,369,728	2,544,192	4,520,448	6,747,840	9,383,040
DSP Blocks	12	16	36	48	63	96
Embedded 18-bit x 18-bit Multipliers	48	64	144	192	252	384
PLLs	6	6	12	12	12	12
Maximum User I/O Pins	358	542	702	886	1,110	1,158
Available Packages	484-Pin FBGA 672-Pin FBGA	484-Pin FBGA 672-Pin FBGA	484-Pin FBGA ¹ 672-Pin FBGA 1,020-Pin FBGA	1,020-Pin FBGA 1,508-Pin FBGA	1,020-Pin FBGA 1,508-Pin FBGA	1,020-Pin FBGA 1,508-Pin FBGA

Quartus II Design Software

Stratix II devices are supported by Quartus[®] II version 4.0 design software, the industry's most advanced development software for FPGA, CPLD, and structured ASIC designs. Including many new ASIC-like design capabilities, this design software offers customers a comprehensive suite of synthesis, optimization, and verification tools in a single,

unified design environment. Timing closure and block-based design methodologies and features such as SOPC Builder and the SignalTap[®] II embedded logic analyzer allow designers to move from concept to production in just hours. Quartus II software also integrates seamlessly with all leading third-party synthesis and simulation tools. A free version of the software, Quartus II Web Edition, can be downloaded from the Altera web site at www.altera.com/q2webedition.