
Stratix Device Backgrounder

Introduction

Digital system design is driven by the need to shorten design cycles, enable faster time-to-market, and still allow for flexibility and ease-of-design to accommodate rapid technological advances. At the same time, systems are becoming increasingly complex and introducing more design challenges. These issues have gradually guided designers to integrate more functions into a single, high-density device.

For the first time, a programmable logic device (PLD) family has addressed these issues to create a more comprehensive solution: the Stratix™ device family from Altera.

Stratix Device Family

The Stratix device family is the ideal solution for complex designs such as data storage, test equipment, telecom infrastructure and other applications. Optimized to address the challenges of high-bandwidth systems, Stratix devices feature unmatched core performance, memory capacity, and time-to-market advantages. Stratix devices also offer dedicated functionality for clock management and digital signal processing (DSP) applications, as well as support for single-ended and differential I/O standards. In addition, Stratix devices offer on-chip termination and the capability for remote system upgrades.

Stratix devices are based on a 1.5-V, 0.13- μ m, all-layer copper SRAM process, with densities ranging from 10,570 to 114,140 logic elements (LEs) and up to 10 Mbits of RAM. Stratix devices offer up to 28 DSP blocks with up to 224 (9-bit x 9-bit) embedded multipliers optimized for DSP applications that require high data throughput. These devices support various differential I/O electrical standards such as the LVDS, LVPECL, PCML, and HyperTransport™ standards, as well as high-speed communication interfaces, including the 10G Ethernet XSBI, SFI-4, POS-PHY Level 4 (SPI-4 Phase 2), HyperTransport, RapidIO™, and UTOPIA IV standards. Stratix devices also offer a complete clock management solution with a hierarchical clock structure including up to 40 unique system clocks and up to 12 phase-locked loops (PLLs). Table 1 outlines the Stratix device family members and features.

Feature	EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1S120
Logic Elements (LEs)	10,570	18,460	25,660	32,470	41,250	57,120	79,040	114,140
M512 RAM Blocks 512-bits + parity	94	194	224	295	384	574	767	1,118
M4K RAM Blocks 4-Kbits + parity	60	82	138	171	183	292	364	520
MegaRAM Blocks 512-Kbits + parity	1	2	2	4	4	6	9	12
Total RAM bits	920,448	1,669,248	1,944,576	3,317,184	3,423,744	5,215,104	7,427,520	10,118,016
DSP Blocks	6	10	10	12	14	18	22	28
Embedded Multipliers	48	80	80	96	112	144	176	224
PLLs	6	6	6	10	12	12	12	12
Maximum User I/O Pins	422	582	702	726	818	1,018	1,234	1,310

Stratix devices are based on a new high-performance architecture built to simplify complex system design and allow for new levels of system integration. The new Stratix architecture, in conjunction with the Altera® Quartus® II design software, enables block-based design methodology, easy performance optimization of design blocks, and flexible integration of system features throughout the device.

The Stratix architecture has been built from the ground up by fusing technological aspects of hardware, software, and intellectual property (IP) functions for block-based design. The new architecture includes a MultiTrack™ interconnect routing structure with DirectDrive™ technology to fully harness the incremental design capability available in the Quartus II design software.

Stratix devices also have silicon-efficient dedicated functionality such as TriMatrix™ memory, DSP blocks, phase-locked loops (PLLs), True-LVDS™ circuitry, and double data rate (DDR) I/O circuitry. This functionality is not only optimized for maximum performance, but is also well integrated with the architecture's general programmable logic resources.

MultiTrack Interconnect

The new, high-performance Stratix architecture is based on the MultiTrack interconnect with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths used for inter- and intra-design block connectivity. MultiTrack routing is optimized for performance and maximum routing efficiency.

DirectDrive Technology

DirectDrive technology is a proprietary, deterministic routing technology that ensures identical routing resource usage for any function, regardless of its placement within the device. DirectDrive technology simplifies the system integration stage of block-based design by eliminating the time-consuming system re-optimization cycles that typically follow design changes and additions.

Performance Innovations in Stratix Devices

The combination of the MultiTrack interconnect, dedicated DSP blocks, and dedicated memory blocks give designers a performance-optimized architecture, resulting in significant performance improvements over previous architectures. These innovations allow Stratix devices to deliver on average a 40% improvement in push-button fMAX performance over previous architectures.

The performance enhancements in Stratix devices results in high-bandwidth capacity: up to 12 terabits per second memory bandwidth, data throughput of 2 GMACS per DSP block, an aggregate device data throughput of up to 600 Gbps, and up to 420-MHz core performance.

Stratix Device Features

Stratix devices contain powerful system-level features that offer unprecedented design flexibility and high-performance system integration. A general-purpose device family, Stratix devices offer a feature-rich, high-bandwidth system solution to take system-on-a-programmable chip (SOPC) solutions to new levels.

TriMatrix Memory

TriMatrix memory is a revolutionary memory structure that consists of an array of three sizes of memory blocks, each optimized to target a different class of applications: 512-bit M512 blocks for small functions such as first-in first-out (FIFO) applications; 4-Kbit M4K blocks for functions such as asynchronous transfer mode (ATM) cell processing; and 512-Kbit MegaRAM™ blocks for uses such as code storage for a Nios™ soft core embedded processor.

With up to 1,650 memory blocks, Stratix devices have more embedded memory than any other PLD. They offer the highest memory-to-logic ratio and the highest memory bandwidth with up to 10 Mbits of RAM, and up to 12 terabits per second of device memory bandwidth. The TriMatrix memory structure makes the Stratix family the PLD of choice for memory-intensive applications.

DSP Blocks

The DSP blocks in Stratix devices are high-performance embedded arithmetic units optimized for applications such as rake receivers, voice over Internet protocol (VoIP) applications, orthogonal frequency division multiplexing (OFDM), image processing applications, and multimedia entertainment systems. The DSP blocks eliminate performance bottlenecks in DSP applications, provide predictable and reliable performance, and result in resource savings without compromising performance. This makes DSP blocks ideal for implementing complex arithmetic functions while providing high data throughput.

Extensive PLLs & Clock Management Circuitry

Stratix clock management circuitry consists of a performance-optimized clock network and feature-rich PLLs for on- and off-chip clock management. With up to 12 PLLs and up to 40 system clocks per device, Stratix devices are the first PLDs to offer the on-chip PLL features for system-level clocking management previously found only in high-end discrete PLL devices. This comprehensive timing solution eliminates the need for multiple discrete timing devices on a board, saving real estate and overall systems cost. Stratix PLLs offer advanced features such as external feedback, clock switchover, PLL configuration, spread-spectrum clocking, and programmable bandwidth, providing customers with the tools to manage the most complex timing challenges for high-speed designs today.

Differential I/O Support

The Stratix family provides unprecedented high-speed differential I/O support with a maximum aggregate device bandwidth of up to 600 Gbps. The Stratix device family offers up to 116 high-speed differential I/O channels with up to 80 channels optimized for 840-Mbps operation. Stratix devices build on the True-LVDS capabilities of other Altera devices by providing enhanced embedded SERDES, multi-mode clocking, and data realignment.

Terminator Technology

Terminator technology is an on-chip termination resistor technology that supports on-chip serial, parallel, and differential termination to reduce reflections, improve signal integrity, and simplify complex board layout. Stratix devices are the first PLDs to offer termination support for differential I/O standards (such as LVDS) where high-quality signals are important for fast data transfer.

Dedicated External Memory Interfaces

In addition to offering abundant on-chip memory resources with the TriMatrix memory structure, Stratix devices have dedicated interfaces for high-speed external memory. This dedicated interface supports the latest industry-standard memory technologies, including DDR, SDRAM, QDR II SRAM, and ZBT SRAM devices. Designers can easily interface with these high-density memory devices without degrading data access performance or increasing development time.

Conclusion

Together with the Quartus II software, Stratix devices enable block-based methodology and flexible system integration. These high-performance, high-density PLDs offer shorter design cycles, and faster time-to-market for complex designs, and they allow designers to integrate more and more complex functions into a single device.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>

Copyright © 2002 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. HyperTransport is a trademark of the HyperTransport Consortium and RapidIO is a trademark of the RapidIO Trade Association. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.