



DSP Builder

Release Notes and Errata



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This chapter describes new features, revision history, known errata and documentation changes for the DSP Builder standard blockset.

Revision History

Table 1–1 lists the revision history for the DSP Builder standard blockset.

Table 1–1. DSP Builder Standard Blockset Revision History (Part 1 of 3)

Version	Date	Revision
8.1	November 2008	Removed obsolete Simulation Accelerator support and deprecated support for the Video and Image Processing Suite. Updated HIL block user interface.
8.0 SP1	July 2008	Maintenance release
8.0	May 2008	New Display Pipeline Depth block. Export HDL option added to Signal Compiler. Integration with the Quartus® II state machine editor. Added support for Stratix® IV devices. Stratix III DSP block renamed as DSP block. Added support for the Cyclone® III 3C120 and Stratix III 3SL150 DSP development boards. Added support for MATLAB R2007b and R2008a (dropped R14 SP3). Added support for the Quartus II IP (.qip) file and design archiving. Expanded platform support (Windows Vista 32-bit and 64-bit with 32-bit MATLAB). Several errata fixes and documentation updates.
7.2 SP3	March 2008	There were no errata fixes or documentation updates in this service pack which was released for compatibility with the Quartus II software only.
7.2 SP2	February 2008	There were no errata fixes or documentation updates in this service pack which was released for compatibility with the Quartus II software only.
7.2 SP1	December 2007	Several errata fixes and documentation updates.
7.2	October 2007	DSP Builder data type can now be displayed on signal connections. New Resource Usage block with ability to check hardware used and highlight critical paths. New simulation only Video Source and Video Sink blocks to support Video and Image Processing Suite MegaCore functions. Option to use port order from HDL when importing HDL. New option in TestBench block to handle unknowns. Added support for Cyclone II DE2 and Stratix II GX PCI Express boards. Enable port added to Barrel Shifter block. Non-zero reset option added to Delay block. Enhancements to Round block. Round and saturate modes added to Constant block.

Table 1-1. DSP Builder Standard Blockset Revision History (Part 2 of 3)

Version	Date	Revision
		<p>Removed port number restriction on <code>VCD Sink</code> block.</p> <p>Added optional saturation occurred port added to <code>Saturation</code> block.</p> <p>Control ports made optional on <code>Parallel to Serial</code> and <code>Serial to Parallel</code> blocks.</p> <p>The <code>HDL Input</code>, <code>Output</code>, and <code>Non-synthesizable Output</code> blocks now have option to specify a <code>Simulink Fixed Point</code> or <code>Double</code> type.</p> <p>New option in the <code>HDL Entity</code> block to take port names from the subsystem instead of using the <code>HDL Input</code> and <code>HDL output</code> block names.</p> <p>The dependency on text files and limitation on number of ports has been removed for the <code>State Machine Table</code> block.</p> <p>The <code>MegaCore</code> function blocks now display ports in the order they are displayed in the <code>VHDL</code>.</p>
7.1 SP1	June 2007	Several errata fixes plus various documentation enhancements and corrections.
7.1	May 2007	<p>New blocks include: <code>Single-Port RAM</code>, <code>True Dual-Port RAM</code>, <code>Bus Splitter</code>, new <code>Signal Compiler</code> and <code>TestBench</code>, <code>Clock</code> and <code>Clock_Derived</code> (replaces <code>ClockAltr</code>), <code>Stratix III DSP</code> block (supports fine-grain control of multiply add and multiply accumulate operations for Stratix III devices)</p> <p><code>Single-port Avalon-MM</code> blocks obsoleted in favour of the multi-port <code>Avalon-MM Master</code> and <code>Avalon-MM Slave</code> blocks.</p> <p>New fast functional simulation support for <code>Video</code> and <code>Image Processing Suite MegaCore</code> functions.</p> <p>New HDL generation flow.</p> <p>Support for multiple-clock domains</p> <p>Individual controls for optional ports and implicitly wired asynchronous clear.</p> <p>Added support for <code>Arria™ GX</code> devices.</p>
6.1	December 2006	<p>Added support for <code>Stratix III</code> devices.</p> <p>Added support for the <code>Cyclone II EP2C70</code> DSP development board and <code>Santa-Cruz</code> connectors added to the <code>Cyclone II EP2C35</code> board</p> <p><code>DSPBUILDER_ROOTDIR</code> is now a system environment variable</p> <p>New <code>All Blocks</code> library provides direct access to all blocks.</p> <p>New <code>Simulation</code> library containing <code>External RAM</code> block</p> <p><code>SOPC Builder Links</code> library renamed as <code>Interfaces</code> library contains renamed <code>Avalon®</code> <code>Memory-Mapped</code> interface blocks and new <code>Avalon Streaming</code> adapter and interface blocks.</p> <p>New <code>tbdiff</code> comparison utility and updated <code>dspbuilder_sh</code> utility</p>
6.0 SP1	June 2006	Updated <code>Quartus II Global Project Assignment</code> block and various errata fixes.
6.0	April 2006	<p>New <code>DSPBUILDER_ROOTDIR</code> environment variable.</p> <p>Added support for <code>Stratix II GX</code> devices.</p> <p>Further enhancements to <code>SOPC Builder</code> integration.</p> <p>Extended parameter support using <code>MATLAB</code> workspace or masked subsystem variables.</p> <p>The help system now supports the <code>MATLAB Index</code> and <code>Search</code> tabs.</p>
5.1 SP1	January 2006	Various errata fixes and documentation enhancements.

Table 1-1. DSP Builder Standard Blockset Revision History (Part 3 of 3)

Version	Date	Revision
5.1	October 2005	New HDL Import block in Altlib library. Improved SOPC Builder integration including new Avalon blockset in SOPC Builder links library. Automatic propagation of signal names. Parameterized signal widths supported using MATLAB workspace variables. Improved error messaging. Improved documentation integrated with the MATLAB help system.
5.0.1	August 2005	Added support for the Stratix II EP2S180 DSP development board.
5.0.0	April 2005	Updated version from 3.0.0 to 5.0.0. Added support for the Cyclone II EP2C35 DSP development board.
3.0.0	January 2005	Added support for Hardware in the Loop (HIL). Added additional blocks and design examples.
2.2.0	August 2004	Added support for MegaCore functions. Added support for Cyclone II and Stratix II devices.
2.1.3	July 2003	Split documentation into separate reference manual and user guides.
2.1.2	April 2003	Added support for the Stratix EP1S80 DSP development board.
2.1.1	February 2003	Added information on using DSP Builder modules in external RTL designs. Added information on creating custom library blocks.
2.1.0	December 2002	Added support for Stratix GX and Cyclone devices. Added PLL and state machine support.
2.0.0	June 2002	New arithmetic, storage, DSP board, complex signals and SOPC Builder blocks.
1.0	October 2001	First release of DSP Builder.

Errata

Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. [Table 1-2](#) shows the errata that affect the DSP Builder standard blockset v8.1, v8.0 SP1, v8.0, v7.2 SP1, and v7.2.



There were no errata added or updated in the 7.2 SP3 or 7.2 SP2 releases of DSP Builder.

Table 1-2. DSP Builder Standard Blockset Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version				
		8.1	8.0 SP1	8.0	7.2 SP1	7.2
01Nov08	Cannot Compare Simulink Against ModelSim When Using VIP Suite IP	✓	—	—	—	—
	MATLAB Hangs If You Press Enter in Signal Compiler Device Box	✓	—	—	—	—
	Reset Signal Inverted if _n Appended to Signal Name	✓	✓	✓	✓	✓
	Error Generating HDL for State Machine Editor Block	Fixed	✓	✓	—	—
	Run-Time Error During FFT Fast Functional Simulation	Fixed	✓	✓	—	—

Table 1-2. DSP Builder Standard Blockset Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version				
		8.1	8.0 SP1	8.0	7.2 SP1	7.2
15May08	Errors Issued With Imported Quartus II Project	✓	✓	✓	—	—
	Additional Project Assignments Required for User Libraries	✓	✓	✓	—	—
01Dec07	Incorrect Format Documented for Product Block Output	—	—	—	Fixed	✓
15Oct07	SignalTap II Analyzer Failed Acquire Action After Recompile	—	—	Fixed	✓	✓
	Fast Functional Simulation Fails for 128-bit Avalon-MM Interface	—	—	—	Fixed	✓
01Oct07	Cannot Compile a v7.1 Design Containing a PFC Block	—	—	Fixed	✓	✓
	Cannot Simulate Deinterlacer with Avalon-MM Master Block	—	—	Fixed	✓	✓
01Jun07	Development Board Output Clocks Missing in VHDL	—	—	—	—	Fixed
	ena Port on Counter Block is Connected Differently	—	—	—	—	Fixed
01May07	Dual-Clock FIFO Simulation Does Not Match ModelSim	✓	✓	✓	✓	✓
	Cannot Initialize RAM From HEX Files if Widths are Different	—	—	—	—	Fixed
01Mar07	State Machine VHDL Incorrect if Logic Operator used as Input	—	—	—	—	Fixed



For the latest errata information, refer to the *DSP Builder Release Notes and Errata* on the Altera literature website.

Cannot Compare Simulink Against ModelSim When Using VIP Suite IP

Execution of the **Compare against HDL** or **Generate HDL** steps available in the **Testbench Generator** dialog box generates an error for Video and Image Processing Suite MegaCore functions.

Affected Configurations

Designs using Video and Image Processing Suite MegaCore function blocks.

Design Impact

Testbench generation does not complete successfully, and automatic comparison of the Simulink simulation results against the results from ModelSim is not possible.

Workaround

A MATLAB m-script is provided that give access to the testbench flow, with the flow output being sent to the MATLAB command window. The command required to use this script is:

```
alt_dspbuilder_compare_VIP_design_against_HDL(<model>, <performcompare>)
```

where:

- *<model>* is the name of the .mdl file for which the flow is to be run.
- *<performcompare>* is optional, setting it to 0 causes the final Compare Results step to be skipped. The default value of 1 causes the Compare Results step to be run.

After the script is run, the features available in the **Advanced** tab of the **Testbench Generator** dialog box can be used (excluding the **Generate HDL** step).

Solution Status

Use of the Video and Image Processing Suite MegaCore functions in DSP Builder v8.1 is deprecated, and support is likely to be dropped in future releases.

MATLAB Hangs If You Press Enter in Signal Compiler Device Box

MATLAB hangs if you press the Enter or Return key in the **Device** box on the **Signal Compiler** dialog box.

Affected Configurations

All configurations.

Design Impact

None.

Workaround

Take care to avoid pressing the Enter or return key after typing the device name.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Reset Signal Inverted if `_n` Appended to Signal Name

The reset signal is inverted if `_n` is appended to the signal name specified in the `Clock` or `Clock_Derived` block.

Affected Configurations

Designs which include a `Clock` or `Clock_Derived` block.

Design Impact

The inverted reset signal is propagated through the design.

Workaround

Do not append `_n` to the reset signal specified in a `Clock` or `Clock_Derived` block unless you explicitly want the signal to be inverted. Note that you can append `_N` (uppercase) without inverting the reset signal.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Error Generating HDL for State Machine Editor Block

Generating HDL from some State Machine Editor block configurations can cause an access violation to occur.

Affected Configurations

Designs using the State Machine Editor block which include the `==` operator in conditional expressions.

Design Impact

HDL generation does not complete successfully, and the block configuration is not integrated into the DSP Builder design.

Workaround

Do not use the == operator in conditional expressions. However, you can use the ~ operator. For example, use `in1` and `~in1` rather than `in1==1` and `in1==0`.

Solution Status

This issue is fixed in v8.1 of the Quartus II software.

Run-Time Error During FFT Fast Functional Simulation

Designs containing the FFT MegaCore function block cannot be simulated using the fast functional simulation technology.

Affected Configurations

Any v8.0 design containing v7.1, v7.2 or v8.0 FFT MegaCore function blocks.

Design Impact

Attempting to perform a bit-accurate (faster) simulation will cause a run-time error to occur.

Workaround

Double-click the `Simulation Accelerator` block to select cycle-accurate mode before performing simulation.

Solution Status

Fast functional simulation is obsolete in v8.1.

Errors Issued With Imported Quartus II Project

HDL `Import` blocks that import Quartus II projects may cause errors whilst executing the Signal Compiler or TestBench flows.

Affected Configurations

Models with HDL `Import` blocks that import Quartus II projects with `SEARCH_PATH` assignments, rather than `USER_LIBRARIES` assignments.

Design Impact

Models containing HDL `Import` blocks that import Quartus II projects generated using Quartus II v8.0 may fail to generate hardware because library settings are not obeyed.

Workaround

Add a `USER_LIBRARIES` setting to the `.qsf` file for the Quartus II project to be imported. The assignment value should be the concatenation of all the project's `SEARCH_PATH` assignment values, separated by semi-colons and enclosed within quotes. These required search path values may be in the top-level `.qsf` file, or in `.qip` files included in the project. Then recompile the `HDL Import` block.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Additional Project Assignments Required for User Libraries

Additional project assignments may be required when using the Export HDL flow with user libraries.

Affected Configurations

Configurations that include MegaCore function, `HDL import` or `State Machine Editor` blocks.

Design Impact

Compilation fails in the Quartus II software with an error of the form:

```
Error: Node instance <block_name> instantiates undefined entity  
<entity_name>
```

Workaround

Add the following to the Quartus II project:

- The `.qip` file corresponding to the entity named in the error message. (This file is located in the import subdirectory corresponding to the library model.)
- In some cases you may also need to add any libraries which are referenced by `HDL Import` block(s) in the library model.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Incorrect Format Documented for Product Block Output

The output format for the `Product` block was given incorrectly in the documentation as:

```
Simulink:  
O1[L1+L2].[2*max(R1,R2)]  
VHDL:  
O1:out STD_LOGIC_VECTOR({L1+L2+2*max(R1,R2)-1} DOWNT0 0)
```

The output formats should be:

```
Simulink:  
O1[2*max(L1,L2)].[2*max(R1,R2)]
```

```
VHDL:  
O1:out STD_LOGIC_VECTOR( {2*max(L1,L2)+2*max(R1,R2)-1} DOWNT0 0)
```

Solution Status

This issue is fixed in DSP Builder v7.2 SP1.

SignalTap II Analyzer Failed Acquire Action After Recompile

The SignalTap II Analyzer caches information after it is run.

Affected Configurations

All configurations using Signal Tap II are affected.

Design Impact

When a design is recompiled in Signal Compiler and the device is reprogrammed with the new .sof, SignalTap II Logic Analyzer fails to acquire, with the following error messages:

```
Error: Can't find the instance.  
Download a design with SRAM Object File containing this instance.  
Error: Acquisition stopped unexpectedly. No data are returned. Please  
check previous error messages.
```

Workaround

Re-scan the chain after re-compile (and program) before Acquire. This will reset the SignalTap II Analyzer. Alternatively, you can close the model and open it again to clear the cached information.

Solution Status

This issue is fixed in DSP Builder v8.0.

Fast Functional Simulation Fails for 128-bit Avalon-MM Interface

The 128-bits wide master ports of the Video and Image Processing Suite Deinterlacer MegaCore function cannot be simulated using bit-accurate simulation in DSP Builder.

Affected Configurations

Configurations using the Video and Image Processing Suite Deinterlacer MegaCore function with 128-bits wide data ports on an Avalon® Memory-Mapped (Avalon-MM) interface.

Design Impact

The design cannot be simulated using fast, bit-accurate only, simulation. Attempting to do so may cause MATLAB to crash.

Workaround

Change the Avalon-MM port widths to 64 to test the design with the fast bit-accurate simulation, then revert to 128 bits before the compilation.

Solution Status

This issue is fixed in DSP Builder v7.2 SP1.

Cannot Compile a v7.1 Design Containing a PFC Block

The v7.2 `Signal Compiler` and `TestBench` blocks cannot handle the resets for a `Packet Format Converter (PFC)` block from a v7.1 design.

Affected Configurations

Any v7.1 design containing an `Avalon-ST Packet Format Converter` block.

Design Impact

The design does not compile in `Signal Compiler` or `TestBench`.

Workaround

Open the `DSPBuilder_<design_name>_import` directory. In this directory, delete all files with names that begin with `alt_avalonst_pfc`. Simulate the design in Simulink and recompile using the `Signal Compiler` or `TestBench` block.

Solution Status

This issue is fixed in DSP Builder v8.0.

Cannot Simulate Deinterlacer with Avalon-MM Master Block

If the Avalon-MM master ports on the Deinterlacer MegaCore function are connected to DSP Builder `Avalon-MM Master` blocks then Simulink detects algebraic loops and cannot simulate.

Affected Configurations

This issue affects the Deinterlacer v7.2 MegaCore function with double or triple buffering selected.

Design Impact

The design can be synthesized as normal, but simulation cannot be performed in Simulink.

Workaround

The problem occurs because Avalon-MM masters have to respond combinationally to their `waitrequest` port. This means that the `waitrequest` ports on the Deinterlacer have to be marked as direct-feed through so that Simulink can simulate them correctly.

However, if Simulink finds a loop where an output of a block could drive an input to the same block via only direct feed-through connections then an algebraic loop is reported and simulation cannot be performed.

This happens when the Deinterlacer's master ports are connected to the `Avalon-MM Master` block because the master block is also direct-feed through, and Simulink cannot see that its `waitrequest` input is only connected to its `waitrequest` output.

The problem can be worked around by incorrectly asserting to Simulink that the `waitrequest` port of the Deinterlacer is not direct-feed through. This does have the limitation that if `waitrequest` is ever set high during the simulation then the simulation results are incorrect.

The `External RAM` simulation block does not assert `waitrequest` unless it is specifically configured to do so in its GUI, so this allows some level of simulation to be performed.

To mark the port as delayed rather than direct feed through, there are two options. Either:

1. Download the *Video Processing Reference Design* from the Altera website.
2. Open `example_design_data_path.mdl`.
3. Copy and paste the block named `algebraic_loop_cut_dil` into your design.

Or:

1. Click on the Deinterlacer MegaCore function block to select it.
2. In the MATLAB command window, type:

```
set(gcbh,'inDelayed', regexprep(get(gcbh,'inDelayed'),'0','1'));
```

Solution Status

This issue is fixed in a DSP Builder v8.0.

Development Board Output Clocks Missing in VHDL

In DSP Builder v7.0 or earlier, one or more PLLs are automatically included to provide output clocks which are listed in the top level VHDL, with the clock locations assigned to the selected pins from the board configuration block. In v7.1 and later, PLLs are not automatically added in the design because there may be conflicting PLLs in higher levels of the design hierarchy.

Affected Configurations

All configurations are affected.

Design Impact

The clock outputs selected from the board configuration block do not appear in the top level of the generated VHDL.

Workaround

Add PLL blocks into your design and configure them to provide the required output clocks. In v7.1, the PLL output clocks need to be exported for them to appear in the VHDL top level. You can assign locations to the pins by creating a Tcl script named `<pll_clock_pins>_add.tcl` in the `DSPBuilder_<design_name>_import` folder within the design folder. The following example shows the required assignments for the `Test2S60Board.mdl` design example:

```
set_location_assignment PIN_C16 -to PLL_clk0_out
set_location_assignment PIN_B15 -to PLL_clk1_out
set_location_assignment PIN_B18 -to PLL_clk2_out
```

```
set_location_assignment PIN_D18 -to PLL_clk3_out
set_location_assignment PIN_D16 -to PLL_clk4_out
set_location_assignment PIN_C15 -to PLL_clk5_out
```

Solution Status

In v7.2 or later, you can make the assignments directly in the model using the Quartus II Pinout Assignments block.

ena Port on Counter Block is Connected Differently

In v6.1, the ena port was connected to the clock enable (clk_ena) on the LPM. However, in v7.1, it is connected to the count enable (cnt_ena).

Affected Configurations

All configurations are affected.

Design Impact

sload loads data while not enabled.

Workaround

Modify the input to the sload port by ANDing the synchronous load signal with the enable signal into this port (to make sure that you are not performing a synchronous load while the enable is low).

Solution Status

This issue is fixed in DSP Builder v7.2. Two enable control ports are now provided: The clock enable (clk_ena) disables counting, sload, sset and sclr. The counter enable (ena) disables counting, but not sload, sset or sclr.

Dual-Clock FIFO Simulation Does Not Match ModelSim

The Dual-Clock FIFO simulation in Simulink is functionally equivalent to hardware, but not cycle-accurate.

Affected Configurations

Most configurations are affected.

Design Impact

The delay between the write-side adding data and the read-side seeing it, and between the read-side clearing space in the FIFO and the write-side seeing it, does not match hardware.

Workaround

Do not rely on these timing characteristics for correctness of a design.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Cannot Initialize RAM From HEX Files if Widths are Different

You cannot initialize the Single-Port RAM, Dual-Port RAM, True Dual-Port RAM, or ROM blocks using an Intel format HEX file unless the widths in the HEX file and on the block are the same or a multiple of 8.

Affected Configurations

All configurations are affected.

Design Impact

An exception is issued.

Workaround

Set the block width to be the same or a value divisible by 8. For example, if you want a width of 65, set it to 72 instead. This will then not give an exception. In general, make sure that the data width in any initialization HEX file is identical to the data width specified for the block.

A warning is issued if this is not the case and the simulation results may not be the same as hardware. Note that you can quickly compare the simulation results with hardware using a TestBench block.

Solution Status

This issue is fixed in DSP Builder v7.2.

State Machine VHDL Incorrect if Logic Operator used as Input

When state machine VHDL is generated, the expression strings for the port names are replaced by signals named *<port name>_sig*. This replacement can interfere with the expression logic. For example, if you have an AND statement and a port named A, then AND is replaced by A_sigAND in the generated VHDL. Similar problems occur if AN, AND, O or OR are used as input names.

Affected Configurations

All configurations are affected.

Design Impact

Invalid VHDL is generated.

Workaround

Avoid using inputs named A, AN, AND, O or OR.

Solution Status

This issue is fixed in DSP Builder v7.2.

This chapter describes new features, revision history, known errata and documentation changes for the DSP Builder advanced blockset.

Revision History

Table 2–1 lists the revision history for the DSP Builder advanced blockset.

Table 2–1. DSP Builder Advanced Blockset Revision History

Version	Date	Revision
8.1	November 2008	New W-CDMA example designs. Latency display option on ModelIP blocks. DONT_CARE option on Dual Memory block. Diagrammatic channelization format display for ModelIP blocks. Quartus IP (.qip) file support. Latency constraints can be applied to primitive subsystems using the <code>SynthesisInfo</code> block.
8.0 SP1	July 2008	Maintenance release
8.0	May 2008	First release of the DSP Builder Advanced Blockset

Errata

Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications.


Table 2–2 shows the errata that affect the DSP Builder advanced blockset v8.0 SP1 or V8.0.

Table 2–2. DSP Builder Standard Blockset Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version		
		8.1	8.0 SP1	8.0
01Nov08	Saturation Limitation When using the Scale Block	✓	—	—
	Very High Hard Multiplier Threshold Does Not Force the Use of Logic	✓	—	—
	No Forward Flow Control in primitive Subsystems	✓	—	—
	Primitive Automatic Testbench Flow Incorrect With Many Integer Bits	✓	—	—
	Limitations of the ModelSim Testbench Flow	✓	—	—
	Limit of 50 Subsystem Ports Anywhere in a Design	✓	—	—
	HIL Error When Using Async Clear as Async Load	Fixed	✓	✓

Table 2-2. DSP Builder Standard Blockset Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version		
		8.1	8.0 SP1	8.0
15May08	Results for ModelPrim Blocks May be Incorrect for Fractional Types	Fixed	✓	✓
	Cannot Import a Combined Blockset Design into SOPC Builder	✓	✓	✓
	Incorrect Simulation Results if Word Length Greater Than 64bits	✓	✓	✓
	Compilation Error if Unused Channel Out Port is Terminated	✓	✓	✓

 For the latest errata information, refer to the *DSP Builder Release Notes and Errata* on the Altera literature website.

Saturation Limitation When using the Scale Block

When you increase the number of fractional bits used for a signal, the MSB may be truncated.

Affected Configurations

Configurations using the Scale block.

Design Impact

The MSB may be truncated.

Workaround

Use a Convert block inside the primitive subsystem.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Very High Hard Multiplier Threshold Does Not Force the Use of Logic

Setting a very high Hard Multiplier Threshold should avoid using any DSP blocks.

Affected Configurations

All configurations.

Design Impact

Unwanted use of DSP blocks.

Workaround

None.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

No Forward Flow Control in primitive Subsystems

'Bursty' input data is not supported for primitive subsystems, that is designs where the valid signal toggles high and low.

Affected Configurations

Any primitive subsystem.

Design Impact

The simulation results are incorrect.

Workaround

Avoid using bursts of data.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Primitive Automatic Testbench Flow Incorrect With Many Integer Bits

The primitive automatic testbench flow may be incorrect when using fractional representations with many integer bits.

Affected Configurations

Designs that require a large number of integer bits.

Design Impact

Unexpected Simulation mismatches are reported.

Workaround

Reduce the number of integer bits required by your model.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Limitations of the ModelSim Testbench Flow

The Run ModelSim block can be used to simulate a model in ModelSim. This flow attempts to make a ModelSim testbench by synthesizing all the block (including any Simulink blocks in the top-level). However only a limited number of Simulink blocks are synthesizable and an empty subsystem is created for the unsupported blocks.

Affected Configurations

Any model with unsynthesizable Simulink blocks in the top-level.

Design Impact

The testbench cannot be simulated.

Workaround

Use only the supported blocks in the testbench for your design or write your own HDL for the empty subsystems. (A full list of synthesizable blocks is given in the description of the Run ModelSim block.) Alternatively, you can use the automatic test bench flow to simulate each subsystem in your design separately.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Limit of 50 Subsystem Ports Anywhere in a Design

All blocks that become functional units are restricted to a maximum of 50 ports.

Affected Configurations

Any block or subsystem that has more than 50 ports.

Design Impact

An assert `m_inCount <= m_maxInCount` which crashes MATLAB.

Workaround

Avoid creating a subsystem or block with more than 50 ports.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

HIL Error When Using Async Clear as Async Load

A Hardware-in-the-Loop (HIL) design does not work when the reset is used both as Async Clear and Async Load, and is tied to the JTAG reset.

Affected Configurations

Advanced blockset designs that integrate a HIL block from the standard blockset.

Design Impact

The design stays under reset and all outputs are zero.

Workaround

None.

Solution Status

This issue is fixed in v8.1 of the DSP Builder advanced blockset.

Results for ModelPrim Blocks May be Incorrect for Fractional Types

The ModelPrim blocks give an incorrect result if you specify a fractional output bit width that is different to the width that would be selected if you choose the **Inherit via Internal Rule** option.

Affected Configurations

Configurations of ModelPrim blocks where the **Specify via dialog** option has been used.

Design Impact

The simulation value does not match the Simulink multiplier.

Workaround

When using fractional types, ensure that the output bit width is specified to be the sum of the input bit widths. Alternatively, add a `Convert` block if you need any other fractional output bit width.

Solution Status

This behavior is described in v8.1 of the *DSP Builder Advanced Blockset User Guide*.

Cannot Import a Combined Blockset Design into SOPC Builder

You cannot import a design that combines blocks from the standard and advanced blocksets into SOPC Builder.

Affected Configurations

Configurations which combine blocks from the standard and advanced blocksets.

Design Impact

If you attempt to import a combined blockset design into SOPC Builder, warning are issued stating that there are multiple clocks with the same name and the component is not added to the system.

Workaround

There is no workaround.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Incorrect Simulation Results if Word Length Greater Than 64bits

The simulation results are incorrect for ModelIP blocks if the word length is greater than 64 bits.

Affected Configurations

Configurations which include ModelIP blocks are affected. However, ModelPrim blocks do support word lengths greater than 64 bits.

Design Impact

The simulation results are incorrect.

Workaround

Restrict the word length used by ModelIP blocks to 64 bits.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Compilation Error if Unused Channel Out Port is Terminated

Quartus II compilation fails if an unused channel or valid signal from a Channel Out block is connected to a Simulink Terminator block inside a primitive subsystem.

Affected Configurations

Primitive subsystems with unused channel or valid output signals.

Design Impact

Incorrect HDL is generated and errors are issued when you attempt to compile the design in the Quartus II software.

Workaround

Leave the unused signals unconnected or terminate the signals outside the primitive subsystem.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Update Status

The following table displays the update status for these release notes.

Date	Version	Changes Made
November 2008	3.0	Updated for software version 8.1.
July 2008	2.1	Added one errata to standard blockset chapter.
May 2008	2.0	Added separate chapter for the advanced blockset and moved install information to new <i>DSP Design Flow User Guide</i> .
December 2007	1.2	Fixed two errata.
15 October 2007	1.1	Added two errata.
October 2007	1.0	New combined release notes and errata document for the current and previous two releases.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Contact 1	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com







Note to table:

- (1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown in the following table.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, and software utility names. For example, \qdesigns directory, d: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicates document titles. For example: <i>AN 519: Stratix IV Design Guidelines</i> .

Visual Cue	Meaning
<i>Italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>. .pcf file.
Initial Capital Letters	Indicates keyboard keys and menu names. For example, Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. Active-low signals are denoted by suffix n. Example: resetn. Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
 CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
 WARNING	A warning calls attention to a condition or possible situation that can cause you injury.
	The angled arrow instructs you to press the enter key.
	The feet direct you to more information about a particular topic.