

This document provides late-breaking information about the following areas of the Altera® Quartus®II software version 10.0:

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For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes*. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*. Both documents are available on the Altera website at <http://www.altera.com/literature/lit-rn.jsp>.

New Features & Enhancements

The Quartus II software version 10.0 includes the following new features and enhancements:

- The Quartus II software version 10.0 supports the following new megafunctions:
 - 10-Gbps Ethernet MAC MegaCore function
 - 10GBase-R PHY MegaCore function
 - Altera PLL megafunction
 - Custom PHY megafunction
 - DDR2 and DDR3 SDRAM with UniPHY MegaCore functions
 - Interlaken PHY MegaCore function
 - Low Latency PHY megafunction
 - Low Latency PHY Controller megafunction
 - PCI Express PIPE PHY megafunction
 - Transceiver Reconfiguration Controller PHY megafunction

- XAUI PHY MegaCore function
- The System Console includes new Transceiver Toolkit support for evaluating the data transfer error rate of transceiver links between transmitters and receivers under different configurations in your system. The System Console performs low-level hardware debugging of SOPC Builder systems. You can use the System Console to access IP cores instantiated in your SOPC Builder system for initial bring-up of your PCB and for low-level testing.
- The Transceiver Toolkit allows you to quickly test the functionality of transceiver channels and the signal integrity of transceiver links in your design. You can use the Transceiver Toolkit before your design is complete to verify that your design is functioning properly at different stages in the development process.
- The QXP Viewer allows you to view a summary of the contents in a Quartus II Exported Partition File (**.qxp**) when you open the **.qxp** in the Quartus II software.
- When you export a partition, depending on the level of results preservation you want to maintain, you can now choose to export a post-synthesis netlist, a post-fit netlist, or both.

EDA Interface Information

The Quartus II software version 10.0 supports the following EDA tools:

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify & Synplify Pro	C-2009.12	✓
Mentor Graphics Precision RTL Synthesis	2009a	✓
Mentor Graphics LeonardoSpectrum	2009a	✓
Synopsys Design Compiler	Not supported	—
Mentor Graphics DK Design Suite	5.0 SP5	✓
Simulation Tools	Version	NativeLink Support
Mentor Graphics ModelSim	6.5e	✓
Mentor Graphics ModelSim-Altera	6.5e	✓
Mentor Graphics ModelSim-Altera Starter Edition	6.5e	✓
Mentor Graphics QuestaSim	6.5e	✓
Cadence NC-Sim	9.2 (Linux only)	—
Synopsys VCS / VCS MX	Y-2009.12	✓
Aldec Active-HDL	8.2-SP1 (Windows only)	✓
Aldec Riviera-PRO	2010.02	✓
Formal Verification Tools (Equivalence Checking)	Version	NativeLink Support
Cadence Encounter Conformal	8.1	—
Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	Version	NativeLink Support
Mentor Graphics TAU		—
Board Level Symbol/Pin-out Management	Version	NativeLink Support
Mentor Graphics I/O Designer		—

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Refer to the Quartus II Default Settings File (.qdf), `<Quartus II installation directory>/quartus/bin/assignment_defaults.qdf`, for a list of all the default assignment settings for the latest version of the Quartus II software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 10.0	
The Simulator and the Waveform Editor are not provided in the Quartus II software beginning with version 10.0.	Use Mentor Graphics ModelSim-Altera Edition or a third-party EDA simulator and waveform editor.
The Classic Timing Analyzer will not be provided in future versions of the Quartus II software beginning with version 10.1.	Use the Quartus II TimeQuest Timing Analyzer.
In future versions of the Quartus II software beginning with version 10.1, the Quartus II software will not set a QUARTUS_ROOTDIR environment variable.	Modify any scripts you may have so that they do not depend on the QUARTUS_ROOTDIR environment variable or set a QUARTUS_ROOTDIR environment variable to <code><Quartus II software path>\quartus</code> manually.
If you change Advanced options in the Convert Programming Files dialog box, the Memory Map file (.map) generated by the Programmer contains a list of your Advanced options changes.	
For designs that target Cyclone IV GX devices, the TimeQuest Timing Analyzer automatically creates clock uncertainty constraints for forwarded clocks.	
The MegaWizard Plug-In Manager no longer supports the following megafunctions: ALT3PRAM, ALTACCUMULATE, ALTGXB, ALTSHIFT_TAPS, ALTSQRT, LPM_ABS, LPM_ADD_SUB, LPM_AND, LPM_COMPARE, LPM_CONSTANT, LPM_COUNTER, LPM_DECODE, LPM_DIVIDE, LPM_FF, LPM_FIFO+, LPM_INV, LPM_LATCH, LPM_MUX, LPM_OR, LPM_RAM_DP, LPM_RAM_DP+, LPM_RAM_DQ, LPM_ROM, LPM_SHIFTREG, and LPM_XOR. You can compile designs that include the above megafunctions in the Quartus II software version 10.0, but you cannot create new instances or edit existing variations of these megafunctions.	
The ALTLVDS megafunction has been repackaged as two megafunctions: ALTLVDS_RX and ALTLVDS_TX. Designs developed with previous versions of the ALTLVDS megafunction can be compiled with the Quartus II software version 10.0; however, you cannot modify an ALTLVDS megafunction with the Quartus II software version 10.0.	If you want to modify your ALTLVDS megafunction variant, you must instantiate new ALTLVDS_RX and ALTLVDS_TX megafunctions.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 10.0	
If you press the Esc key during installation of the Altera Complete Design Suite, the Altera Installer exits immediately, leaving partially incorrectly installed software.	Do not press the Esc key while the Altera Installer is open.
The Destination path box in the Altera Installer supports only the Basic Latin character set.	Use only Basic Latin characters in the Destination path box.
If you uninstall any component of the Altera Complete Design Suite, and then attempt to uninstall DSP Builder, uninstallation of DSP Builder fails.	Uninstall DSP Builder first.
Tk scripts cannot be run from the Quartus II GUI.	
Tcl scripts that include the line <code>package require ::quartus::project</code> cannot be run from the Tcl Script dialog box or the Tcl Console.	To run the Tcl script either: <ul style="list-style-type: none"> ■ Change the line <code>package require ::quartus::project</code> to <code>package require ::quartus::project_ui</code> or ■ Run the script from a command prompt with the quartus_sh command: <code>quartus_sh -t <Tcl script file name></code>
Revision creation fails silently if the Quartus II Project File (.qpf) is read-only. This failure occurs if you attempt to create revisions with the GUI or with the Tcl API, and can cause failures in features that rely on the creation of revisions, such as Design Space Explorer (DSE).	Ensure that the .qpf for your project is writable.
In the MegaWizard Plug-In Manager, you cannot copy an existing custom megafunction variation (page 2d does not copy).	Manually copy your existing custom megafunction variation to a different directory.

Issue	Workaround
<p>The IP Search Path used by the MegaWizard Plug-In Manager includes the Global Libraries and the Normal IP Search Path as described in <i>SOPC Builder Component Search Path</i> in the <i>SOPC Builder Chapter</i> of Volume IV of the <i>Quartus II Handbook</i>, but the IP Search Path does not include the User Library Search Path.</p>	<p>Add the paths to your libraries to the IP Search Path in SOPC Builder by performing the following steps:</p> <ol style="list-style-type: none"> 1. In the main window of the Quartus II software, on the Tools menu, click SOPC Builder. 2. In the Create New System dialog box of SOPC Builder, click Cancel. 3. In SOPC Builder, on the Tools menu, click Options. 4. In the Category list of the Options dialog box, click IP Search Path. 5. Click Add. 6. In the Open dialog box, select the directory containing your libraries. 7. Click Open. 8. Repeat steps 3-5 to add additional library paths. 9. Click Finish.
<p>In the Pin Planner, on the Edit menu, the Find and Find Next commands are not available.</p>	
<p>In the Key box of the SOF File Properties:Bitstream Encryption - Key Entry dialog box, the backspace key does not function correctly. Instead of deleting the last character in the box, it deletes the second-to-last character.</p>	<p>Use the Clear button at the bottom of the dialog box, and then re-type the entry into the Key box.</p>
<p>In UniPHY-based IP, If you attempt to run the <code><variation name>_pin_assignments.tcl</code> file from the Tcl Scripts dialog box, the file fails to apply pin assignments.</p>	<p>To run the <code><variation name>_pin_assignments.tcl</code> file, type the following command in the Tcl Console:</p> <pre>source <path to file>/<variation name>_pin_assi gnments.tcl</pre> <p>For example:</p> <pre>D:/MyQDR/constraints/qdr_pin_assignments .tcl</pre>
<p>All of the FIFO MegaWizard Plug-In Manager cannot be displayed with a 1024x780 screen resolution.</p>	<p>Change your screen resolution to a higher value or move the page to see the right side.</p>
<p>In the FIFO MegaWizard Plug-In Manager, on the Rdreq Option, Blk Type tab of the Parameter Settings page, the last item in the Set the maximum block depth to box is not fully displayed.</p>	<p>The last item in the dropdown box is 131072.</p>
<p>In the FIFO MegaWizard Plug-In Manager, if you select the SCFIFO megafunction and set depth to a lower value than usedw[], the error message displayed does not show the correct depth. Instead, the error message displays (%1) as the depth value.</p>	<p>If you do not know the depth value of the FIFO, set depth to 1, and then check the depth value. You can now set the value of depth or usedw[] so that depth is greater than or equal to usedw[].</p>

Issue	Workaround
<p>In the DCFIFO MegaWizard Plug-In Manager, on page 3 under Are the FIFO clocks synchronized?, the option Yes, the clocks are synchronized, do not add clock synchronization latency. is not available.</p>	<p>If you want to use this option, generate the megafunction with the No, the clocks are not synchronized, add latency to handle unrelated clocks. option. Edit the megafunction file generated and change the line:</p> <pre>dcfifo_component.clocks_are_synchronized = "FALSE"</pre> <p>to</p> <pre>dcfifo_component.clocks_are_synchronized = "TRUE"</pre>
<p>In the DCFIFO MegaWizard Plug-In Manager, if you turn on Add circuit to synchronize 'aclr' with 'wrcrk', the TimeQuest Timing Analyzer might report recovery or removal failures.</p>	<p>Because read clock registers are guaranteed not to toggle after <code>aclr</code> de-assertion (the queue is empty), you may safely cut <code>aclr</code> as a false path.</p>
<p>When you generate a XAUI PHY megafunction with the XAUI PHY MegaWizard Plug-In Manager, if you select, on the General Options tab, Hard XAUI in the XAUI interface type box, the MegaWizard Plug-In Manager generates messages similar to the following:</p> <pre>Warning: <connection name> must be connected to an Avalon-ST sink</pre> <pre>Warning: <connection name> must be connected to an Avalon-ST source</pre> <p>If you turn on Include control and status ports on the Advanced Options tab, the MegaWizard Plug-In Manager generates the following additional message:</p> <pre>Warning: <connection name> cannot be both connected and exported</pre> <p>When you generate a XAUI PHY megafunction with the XAUI PHY MegaWizard Plug-In Manager, if you select, on the General Options tab, Soft XAUI in the XAUI interface type box, the MegaWizard Plug-In Manager also generates messages similar to the following:</p> <pre>Warning: alt_pma_0.tx_out_clk: Signal tx_out_clk[4] of type clk must have width [1]</pre> <pre>Warning: alt_pma_0.rx_recovered_clk: Signal rx_recovered_clk[4] of type clk must have width [1]</pre> <pre>Warning: sxau_i_0.tx_out_clk: Signal tx_out_clk[4] of type clk must have width [1]</pre> <pre>Warning: sxau_i_0.rx_recovered_clk: Signal rx_recovered_clk[4] of type clk must have width [1]</pre>	<p>These messages do not affect generation. You may safely ignore these messages.</p>

Issue	Workaround
<p>In the RAM: 2-PORT MegaWizard Plug-In Manager, on the Regs/Clkens/Aclrs page, some port names are missing:</p> <ul style="list-style-type: none"> ■ For simple dual-port RAM (with one read port and one write port) the port names data, wraddress, and wren are missing. ■ For true dual-port RAM (with two read/write ports) the port names data_b, wraddress_b, and wren_b are missing. 	<p>You can review all port names in the HDL file the MegaWizard Plug-In Manager generates.</p>
<p>In the ROM: 2-PORT MegaWizard Plug-In Manager, Resource Usage estimates are not available.</p>	<p>To determine the number of LUTs, registers, and RAM blocks required for your ROM: 2-PORT megafunction variation, compile the megafunction as an independent project with quartus_map and then refer to the Analysis & Synthesis report.</p>
<p>In the ROM:1-PORT MegaWizard Plug-In Manager, the Resource Usage box is empty.</p>	<p>Click on any option to populate the Resource Usage box.</p>
<p>VHDL designs and test benches that use VHDL std_developerskit fail to compile in ModelSim-Altera Starter Edition version 6.5e and ModelSim-Altera version 6.5e.</p>	<p>Re-implement your VHDL code using standard IEEE VHDL libraries so that code does not depend on the std_developerskit library or use ModelSim-Altera Edition version 6.5b.</p>
<p>The LPM_CLSHIFT MegaWizard Plug-In Manager does not correctly set the shift direction.</p>	<p>After you generate a left or right shifter with the MegaWizard Plug-In Manager, manually modify the MegaWizard-generated wrapper to add the direction.</p> <p>For example, add the <code>direction</code> line as bolded below:</p> <pre> lpm_clshift LPM_CLSHIFT_component (.data (data), .distance (distance), .direction (1'b1), .result (sub_wire0) // synopsys translate_off , .aclr (), .clken (), .clock (), .overflow (), .underflow () // synopsys translate_on); </pre> <p>Note: VCC (1'b1) creates a right shifter; GND (1'b0) creates a left shifter.</p>
<p>If you want to add an ALTFP_MATRIX_MULT megafunction to your project, you must manually include the ALTFPC_LIB library to your project.</p>	<p>Add the <code>altfpc_lib.v</code> or <code>altfpc_lib.vhd</code> file to your project.</p>

Issue	Workaround
<p>A parameter setting on a parent instance incorrectly overrides the default value of a similarly named parameter on a child instance. For example, if both the parent and child define a parameter <code>FOO</code> and, on the parent instance, you set the value of <code>FOO</code> to 7, the value of <code>FOO</code> on the child is (incorrectly) set to 7.</p>	<p>Modify the child instance to explicitly set the parameter to the default value. You can modify the child instance by editing your HDL source or by adding a <code>set_parameter</code> assignment to the Quartus Settings File (<code>.qsf</code>):</p> <pre>set_parameter -name FOO <value> -to <child instance name></pre>
<p>If, in the License Setup page of the Options dialog box, you browse to license file before all the licensed cores have been listed, the page stops listing the cores.</p>	<p>To see all licensed core or to view a license file, wait until the page lists all licensed cores before selecting any of them.</p>
Version 9.1 SP1	
<p>If you use the Remote System Upgrade configuration scheme to create a Programmer Object File (<code>.pof</code>) to update a device programmed with a <code>.pof</code> from a previous version of the Quartus II software, the Quartus II software version 9.1 SP1 might generate an internal error similar to the following:</p> <pre>Internal Error: Sub-system: PGMIO, File: /quartus/pgm/pgmio/pgmio_pof_diff.cpp, Line: 635 data do not match</pre>	<p>Use the version of the Quartus II software you used to generate the original <code>.pof</code> to create the updated <code>.pof</code>.</p>
<p>If you implement an <code>ALTCLKCTRL</code> megafunction and then run the Design Assistant, the Design Assistant might generate a message similar to the following:</p> <pre>Critical Warning: (Critical) Rule C101: Gated clock should be implemented according to the Altera standard scheme. Found 1 node(s) related to this rule.</pre>	<p>You may safely ignore this message.</p>
Version 9.1	
<p>If you use variable part select with two-dimensional arrays, the Quartus II software version 9.1 SP1 generates an error similar to the following:</p> <pre>no support for variable part select of multidimensional arrays (System Verilog)</pre>	<p>Do not use variable part select with two-dimensional arrays. Use multiple constant part selects such as <code>m[2+:1]</code>, and then choose from them.</p>
<p>The Quartus II software version 9.1 does not correctly synthesize <code>disable</code> statements when the <code>disable</code> statement refers to a labeled statement. For example, the following Verilog statements are not synthesized correctly:</p> <pre>label: out1 <=r1^r2; disable label;</pre>	<p>Rewrite your code so that the statement is surrounded by a begin-end block and name the block after the begin keyword. For example, the following is synthesized correctly:</p> <pre>begin: label out1 <=r1^r2; disable label; end;</pre>

Issue	Workaround
If you attempt to add the ALTFP_MATRIX_INV megafunction to your project with the MegaWizard Plug-In Manager, the MegaWizard Plug-In Manager fails to add the altfpc_lib library to your project.	Manually include the <code>altfpc_lib.v</code> or <code>altfpc_lib.vhd</code> file in the project.
<p>When a RAM is inferred under all the following conditions, the synthesized circuit is not guaranteed to be correct:</p> <ul style="list-style-type: none"> ■ The read from and write to the memory occur in the same always block or process. ■ The always block or process that reads/writes to the memory array is combinational. <p>The write assignment happens before the read.</p>	To solve this problem, either disable RAM inference or rewrite the HDL description of the RAM. RAM inference can be disabled by setting the <code>auto_ram_recognition</code> variable to Off . Alternatively, a different HDL description can be used for the RAM (refer to the “Inferring Memory Functions from HDL Code” chapter in the <i>Quartus II Handbook</i>).

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 10.0	
After installation of the Altera Complete Design Suite or any of its components, neither the ACDS nor its components appear in the Windows Add or Remove Programs dialog box.	To uninstall the ACDS or any of its components, use the Windows Start menu to run the uninstaller.
<p>If you run the stand-alone Quartus II SignalTap II Logic Analyzer, and then click About Quartus II SignalTap II Logic Analyzer on the Help menu, the Quartus II SignalTap II Logic Analyzer exits with an error similar to the following:</p> <pre>Internal Error: Sub-system: QUI, File: /quartus/sys/qui/qui_help_menu.cpp, Line: 256 Cannot load library sys_mdb.dll: The specified module could not be found.</pre>	Do not click the About Quartus II SignalTap II Logic Analyzer command.
Dialog boxes that open or select files (such as Open , Open Project , Save As) can be very slow to open.	<p>You can speed up these dialog boxes by adding to your <code>quartus.ini</code> file the following line:</p> <pre>use_native_windows_file_dialogs=on</pre> <p>This line speeds up the dialog boxes, but reduces their functionality.</p>
Internet Explorer browser security settings can prevent search result links from www.altera.com to Quartus II Help topics from functioning correctly.	Add <code>quartushelp.altera.com\current</code> as an IE trusted site to your Internet Explorer browser, and then restart your browser.

Issue	Workaround
<p>After you install the Quartus II software version 10.0 to a Windows 7 operating system, the following message is generated by the operating system:</p> <pre>This program might not have installed correctly.</pre>	<p>This message appears because Altera has not applied to the Windows 7 Software Logo Program</p> <p>You can safely ignore this message.</p>
<p>The MegaWizard Plug-In Manager cannot output a Block Symbol File (.bsf) to a path that contains spaces, for example, if you attempt to generate a .bsf to C:\New Folder\myproject, generation of the .bsf fails.</p>	<p>Ensure that the destination path for your .bsf files does not contain spaces.</p>

Linux Platforms Only

Issue	Workaround
Version 10.0	
<p>On computers running SUSE Enterprise 11, the Altera Installer GUI might fail to open.</p>	<p>To open the Altera Installer GUI, first turn off X Authentication.</p>
<p>On computers running 64-bit Red Hat Enterprise Linux, attempting to run the Altera Installer directly from the DVD drive fails with the following message:</p> <pre>Not enough space left in . (0 KB) to decompress ./altera_installer.sh</pre>	<p>Run the Altera Installer (altera_installer.sh) from a local directory.</p>
<p>The Altera Installer on the Linux DVD offers the Quartus II Web Edition Software; however, the Linux DVD does not contain that software.</p>	<p>To obtain the Quartus II Web Edition Software for Linux, download it from the Altera Download Center website.</p>
<p>For 64-bit Red Hat Enterprise Linux, upgrading the kernel from version 2.6.9-67 to version 2.6.9-89 can improve the performance of the Quartus II software version 10.0.</p>	

Issue	Workaround
<p>If you are using a shared MATLAB environment, and during installation of the standalone DSP Builder you select Skip setup, DSP Builder cannot communicate with MATLAB because the Altera Installer fails to create a startup.m file. .</p>	<p>Manually configure the MATLAB environment by performing the following steps:</p> <ol style="list-style-type: none"> 1. In MATLAB, on the File menu, click Set Path. 2. For the standard blockset, add the following paths: <ul style="list-style-type: none"> ■ <code><quartus path>/dsp_builder/bin</code> ■ <code><quartus path>/dsp_builder/bin/matlab</code> ■ <code><quartus path>/dsp_builder/bin/mdllibrary</code> 3. For the advanced blockset, add the following paths: <ul style="list-style-type: none"> ■ <code><quartus path>/dspba/Blocksets</code> ■ <code><quartus path>/dspba/Blocksets/BaseBlocks</code> ■ <code><quartus path>/dspba/Blocksets/FFTBlocks</code> ■ <code><quartus path>/dspba/Blocksets/Filters</code> ■ <code><quartus path>/dspba/Blocksets/ModelBus</code> ■ <code><quartus path>/dspba/Blocksets/ModelPrim</code> ■ <code><quartus path>/dspba/Blocksets/WaveformSynthesis</code> ■ <code><quartus path>/dspba/Docs</code> ■ <code><quartus path>/dspba/Docs/Help</code> 4. Add the following paths to the LD_LIBRARY_PATH environment variable: <ul style="list-style-type: none"> ■ <code><quartus path>/quartus/linux</code> ■ <code><quartus path>/dsp_builder/bin</code> ■ <code><quartus path>/dspba/Blocksets/BaseBlocks</code> 5. Create a startup.m file in \$HOME/matlab and include the following lines: <ul style="list-style-type: none"> ■ <code>addpath(' <quartus path>/dsp_builder/bin')</code> ■ <code>addpath(' <quartus path>/dsp_builder/bin/matlab')</code> ■ <code>addpath(' <quartus path>/dsp_builder/bin/mdllibrary'</code> <code>)</code> ■ <code>javaaddpath(' <quartus path>/dsp_builder/bin/dspb_blocks.jar')</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets')</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets/BaseBlocks'</code> <code>)</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets/FFTBlocks')</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets/Filters')</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets/ModelBus')</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets/ModelPrim')</code> ■ <code>addpath(' <quartus path>/dspba/Blocksets/WaveformSynthesis')</code> ■ <code>addpath(' <quartus path>/dspba/Docs')</code> ■ <code>addpath(' <quartus path>/dspba/Docs/Help')</code> ■ <code>addpath(genpath(' <quartus path>/Examples'))</code>

Issue	Workaround
<p>If your quartus2.qreg file includes the line:</p> <pre>General\Check_for_New_Info_Message_at_Startup=Yes</pre> <p>and you attempt to start the Quartus II GUI, startup fails.</p>	<p>In your quartus2.qreg file, change the line</p> <pre>General\Check_for_New_Info_Message_at_Startup=Yes</pre> <p>to</p> <pre>General\Check_for_New_Info_Message_at_Startup=No</pre> <p>The quartus2.qreg file is located in ~/altera.quartus.</p>
<p>The GUI can be slow in some Linux environments, especially if you use a remote display technology such as VNC or NX.</p>	<p>In the shell environment, set the following environment variable before you start the Quartus II software:</p> <pre>QUARTUSII_DISABLE_INTERNAL_ANTI_ALIASING=on</pre> <p>This line speeds up the GUI, but might reduce graphics display quality and text might appear jagged.</p>

Device Family Issues

Arria II GX

Issue	Workaround
Version 10.0	
<p>If you attempt to generate the ALTGXB megafunction from a command line using</p> <pre>qmegawiz -silent</pre> <p>generation fails with messages similar to the following:</p> <pre>Error: The GXB PLL 'CMU' parameter 'input_clock_frequency' is set to an illegal value of '155.52 MHz'. The value is illegal when the device speed grade is '4', the parameter 'base_data_rate' is set to '2967.0 Mbps', and the parameter 'Pll Type' is set to 'CMU' on atom 'test_alt4gxb_t3t6:test_alt4gxb_t3t6_component tx_pll_alt0'</pre> <pre>Error: The 'GXB PLL' parameter 'm' is set to an illegal value of '1'. The reference clock frequency to the PLL PFD (phase-frequency detector), which is input_clock_frequency ('155.52 MHz') \ n ('1'), must be the same as the feedback frequency to the PLL PFD, which is base_data_rate ('2967.0 Mbps') \ 2 \ m on atom 'test_alt4gxb_t3t6:test_alt4gxb_t3t6_component tx_pll_alt0'</pre> <pre>Error: The 'GXB PLL' parameter 'n' is set to an illegal value of '1' on atom 'test_alt4gxb_t3t6:test_alt4gxb_t3t6_component tx_pll_alt0'. The value of n is restricted based on the min and max reference clocks to the PLL PFD (phase-frequency detector) for the speed grade of 4 and the specific Pll Type of 'CMU'. For non-basic protocol configurations, the value of N is fixed.</pre>	<p>Use the MegaWizard Plug-In Manager GUI to configure and generate your ALTGXB megafunction.</p>
Version 9.1 SP1	
<p>In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 1. However, Chapter 7 “External Memory Interfaces in Arria II GX Devices” in Volume 1 of the Arria II GX Device Handbook numbers DLLs from 1 to 2.</p>	<p>Use numbers 0 to 1 to refer to DLLs when you make location assignments in the Quartus II software.</p>

Issue	Workaround
Version 9.1	
<p>For Stratix III, Stratix IV, Hardcopy III, Hardcopy IV, and Arria II GX devices, because the PCI_IO logic option assignment is not honored by the Assembler during programming file generation, the on-chip clamp diode is always enabled for the 3.0V-PCI/PCI-X I/O standard; for 3.3/3.0V-LVTTL/LVCMOS I/O standard, the on-chip clamp diode is always disabled.</p> <p>This issue is corrected in the Quartus II software version 10.0.</p>	<p>If you need to either disable the on-chip clamp diode for 3.0V-PCI/PCI-X I/O or enable the on-chip clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O, Altera recommends that you recompile the design using the Quartus II software version 10.0. However, in Quartus II 10.0, the PCI_IO logic option is obsolete and replaced with the CLAMPING_DIODE logic option for Stratix III, Stratix IV, Hardcopy III, Hardcopy IV and Arria II GX devices.</p> <p>Altera also recommends that you re-evaluate the effect of using the CLAMPING_DIODE assignment for design compilation. If the default settings of on-chip clamp diode meet your design requirements, you may continue use the same Quartus II software version that you used previously to compile the design</p> <p>If you cannot upgrade to the Quartus II software version 10.0, you can use an external clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O or refer to the solution available at http://www.altera.com/support/kdb/solutions/rd04092010_488.html</p>

Cyclone III

Issue	Workaround
Version 10.0	
<p>For Cyclone III and Cyclone III LS devices, on the Configuration page of the Device and Pin Options dialog box, the Enable input tri-state on active configuration pins in user mode option is not enabled properly.</p>	<p>To enable input tri-state on active configuration pins, use the following assignment in the Quartus Settings File (.qsf):</p> <pre>set_global_assignment -name TRI_STATE_SPI_PINS ON</pre>

Cyclone IV E

Issue	Workaround
Version 10.0	
<p>On the Configuration page of the Device and Pin Options dialog box, the Enable input tri-state on active configuration pins in user mode option is not enabled properly.</p>	<p>To enable input tri-state on active configuration pins, use the following assignment in the Quartus Settings File (.qsf):</p> <pre>set_global_assignment -name TRI_STATE_SPI_PINS ON</pre>

Cyclone IV GX

Issue	Workaround
Version 10.0	
<p>All dropdown boxes in the ALTLVDS_RX megafunction are empty. No options are available.</p>	<p>To populate the ALTLVDS_RX dropdown boxes, perform the following steps:</p> <ol style="list-style-type: none"> 1. On page 2a of the MegaWizard Plug-In Manager, in the Which device family will you be using? box, select Stratix II GX. 2. Click Next. 3. On the Parameter Settings page, click the Receiver settings tab. 4. Turn off Use 'rx_cda_reset' input port. 5. Click the General tab. 6. Turn off Match project/default. 7. In the Currently selected device family box, select Cyclone IV GX. <p>The dropdown boxes are now populated.</p>
<p>If you attempt to instantiate two CPRI channels with PLL phase circuitry detector (PFD) feedback turned on, the Fitter generates errors similar to the following:</p> <pre>Error: Following nodes use the same resource INTERQUAD_TXRX_CLK_X0_Y28_N0_I3 Error: Node "lib_xcvr_channel_module:channel_inst0 rx_pcs_clkout" is currently placed at location RXPCS_X0_Y16_N8 with a Global Signal type of Auto Error: Node "lib_xcvr_channel_module:channel_inst1 rx_pcs_clkout" is currently placed at location RXPCS_X0_Y22_N8 with a Global Signal type of Auto</pre> <p>These errors occur because the Fitter is unable to place the two CPRI channel automatically.</p>	<p>To place two CPRI channels with PLL PFD feedback enabled into one quad, use location assignments to place the channels onto Channel 0 and Channel 2.</p>
<p>Cyclone IV GX transceiver Rx does not support a clock tolerance of +/- 500 PPM or +/- 1000 PPM.</p>	<p>In the ALTGX MegaWizard Plug-In Manager, select a clock tolerance other than +/- 500 PPM or +/- 1000 PPM in What is the acceptable PPM threshold between the receiver CDR VDO and the receiver input reference clock? on the PLL/Ports tab of the Parameter Settings page.</p>

<p>In the ALTGX MegaWizard Plug-In Manager, on the Rx Analog page, the What is the receiver termination resistance? box lists 85, 100, and 150 Ohms; however, only 85 and 150 Ohms are valid. If you select 100 Ohms, the Analysis & Synthesis report displays the following message:</p> <pre>Warning: MGL_INTERNAL_WARNING: (The parameter value is not one of the pre-specified values in the value list.) alt_c3gxb receiver_termination The value assigned is oct_100_ohms and the valid value list is OCT_85_OHMS OCT_150_OHMS</pre>	<p>If you select 100 Ohms, the ALXGX MegaWizard applies the default receiver termination resistance. You may safely ignore the message.</p>
<p>In the ALTGX MegaWizard Plug-In Manager, on the Tx Analog page, the Select the Transmitter termination resistance box lists 85, 100, and 150 Ohms; however, only 100 and 150 Ohms are valid. If you select 85 Ohms, the Analysis & Synthesis report displays the following message:</p> <pre>Warning: MGL_INTERNAL_WARNING: (The parameter value is not one of the pre-specified values in the value list.) alt_c3gxb transmitter_termination The value assigned is oct_85_ohms and the valid value list is OCT_100_OHMS OCT_150_OHMS</pre>	<p>If you select 85 Ohms, the ALXGX MegaWizard applies the default transmitter termination resistance of 100 Ohms. You may safely ignore the message.</p>
<p>If you implement an ALTGX megafunction in Deterministic Latency mode, the Quartus II software might generate messages similar to the following:</p> <pre>Warning (10541): VHDL Signal Declaration warning at c4gx_test.vhd(62): used implicit default value for signal "pll_reconfig_done" because signal was never assigned a value or an explicit default value. Use of implicit default value may introduce unintended design optimizations. Warning (10036): Verilog HDL or VHDL warning at c4gx_test.vhd(142): object "wire_receive_pcs0_signaldetect" assigned a value but never read</pre>	<p>You may safely ignore these messages.</p>
<p>During static simulation, instances that are controlled by an ALTGX_RECONFIG megafunction generated with VHDL cannot be synchronized while the ALTGX_RECONFIG megafunction is reconfiguring them.</p>	<p>Perform static simulation before reconfiguration or reset the PMA with PMA reconfiguration.</p>
<p>For designs that target Cyclone IV GX devices, the Compiler might be unable to place a <code>refclk</code> pin in a location that feeds the transceiver PLLs.</p>	<p>Use location assignments to place the <code>refclk</code> pin and the PLL.</p>
Version 9.1 SP2	
<p>Using a post-fit netlist to simulate (with or without timing) a VHDL design that uses the XAUI protocol might not work properly.</p>	<p>Use a mixed-language simulator based on the Verilog HSSI model.</p>

Stratix II GX

Issue	Workaround
Version 10.0	
<p>In the ALTGX MegaWizard Plug-In Manager, if on page 2a you set Which device family will you be using? to any family other than Stratix II GX, and then on page 3 you turn off Match project/default, and set Currently selected device family to Stratix II GX, the MegaWizard Plug-In Manager becomes unresponsive.</p>	<p>If the MegaWizard Plug-In Manager is unresponsive, close it and start again.</p> <p>If you want to change the device family your ALTGX megafunction targets, change Which device family will you be using? on page 2a.</p>

Stratix III

Issue	Workaround
Version 10.0	
<p>On the Configuration page of the Device and Pin Options dialog box, the Enable input tri-state on active configuration pins in user mode option is not enabled properly.</p>	<p>To enable input tri-state on active configuration pins, use the following assignment in the Quartus Settings File (.qsf):</p> <pre>set_global_assignment -name TRI_STATE_SPI_PINS ON</pre>
Version 9.1 SP1	
<p>In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 3. However, Chapter 8 “External Memory Interfaces in Stratix III Devices” in Volume 1 of the <i>Stratix III Device Handbook</i> numbers DLLs from 1 to 4.</p>	<p>Use numbers 0 to 3 to refer to DLLs when you make location assignments in the Quartus II software.</p>
Version 9.1	
<p>For Stratix III, Stratix IV, Hardcopy III, Hardcopy IV, and Arria II GX devices, because the PCI_IO logic option assignment is not honored by the Assembler during programming file generation, the on-chip clamp diode is always enabled for the 3.0V-PCI/PCI-X I/O standard; for 3.3/3.0V-LVTTL/LVCMOS I/O standard, the on-chip clamp diode is always disabled.</p> <p>This issue is corrected in the Quartus II software version 10.0.</p>	<p>If you need to either disable the on-chip clamp diode for 3.0V-PCI/PCI-X I/O or enable the on-chip clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O, Altera recommends that you recompile the design using the Quartus II software version 10.0. However, in Quartus II 10.0, the PCI_IO logic option is obsolete and replaced with the CLAMPING_DIODE logic option for Stratix III, Stratix IV, Hardcopy III, Hardcopy IV and Arria II GX devices.</p> <p>Altera also recommends that you re-evaluate the effect of using the CLAMPING_DIODE assignment for design compilation. If the default settings of on-chip clamp diode meet your design requirements, you may continue use the same Quartus II software version that you used previously to compile the design</p> <p>If you cannot upgrade to the Quartus II software version 10.0, you can use an external clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O or refer to the solution available at http://www.altera.com/support/kdb/solutions/rd04092010_488.html</p>

Stratix IV

Issue	Workaround
Version 10.0	
On the Configuration page of the Device and Pin Options dialog box, the Enable input tri-state on active configuration pins in user mode option is not enabled properly.	To enable input tri-state on active configuration pins, use the following assignment in the Quartus Settings File (.qsf): <pre>set_global_assignment -name TRI_STATE_SPI_PINS ON</pre>
Some GLOBAL_SIGNAL assignments might be lost if you create a new project revision from an existing revision.	If the base revision contains GLOBAL_SIGNAL assignments, check the new revision for missing assignments.
On page 4 of the ALTLVDS_RX MegaWizard Plug-In Manager, the Use shared PLL(s) for receivers and transmitters box is not available.	To enable the Use shared PLL(s) for receivers and transmitters box, on page 3 turn on Implement Deserializer circuitry in logic cells .
On the Receiver settings tab of the Parameter Settings page of the ALTLVDS_RX MegaWizard Plug-In Manager, if you turn on Use 'rx_channel_data_align' input port , generation fails with a message similar to the following: Error: Port rx_data_align_reset is being set to the state USED which is incompatible with the current settings of IMPLEMENT_IN_LES(OFF), INTENDED_DEVICE_FAMILY(Stratix IV), rx_data_align(UNDEFINED). The legal state is UNUSED	Turn off Use 'rx_channel_data_align' input port .
In the FIFO MegaWizard Plug-In Manager, on the Parameter Settings page, if you turn off Show-ahead synchronous FIFO mode and select MLAB under What should the memory block type be? on the Rdreq Option, Blk Type , and then on the Optimization, Circuitry Protection tab, select No (smallest area) under Would you like to register the output to maximize performance but use more area? , the generated SCFIFO behaves incorrectly.	Under What should the memory block type be? on the Rdreq Option, Blk Type tab of the Parameter Settings page, select a memory block type other than MLAB (that is, select Auto, M9K, or M144K).
On the General Options tab of the 10GBase-R PHY MegaWizard Plug-In Manager, if you set Number of Channels to a value greater than 4, generation fails with the message: Generation FAILED	Specify a value between 1 and 4. If you require more than 4 channels, instantiate additional 10GBase-R PHY megafunctions.

Issue	Workaround
Version 9.1	
<p>For Stratix III, Stratix IV, Hardcopy III, Hardcopy IV, and Arria II GX devices, because the PCI_IO logic option assignment is not honored by the Assembler during programming file generation, the on-chip clamp diode is always enabled for the 3.0V-PCI/PCI-X I/O standard; for 3.3/3.0V-LVTTL/LVCMOS I/O standard, the on-chip clamp diode is always disabled.</p> <p>This issue is corrected in the Quartus II software version 10.0.</p>	<p>If you need to either disable the on-chip clamp diode for 3.0V-PCI/PCI-X I/O or enable the on-chip clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O, Altera recommends that you recompile the design using the Quartus II software version 10.0. However, in Quartus II 10.0, the PCI_IO logic option is obsolete and replaced with the CLAMPING_DIODE logic option for Stratix III, Stratix IV, Hardcopy III, Hardcopy IV and Arria II GX devices.</p> <p>Altera also recommends that you re-evaluate the effect of using the CLAMPING_DIODE assignment for design compilation. If the default settings of on-chip clamp diode meet your design requirements, you may continue to use the same Quartus II software version that you used previously to compile the design</p> <p>If you cannot upgrade to the Quartus II software version 10.0, you can use an external clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O or refer to the solution available at http://www.altera.com/support/kdb/solutions/rd04092010_488.html</p>
See also Stratix IV GX	

Stratix IV GX

Issue	Workaround
Version 10.0	
<p>In the ALTGX MegaWizard Plug-In Manager, on each of the Main PLL and Alt PLL tabs of the Reconfiguration Settings page, the dropdown boxes of the top two options are mismatched:</p> <ul style="list-style-type: none"> ■ What is the PLL logical reference index(used in reconfiguration)? ■ What is the selected input clock source for the Rx/Tx PLLs? <p>The dropdown box to the right of What is the PLL logical reference index (used in reconfiguration)? sets the What is the selected input clock source for the Rx/Tx PLLs? option; likewise, the dropdown box to the right of What is the selected input clock source for the Rx/Tx PLLs? sets the What is the PLL logical reference index (used in reconfiguration)? option.</p>	<p>Use the dropdown box to the right of What is the PLL logical reference index (used in reconfiguration)? to set the What is the selected input clock source for the Rx/Tx PLLs? option and use the dropdown box to the right of What is the selected input clock source for the Rx/Tx PLLs? to set the What is the PLL logical reference index (used in reconfiguration)? option.</p>
<p>If you attempt to instantiate an ALTGX megafunction with two data channels located in different transceiver banks, the Quartus II software fails to merge two edge PLLs together, even if they have the same index and belong to the same reconfiguration group.</p>	<p>To merge the two edge PLLs together, use location assignments to place the two edge PLLs to the same location and ensure that their INCLK_INPUT_PERIOD settings are the same.</p>

Issue	Workaround
<p>In the ALTGX MegaWizard Plug-In Manager, if you select Basic (PMA Direct) in the Which protocol will you be using? box and XN in the Which subprotocol will you be using? box on page 3, turn on Use Auxiliary Transmitter (ATX) PLL on page 4, and then return to page 3 and select None in the Which subprotocol will you be using? box, the MegaWizard Plug-In Manager does not turn off the Use Auxiliary Transmitter (ATX) PLL box on page 4. As a result, the ALTGX megafunction incorrectly enables an ATX PLL.</p>	<p>Before you change the subprotocol from XN to None on page 3, turn off Use Auxiliary Transmitter (ATX) PLL on page 4.</p>
<p>If you instantiate an ALTGX instance with the GIGE protocol and compiled, Analysis and Synthesis generates errors similar to following:</p> <p>Error: gige_alt4gxb:gige_alt4gxb_component receive_pcs0 parameter Rate match pattern 1 of 0 has a length of 1, which does not match its corresponding Size of the rate_match_pattern1 and rate_match_pattern2 parameters of 20</p> <p>Error: gige_alt4gxb:gige_alt4gxb_component receive_pcs0 parameter Rate match pattern 2 of 0 has a length of 1, which does not match its corresponding Size of the rate_match_pattern1 and rate_match_pattern2 parameters of 20</p>	<p>To correct the mismatched settings, activate the validator by changing the number of channels (or any other setting) in the ALTGX MegaWizard interface.</p>
<p>In the ALTGX_RECONFIG MegaWizard Plug-In Manager, if you turn on Analog controls, Data rate division in TX, and Channel and TX PLL select/reconfig, and then turn on Enable continuous write of all the words needed for reconfiguration, the instantiated megafunction exhibits incorrect busy behavior.</p>	<p>If you turn on Analog controls, Data rate division in TX, and Channel and TX PLL select/reconfig, turn off Enable continuous write of all the words needed for reconfiguration.</p> <p>If you turn on Enable continuous write of all the words needed for reconfiguration, turn on only Channel and TX PLL select/reconfig; turn off Analog controls and Data rate division in TX.</p>
Version 9.1 SP1	
<p>In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 3. However, Chapter 7 “External Memory Interfaces in Stratix IV Devices” in Volume 1 of the <i>Stratix IV Device Handbook</i> numbers DLLs from 1 to 4.</p>	<p>Use numbers 0 to 3 to refer to DLLs when you make location assignments in the Quartus II software.</p>
Version 9.1	
<p>With the ALTGX megafunction, if your design uses dynamic protocol reconfiguration from x4 bonding in basic mode to XAUI or PCIe x4 protocols, simulation fails.</p>	
<p>If you enable serial loopback between two PMA Direct mode ALTGX transceivers placed in different channels or quads, communication between the transceivers may fail.</p>	<p>Enable serial loopback only between input and output pins on the same channel or quad.</p>

Stratix IV GT

Issue	Workaround
Version 9.1	
<p>If you import a project created with the Quartus II software version 9.1 or earlier, during fitting, timing analysis, or power analysis, incorrect voltage settings of the VCC, VCCA, or VCCD power rails can generate the following error message:</p> <pre>Error: The supply voltage value <voltage> applied to the <power supply> power rail is illegal for the currently selected device.</pre>	<p>Select supply voltage values with the Voltage tab of the Settings dialog box.</p>

Stratix V

Issue	Workaround
Version 10.0	
<p>If you attempt to compile a design that targets a Stratix V device, compilation might fail with the following error:</p> <pre>Error: Unable to generate the EDA simulation netlist files because the Quartus II software does not currently support gate-level simulation for the Stratix V devices</pre>	<p>Before you start a compilation, turn off the netlist writer by performing the following steps:</p> <ol style="list-style-type: none"> 1. On the Assignments menu, click Settings. 2. In the Category list, select Simulation under EDA Tool Settings. 3. In the Tool name box, select <None>. <p>To perform a nativelylink RTL simulation, after compilation is completed, select your EDA tool in the Tool name box of the EDA Settings dialog box.</p>
<p>If you add a MAXIMUM_CURRENT or MINIMUM_CURRENT Quartus Settings File (.qsf) assignment to any of the following I/O standards:</p> <ul style="list-style-type: none"> ■ Differential 1.2-V SSTL ■ Differential 1.25-V SSTL ■ Differential 1.35-V SSTL ■ Differential 1.5-V SSTL ■ Differential 1.2-V HSUL ■ SSTL-15 ■ SSTL-135 ■ SSTL-125 ■ SSTL-12" ■ 1.2-V HSUL <p>compilation fails with a message similar to the following:</p> <pre>Internal Error: Sub-system: SIN, File: /quartus/tsm/sin/sin_titan_buffer_netli st_builder.cpp, Line: 197</pre>	<p>Remove the assignment.</p>

<p>The ALTMULT_ADD megafunction does not support VHDL behavior models with the Stratix V device family.</p>	<p>Use a co-simulator and VHDL wrapper code to generate a Verilog HDL simulation model or simulate with a ClearBox-generated design.</p>
<p>Although all pins within a group of I/O banks must share a single V_{CCPD} pin, the Fitter does not enforce this restriction.</p> <p>In Stratix V devices, a single V_{CCPD} pin is shared with a group of I/O banks. I/O bank labels with the same number (such as 7A, 7B, 7C, and 7D) form a group that share the same V_{CCPD} pin, with the exception of Banks 3A, 3B, 3C, and 3D—Banks 3A and 3B form a group with one V_{CCPD} pin; Banks 3C and 3D form a different group with its own V_{CCPD} pin.</p> <p>For example, an I/O bank that uses a 3.0-V V_{CCPD} pin forces all other I/O banks in the same group to use 3.0-V V_{CCPD}; an I/O bank that uses a 2.5-V V_{CCPD} pin forces all other I/O banks in the same group to use 2.5-V V_{CCPD}.</p> <p>For details of supported VCCIO voltage levels available for VCCPD pins, refer to the <i>I/O Standards and Voltage Levels</i> section in the <i>I/O Features in Stratix V Devices</i> chapter of the <i>Stratix V Device Handbook</i>.</p>	<p>If you use output or bidirectional pins with the 3.3 V-LVTTL/LVCMOS I/O standard, you must enforce the V_{CCPD} restriction manually with location assignments.</p>
<p>For designs that target Stratix V devices, the Fitter does not perform <code>core_clk</code> connection legality checks.</p>	
<p>In designs that use LVDS, all LVDS SERDES groups use the same I/O standard and all data pins connecting to LVDS SERDES channels must use a differential I/O standard.</p>	<p>Ensure that all LVDS SERDES groups use the same I/O standard and that all data pins connecting to LVDS SERDES channels use a differential I/O standard.</p>
<p>Routing might fail due to congestion if different locally routed signals are used to clock input registers and output registers of I/Os placed (by the Fitter or by user location assignments) in the same location.</p>	<p>Promote one of the failing signals to use the global or quadrant clock network.</p>
<p>If you use the zero delay buffer operation mode, the Fitter can't place PLLs and generates messages similar to the following:</p> <pre>Error: Could not place pin <pin name></pre>	<p>Manually place the external clock output node with a location assignment. The location depends on the PLL location and the target device.</p>
<p>On the Systolic/Preload page of the ALTMULT_ADD MegaWizard Plug-In Manager, if you turn on Enable systolic delay registers, generation fails with messages similar to the following:</p> <pre>Error: Illegal parameter value: SYSTOLIC_DELAY1 and SYSTOLIC_DELAY3 are used without chainin port Error: Assertion error: The current megafunction is configured for use with the clear box feature and cannot be used when the clear box feature is disabled</pre>	<p>The systolic delay registers feature is not available in the current release of the Stratix V ALTMULT_ADD megafunction. Do not turn on Enable systolic delay registers.</p>
<p>During timing analysis of a soft XAUI PHY megafunction, the TimeQuest Timing Analyzer might report setup violations within the <code>mgmt_clk_clk</code> domain and between the <code>mgmt_clk_clk</code> and another clock domain. The TimeQuest Timing Analyzer might also report hold violations.</p>	<p>You may safely ignore these errors. For details, refer to the <i>XAUI PHY</i> chapter of the <i>MegaCore IP Release Notes and Errata</i>.</p>

HardCopy

Issue	Workaround
Version 9.1 SP1	
<p>In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 3. However, Chapter 7 “External Memory Interfaces in HardCopy IV Devices” in Volume 1 of the <i>HardCopy IV Device Handbook</i> and Chapter 7 “External Memory Interfaces in HardCopy III Devices” in Volume 1 of the <i>HardCopy III Device Handbook</i> number DLLs from 1 to 4.</p>	<p>Use numbers 0 to 3 to refer to DLLs when you make location assignments in the Quartus II software.</p>
Version 9.1	
<p>For Stratix III, Stratix IV, Hardcopy III, Hardcopy IV, and Arria II GX devices, because the PCI_IO logic option assignment is not honored by the Assembler during programming file generation, the on-chip clamp diode is always enabled for the 3.0V-PCI/PCI-X I/O standard; for 3.3/3.0V-LVTTL/LVCMOS I/O standard, the on-chip clamp diode is always disabled.</p> <p>This issue is corrected in the Quartus II software version 10.0.</p>	<p>If you need to either disable the on-chip clamp diode for 3.0V-PCI/PCI-X I/O or enable the on-chip clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O, Altera recommends that you recompile the design using the Quartus II software version 10.0. However, in Quartus II 10.0, the PCI_IO logic option is obsolete and replaced with the CLAMPING_DIODE logic option for Stratix III, Stratix IV, Hardcopy III, Hardcopy IV and Arria II GX devices.</p> <p>Altera also recommends that you re-evaluate the effect of using the CLAMPING_DIODE assignment for design compilation. If the default settings of on-chip clamp diode meet your design requirements, you may continue use the same Quartus II software version that you used previously to compile the design</p> <p>If you cannot upgrade to the Quartus II software version 10.0, you can use an external clamp diode for 3.3/3.0V-LVTTL/LVCMOS I/O or refer to the solution available at http://www.altera.com/support/kdb/solutions/rd04092010_488.html</p>
<p>In the ALTDQ_DQS MegaWizard, if the RLDRAMII mode is set to x18 or x36 and both the Simulation Model and Generate netlist options are turned on, the following message is generated:</p> <pre>Failed to generate the synthesis netlist file</pre>	<p>Use the megafuction-generated variation file as input to third party synthesis tools.</p>

SOPC Builder Issues

Issue	Workaround
Version 10.0	
<p>SOPC Builder requires Stratix II device family information to analyze IP port results. If Stratix II device family information is not installed with the Quartus II software version 10.0, IP port analysis fails with the following error:</p> <pre>Stratix II is not a valid device family</pre>	<p>Install Stratix II device family information.</p>

Issue	Workaround
<p>SOPC Builder requires Stratix II device family information during system generation. If Stratix II device family information is not installed with the Quartus II software version 10.0, system generation fails with the following error:</p> <pre>Family name 'Stratix II' is illegal</pre>	<p>Install Stratix II device family information.</p>
<p>For all UniPHY-based memory controllers and the Traffic Generator, SOPC Builder cannot recognize System Verilog files. As a result, System Verilog files are not automatically compiled during ModelSim simulation.</p>	<p>Manually compile all System Verilog files in ModelSim before using the simulation flow.</p>
<p>If you connect a custom component that contains an Avalon Memory-Mapped slave interface without an address bus to a clock-crossing bridge, ModelSim generates errors similar to the following:</p> <pre># ** Failure: (vsim-3807) Types do not match between component and entity for port "slave_address". # Time: 0 ps Iteration: 0 Instance: /clock_crossing_0.vhd Line: 247 # ** Failure: (vsim-3807) Types do not match between component and entity for port "slave_nativeaddress". # Time: 0 ps Iteration: 0 Instance: /clock_crossing_0.vhd Line: 250 # ** Failure: (vsim-3807) Types do not match between component and entity for port "master_nativeaddress". # Time: 0 ps Iteration: 0 Instance: /clock_crossing_0.vhd Line: 259</pre> <p>These errors are caused by a signal type mismatch between the address signal of the clock-crossing bridge and the instantiation of the bridge in the top-level module.</p>	<p>Add a slave address signal with a width equal to one or larger to the Avalon Memory-Mapped slave interface. You can use any valid name for the address signal.</p> <p>You can omit using this slave address signal if it is not required in your design.</p>
<p>In the System Console, if you run add_service pli_master, the path returned by the command does not match the location where the service was added.</p>	<p>Use get_service_paths to determine the location of your new service.</p>

Issue	Workaround
The Tcl parser used by SOPC Builder uses the Tcl version 8.0 API. The Quartus II software uses the Tcl version 8.5 API. Some Tcl syntax, such as regular expressions, may behave differently in your component's hw.tcl folder and in the Quartus II Tcl Interpreter.	Use the Tcl version 8.0 API command set.
<p>When adding components to your system, SOPC Builder might generate messages similar to the following:</p> <pre>Warning: set_module_property on deprecated property class_name, please use name instead Warning: set_module_property on deprecated property preview_elaboration_callback, please use elaboration_callback instead Warning: set_module_property on deprecated property preview_validation_callback, please use validation_callback instead</pre>	You may safely ignore these messages.

Antivirus Verification

The Altera Complete Design Suite version 10.0 has been verified virus-free using the following software:

McAfee VirusScan Enterprise + AntiSpyware Enterprise 8.7.0i
 Scan Engine Version: 5400.1158
 DAT Version: 6016.0000

Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

<http://www.altera.com/support/kdb/kdb-index.jsp>

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 10.0:

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.0							
10018135	10076715	10090961	10146987	10305417	10428910	10464896	10477062
10487945	10495683	10513776	10534060	10541186	10543377	10563347	10575809
10577537	10578289	10583577	10585183	10586447	10595755	10601142	10609607
10619100	10622245	10622998	10624996	10629914	10630273	10630624	10632019

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.0							
10633363	10633909	10634383	10636825	10638789	10639706	10646548	10646783
10647247	10647259	10650861	10651632	10654622	10655958	10656213	10656218
10658793	10661991	10662857	10662863	10664763	10665371	10666006	10666694
10667300	10667646	10667953	10669575	10670153	10670348	10670484	10670710
10671588	10673167	10673206	10677584	10679252	10679281	10679646	10679940
10679952	10681179	10682673	10683068	10683966	10684241	10685351	10685807
10686270	10687246	10687758	10688026	10689192	10689398	10689923	10690032
10691061	10691675	10693164	10694854	10695058	10695063	10695826	10696513
10696757	10697312	10697726	10698118	10698480	10698568	10699558	10700234
10700492	10701473	10701693	10702123	10702334	10702367	10702435	10702618
10703018	10703136	10703623	10703880	10704047	10704072	10704280	10704864
10705662	10705880	10706287	10706887	10707770	10708095	10708109	10708580
10708907	10709120	10709168	10709409	10709919	10710080	10710171	10710518
10710619	10710741	10710752	10710815	10710965	10711491	10711500	10711652
10711675	10712113	10712536	10712751	10712923	10713158	10713186	10713669
10714092	10714306	10714346	10715175	10715230	10715265	10715327	10715728
10715892	10716106	10716247	10716303	10716725	10716752	10716755	10716969
10716976	10717055	10717743	10718119	10718129	10718183	10718214	10718388
10718603	10718715	10718950	10718954	10718960	10719463	10719497	10719813
10719851	10720096	10720105	10720178	10720320	10720391	10720418	10720544
10720588	10720696	10720834	10721018	10721181	10721245	10721335	10721420
10721568	10721841	10722008	10722043	10722189	10722305	10722612	10722619
10722785	10722987	10723042	10723108	10723252	10723360	10723453	10723463
10723573	10723589	10723627	10723651	10723683	10724241	10724436	10724513
10724601	10724746	10724788	10724857	10724859	10724919	10724922	10724937
10724980	10725080	10725109	10725126	10725128	10725236	10725330	10725333
10725417	10725495	10725700	10725868	10725874	10725906	10725960	10726048
10726265	10726313	10726335	10726366	10726571	10726740	10726773	10727125
10727182	10727208	10727258	10727416	10727548	10727614	10727716	10727730
10727909	10727931	10727946	10728179	10728183	10728295	10728329	10728487
10728528	10728648	10728692	10728697	10728698	10728816	10728974	10729195
10729280	10729358	10729400	10729574	10729594	10729604	10729671	10729708
10729721	10729764	10729875	10729926	10729956	10730005	10730038	10730064
10730161	10730395	10730483	10730485	10730641	10730785	10730804	10730827
10730982	10731054	10731149	10731174	10731432	10731484	10731504	10731569
10731758	10731804	10731809	10731833	10732088	10732213	10732272	10732335
10732379	10732548	10732605	10732753	10732798	10732852	10732900	10732942
10732990	10733062	10733233	10733283	10733294	10733363	10733393	10733601
10733648	10733707	10733716	10733746	10733755	10733760	10733804	10733840
10733853	10733883	10734060	10734213	10734259	10734298	10734303	10734322

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.0							
10734371	10734496	10734526	10734699	10734752	10734839	10734859	10734971
10734999	10735028	10735065	10735233	10735438	10735651	10735674	10735702
10735759	10735804	10735844	10735935	10735975	10736002	10736064	10736222
10736225	10736351	10736367	10736384	10736486	10736587	10736616	10736666
10736676	10736838	10737045	10737130	10737161	10737165	10737294	10737491
10737566	10737603	10737621	10737644	10737773	10738061	10738093	10738546
10738642	10738665	10738724	10738772	10738789	10738795	10739014	10739037
10739153	10739422	10739536	10739578	10739671	10739736	10739792	10739809
10739856	10740145	10740310	10740387	10740439	10740441	10740505	10740555
10740705	10740728	10740857	10740981	10740984	10740989	10741175	10741176
10741339	10741347	10741369	10741378	10741395	10741400	10741596	10741612
10741758	10741760	10741801	10741886	10742128	10742241	10742260	10742314
10742329	10742345	10742386	10742425	10742466	10742502	10742618	10742619
10742626	10742682	10742717	10742850	10742884	10742913	10742950	10743086
10743202	10743209	10743222	10743254	10743261	10743401	10743480	10743498
10743535	10743541	10743580	10743610	10743641	10743677	10743679	10743699
10743703	10743772	10743793	10743834	10743851	10743893	10743898	10744017
10744018	10744173	10744248	10744465	10744520	10744533	10744677	10744710
10744767	10744860	10744937	10745070	10745086	10745145	10745161	10745172
10745208	10745299	10745409	10745578	10745619	10745636	10745936	10746425
10746467	10746528	10746555	10746558	10746560	10746606	10746634	10746660
10746662	10746697	10746796	10746912	10746914	10746927	10746999	10747006
10747020	10747030	10747078	10747099	10747103	10747138	10747209	10747210
10747269	10747277	10747298	10747311	10747319	10747350	10747488	10747520
10747687	10747704	10747763	10747786	10747795	10747816	10748052	10748053
10748137	10748138	10748154	10748354	10748469	10748617	10748680	10748702
10748747	10748822	10749023	10749034	10749048	10749162	10749218	10749330
10749350	10749463	10749488	10749630	10749728	10749779	10749845	10749918
10749947	10750014	10750017	10750047	10750140	10750161	10750185	10750240
10750245	10750305	10750321	10750358	10750391	10750406	10750452	10750486
10750612	10750619	10750663	10750667	10750764	10750839	10750939	10750987
10751015	10751051	10751081	10751099	10751168	10751195	10751202	10751208
10751222	10751430	10751446	10751607	10751610	10751701	10751723	10751780
10751894	10751903	10751918	10751949	10751960	10752097	10752101	10752121
10752150	10752189	10752281	10752352	10752406	10752556	10752559	10752582
10752608	10752755	10752786	10752815	10752832	10752861	10752897	10752961
10753021	10753024	10753032	10753055	10753091	10753113	10753138	10753354
10753570	10753667	10753684	10753685	10753693	10753779	10753800	10753810
10753816	10753821	10753826	10753834	10753843	10753876	10753929	10753969
10754040	10754068	10754117	10754148	10754238	10754266	10754284	10754400

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.0							
10754528	10754540	10754550	10754552	10754585	10754697	10754881	10754908
10754941	10755021	10755030	10755053	10755083	10755142	10755317	10755386
10755406	10755467	10755543	10755570	10755729	10755739	10755803	10755838
10755946	10755953	10755968	10755976	10755981	10756118	10756140	10756143
10756164	10756182	10756268	10756272	10756353	10756377	10756474	10756509
10756510	10756551	10756661	10756662	10756739	10756767	10756782	10756893
10757176	10757324	10757338	10757440	10757518	10757800	10757833	10757841
10757875	10758062	10758235	10758245	10758266	10758272	10758315	10758356
10758489	10758585	10758980	10759217	10759451	10759453	10759542	10759547
10759626	10759647	10759660	10759884	10759940	10759992	10760038	10760115
10760142	10760444	10760519	10760545	10760787	10760815	10760857	10760914
10761036	10761157	10761247	10761355	10761377	10761551	10761618	10761697
10761706	10761723	10761833	10761836	10761942	10762648	10762796	10763377
10763581	10763645	10763666	10763747	10764570	10765113	10765175	

Software Patches Included in this Release

The Quartus II software version 10.0 includes the following patches released for the Quartus II software version 9.1 SP2:

Patch	Knowledge Database Solution ID	Knowledge Database Solution Title	Product Affected
2.01	rd02232010_42	Why does the TimeQuest GUI on Linux hang when I access it remotely?	TimeQuest Timing Analyzer
2.03	—	—	ALTGXB
2.06	rd04092010_488	Are there any known issues with the On-Chip Clamp Diode assignments in the Quartus II software versions 9.1 SP2 and earlier?	Assembler
2.07	—	—	PowerFit Fitter
2.08	rd04132010_586	How do I enable Configuration / Programming file generation for Cyclone III LS EP3CLS70 and EP3CLS100 devices in Quartus II 9.1 SP2?	Programmer
2.12	—	—	Programmer
2.13	—	—	PowerFit Fitter
2.15	rd04152010_601	Is there a known issue when trying to JTAG a EP4SGX290NF45 or EP4SGX360NF45 device in the Quartus II software version 9.1 and later?	Programmer
2.16	—	—	Programmer
2.17	—	—	ALTGXB
2.18	rd05192010_821	Are there any known issues with PCI Express x4 and x8 Link Training and Negotiation in Stratix IV GX and Arria II GX devices?	PCI Express Compiler
2.25	—	—	Pin Planner
2.28	—	—	Parallel Flash Loader

Patch	Knowledge Database Solution ID	Knowledge Database Solution Title	Product Affected
2.31	—	—	PowerPlay Power Analyzer
2.32	—	—	PowerFit Fitter
2.34	—	—	PowerFit Fitter
2.38	—	—	ALTGX
2.40	rd05042010_156	Why does timing analysis for the Cyclone IV GX I7 devices report failures for setup and recovery paths in the Quartus II software version 9.1 SP2?	PowerFit Fitter
2.43	—	—	PowerFit Fitter
2.49	rd06022010_582	Internal Error: Sub-system: ASMIO, File: /quartus/comp/asmio/asmio_pin_model.cpp, Line: 1689	Programmer
2.52	rd06142010_464	Why can't I find SFL images for my device in the Quartus II software version 9.1 SP2?	Programmer
2.61	—	—	Programmer

Revision History

Revision	Description
1.0	Initial Release



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